LED Driver with Average-Mode Constant Current Control

Halogen Free

General Description

The FP7125 is an average current mode control LED driver IC operating in a constant off-time mode. FP7125 does not produce a peak-to-average error, and therefore greatly improves accuracy, line and load regulation of the LED current without any need for loop compensation or high-side current sensing. The output LED current accuracy is ±3%.

The FP7125 can be powered from an 8.0 - 100V supply. PWM & Linear dimming input is provided that accepts an external control TTL compatible signal. The output current can be programmed by an internal 250mV reference.

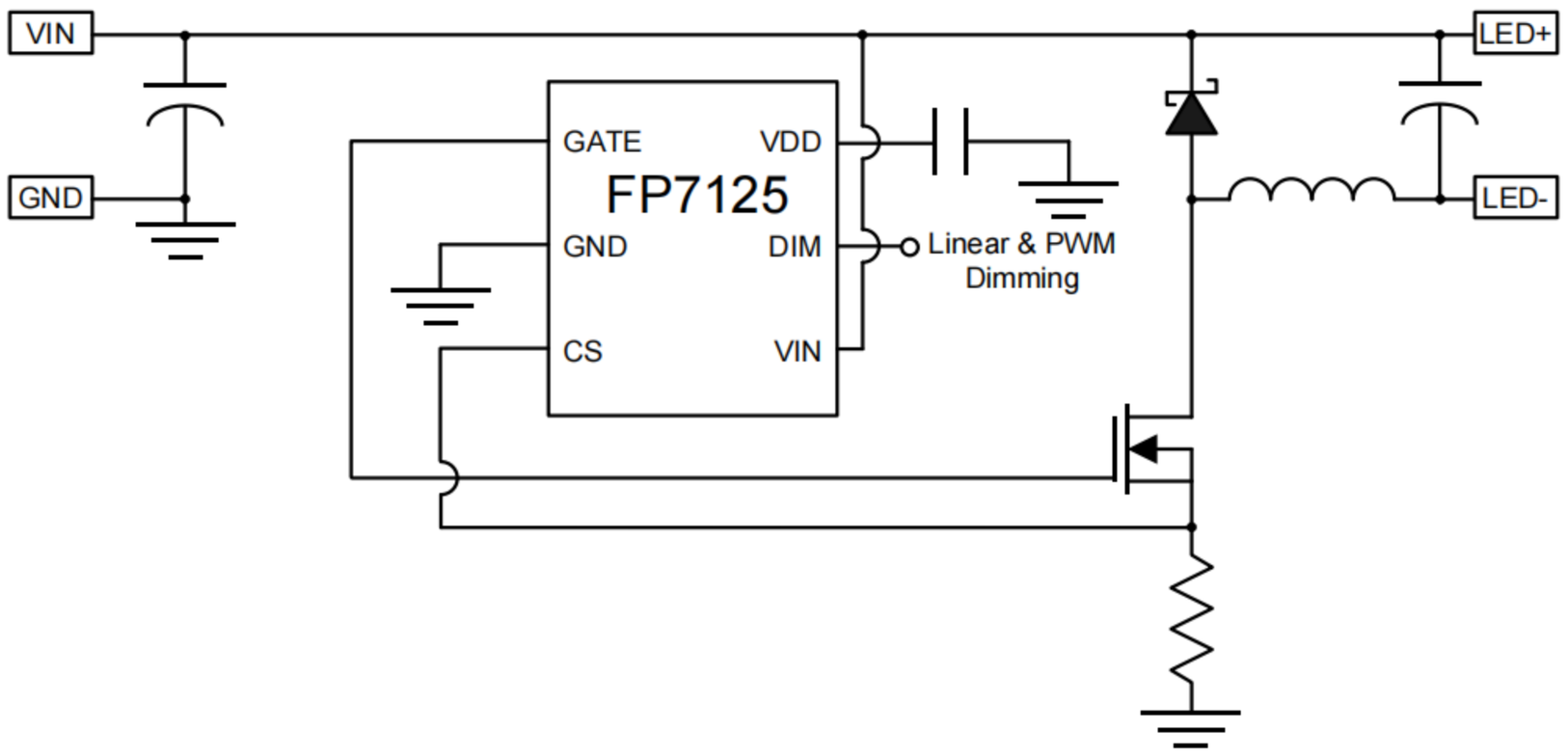
Features

- Fast Average Current Control
- Internal 8 to 100V Linear Regulator
- Linear and PWM Dimming Capability
- Output Short Circuit Protection with Skip Mode
- Requires Few External Components for Operation

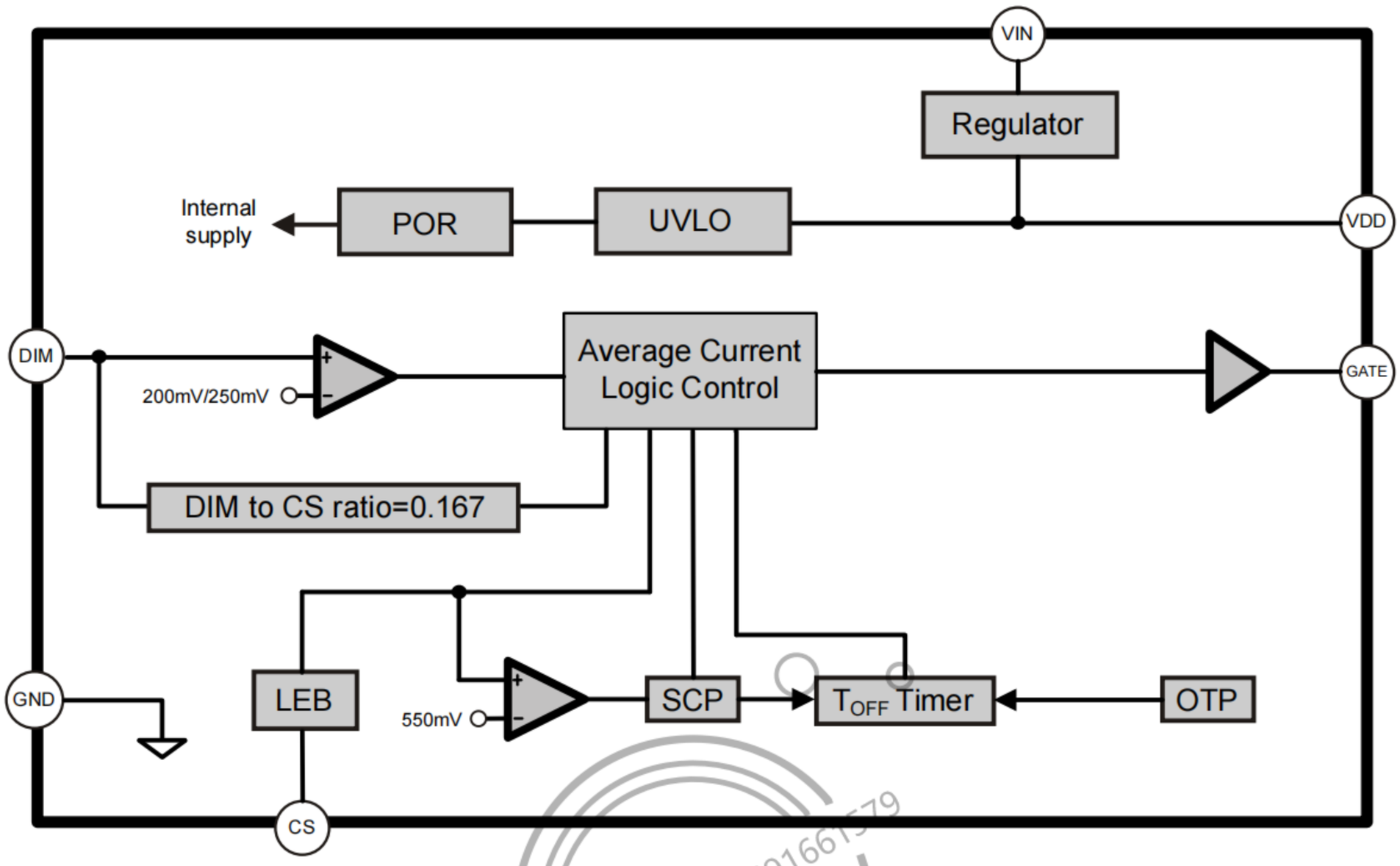
Applications

- DC/DC or AC/DC LED Driver Applications
- LED Street Lighting
- Back Lighting of Flat Panel Displays
- General Purpose Constant Current Source
- Signage and Decorative LED Lighting
- Chargers

Typical Application Circuit

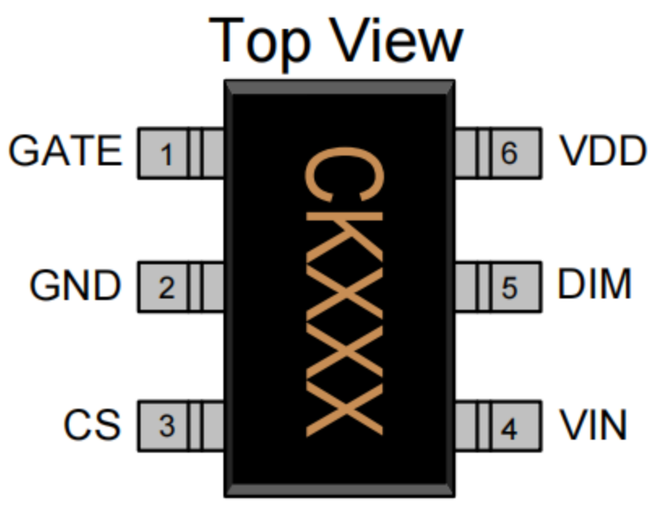


Function Block Diagram



Pin Descriptions

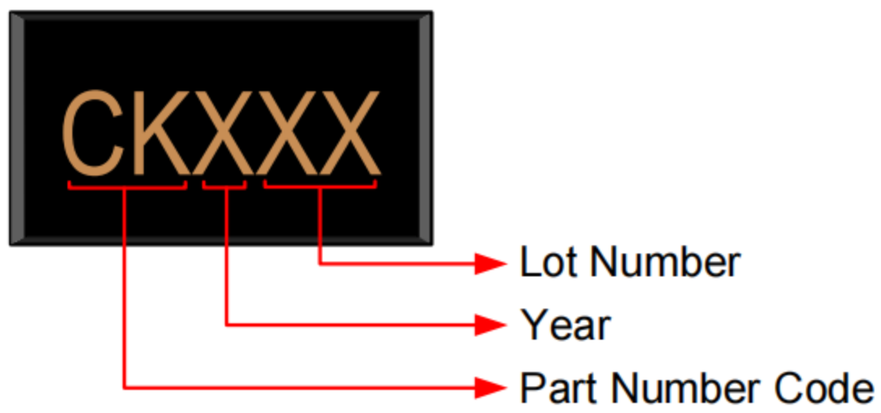
SOT23-6L



Name	No.	I / O	Description
GATE	1	O	This pin is the output GATE driver for an external N-channel power MOSFET.
GND	2	P	Ground return for all internal circuitry.
CS	3	I	This pin is the current sense pin used to sense the FET current by means of an external sense resistor.
VIN	4	P	This pin is the input of an 8 - 100V linear regulator.
DIM	5	I	This pin is the linear & PWM dimming input of the IC.
VDD	6	I	This is the power supply pin for all internal circuits.

Marking Information

SOT23-6L



Lot Number: Wafer lot number's last two digits

For Example: XX486 → 86

Year: Production year's last digit

Part Number Code: Part number identification code for this product. It should be always "CB".

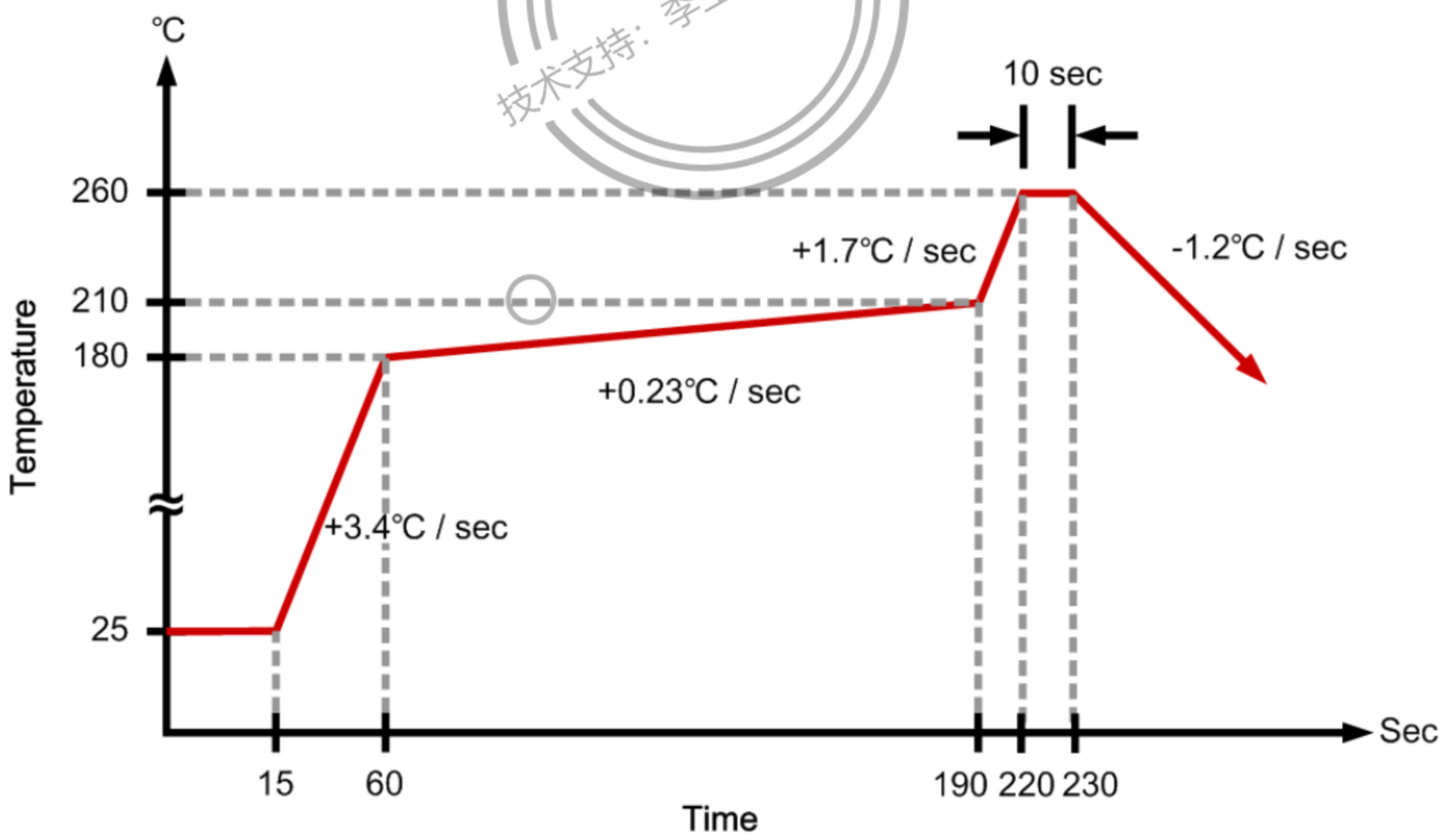
Ordering Information

Part Number	Code	Ambient Operating Temperature	Junction Operating Temperature	Package	MOQ	Description
FP7125LR-G1	CB	-25°C ~ +85°C	-25°C ~ +125°C	SOT23-6L	3000 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{IN}	V_{IN} to GND			100	V
	V_{DD}	V_{DD} to GND			8.5	V
CS, DIM, GATE			-0.3		V_{DD}-0.3V	V
Allowable Power Dissipation	P_D	SOT23-6L $T_A \leqq +25°C$			455	mW
Junction to Ambient Thermal Resistance	θ_{JA}				220	°C / W
Operating Temperature			-25		+85	°C
Storage Temperature	T_S	SOT23-6L	-40		+150	°C
SOT23-6L Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		8		100	V
Ambient Operating Temperature			-25		+85	°C
Junction Operating Temperature			-25		+125	°C

DC Electrical Characteristics (V_{IN}=11V,T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal Regulator						
Internally regulated voltage	V_{DD}	VIN = 8V, $I_{DD(ext)}$= 0, 500pF at GATE;DIM = VDD	7.25	7.5	7.75	V
Line regulation of VDD	$\Delta V_{DD,line}$	VIN = 8 – 100V, $I_{DD(ext)}$=0, 500pF at GATE; DIM = VDD	0	-	1.0	V
Load regulation of V_{DD}	$\Delta V_{DD,load}$	$I_{DD(ext)}$ = 0 – 0.6mA, 500pF at GATE; DIM = VDD	0		100	mV
Shutdown current	I_{SD}	V_{DIM}=0V		0.4		mA
V_{DD} undervoltage lockout threshold	UVLO	V_{DD} rising		6.3		V
V_{DD} undervoltage lockout hysteresis	ΔUVLO	V_{DD} falling		500		mV
PWM Dimming						
Pin DIM input low voltage	$V_{EN(lo)}$	V_{IN} = 8 - 100V			0.1	V
Pin DIM input high voltage	$V_{EN(hi)}$	V_{IN} = 8 - 100V	1.6			V
Average Current Sense Logic						
Current sense reference voltage	V_{CS}		243	250	257	mV
DIM-to-CS voltage ratio	$A_{V(DIM)}$			0.167		
DIM-to-CS voltage offset	$AV_{DIM(OFFSET)}$	Offset = $V_{CS} – A_{V(DIM)} \cdot V_{DIM}$ V_{DIM}=1.2V	0		10	mV
CS threshold temp regulation					5	mV
DIM input voltage, shutdown	$V_{DIM(OFF)}$			200		mV
DIM input voltage, enable	$\Delta V_{DIM(OFF)}$			250		mV
Current sense blanking interval	T_{BLANK}		150		320	ns
Minimum steady-state duty cycle	$T_{ON(min)}$	CS=V_{CS} + 30mV			1000	ns
Short Circuit Protection						
Hiccup threshold voltage	V_{CS}		495	550	605	mV
Short circuit hiccup time	T_{HICCUP}		450	550	650	us
Minimum on-time (short circuit)	$T_{ON(min)}$	CS=V_{DD}			600	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
GATE Driver						
GATE sourcing current	I_{SOURCE}	V_{GATE} = 0V, V_{DD} = 7.5V	165			mA
GATE sinking current	I_{SINK}	V_{GATE} = V_{DD}, V_{DD} = 7.5V	165			mA
GATE output rise time	t_{RISE}	C_{GATE} = 500pF, V_{DD} = 7.5V		30	50	ns
GATE output fall time	t_{FALL}	C_{GATE} = 500pF, V_{DD} = 7.5V		30	50	ns
OFF-Time						
Minimum off time	$T_{OFF(MIM)}$			0.6		us
Maximum off time	$T_{OFF(MAX)}$			50		us
Maximum on time	$T_{ON(MAX)}$			60		us
Thermal Protection						
Thermal protection				130		°C
Thermal shutdown				150		°C

Function Description

Input Voltage Regulator

The FP7125 can be powered directly from its VIN pin and can work from 8.5 - 100VDC at its VIN pin. When a voltage is applied at the VIN pin, the FP7125 maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The FP7125 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the FP7125 will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 8.5V.

In the above equation, f_S is the switching frequency and QG is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

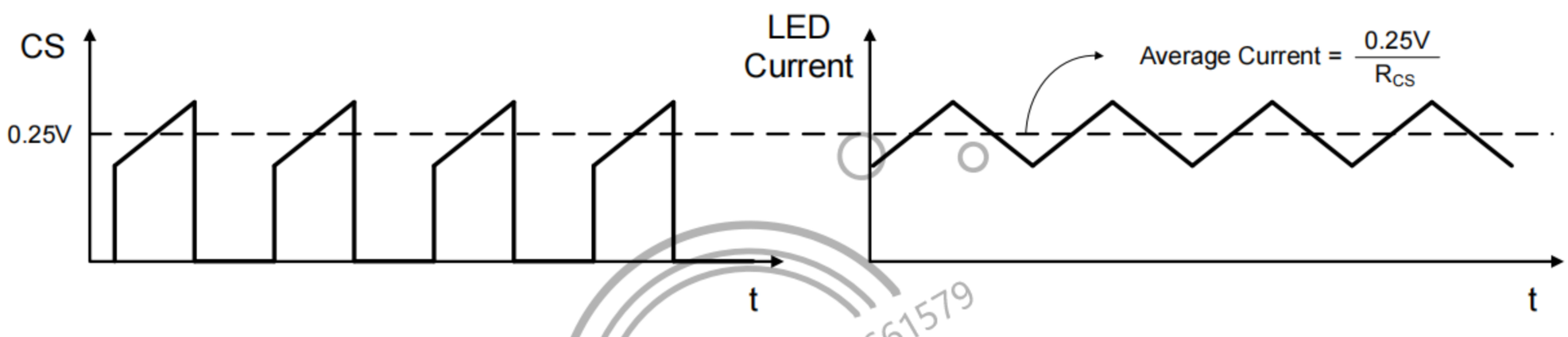
Average Current Control

The LED current is detected using a sense resistor at the CS pin. The feedback operates in a fast open-loop mode. No compensation is required. When the voltage at the DIM input $V_{DIM} \geq 1.5V$, output current is programmed simply as:

$$I_{LED}(A) = \frac{0.25V}{R_{CS}(\Omega)}$$

Otherwise:

$$I_{LED}(A) = \frac{V_{DIM}(V) \times 0.167}{R_{CS}(\Omega)}$$



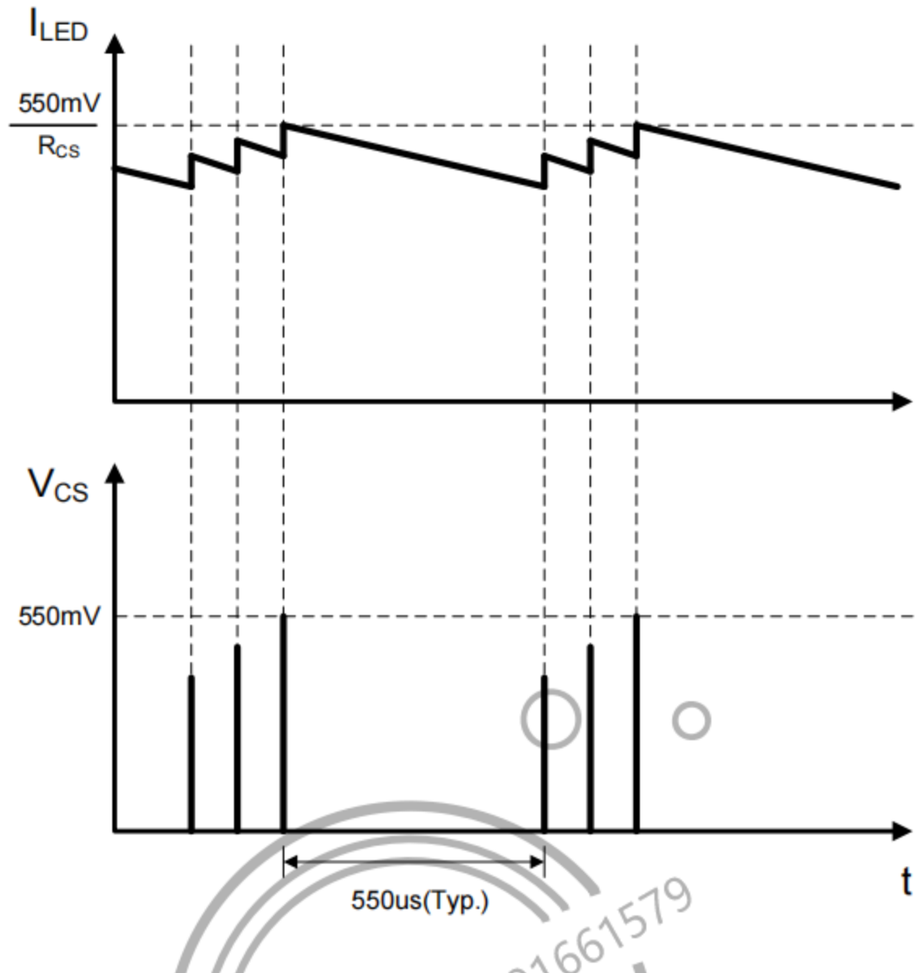
The above equations are only valid for continuous conduction of the output inductor. It is a good practice to design the inductor such that the switching ripple current in it is 25% of its average peak-to-peak, full load, DC current.

GATE Output

The GATE output of the FP7125 is used to drive an external MOSFET. It is recommended that the gate charge QG of the external MOSFET be less than 25nC for switching frequencies ≤100kHz and less than 15nC for switching frequencies >100kHz.

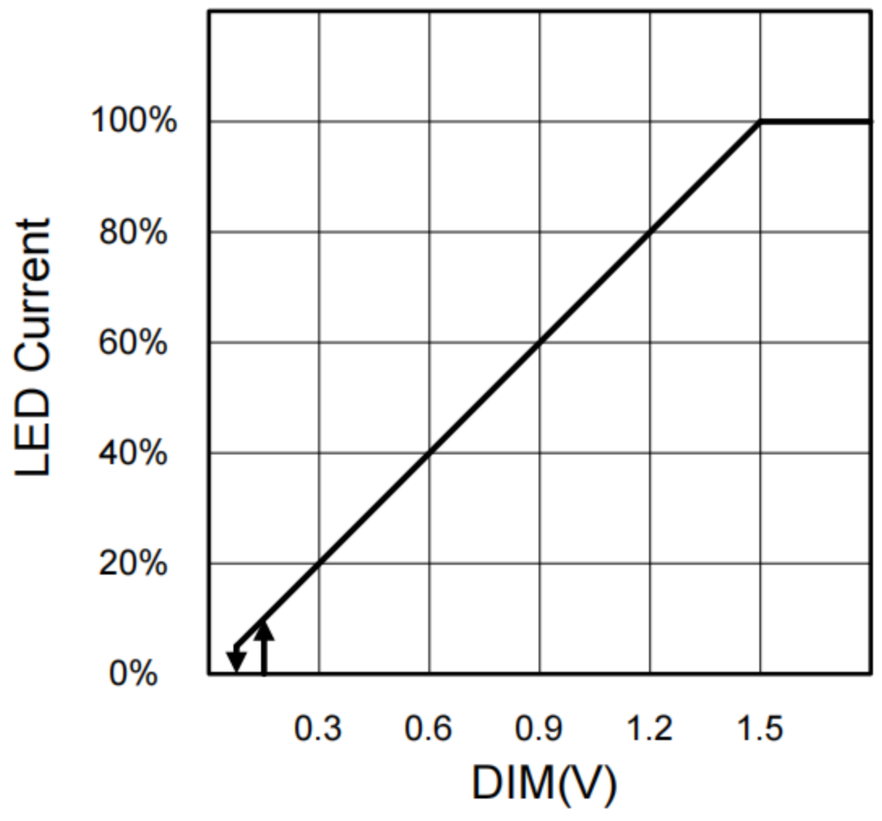
Output Short Circuit Protection

The short circuit protection comparator trips when the voltage at CS exceeds 0.55V. When this occurs, the GATE off-time T_{HICCUP} = 550μs is generated to prevent stair-casing of the inductor current and potentially its saturation due to insufficient output voltage.



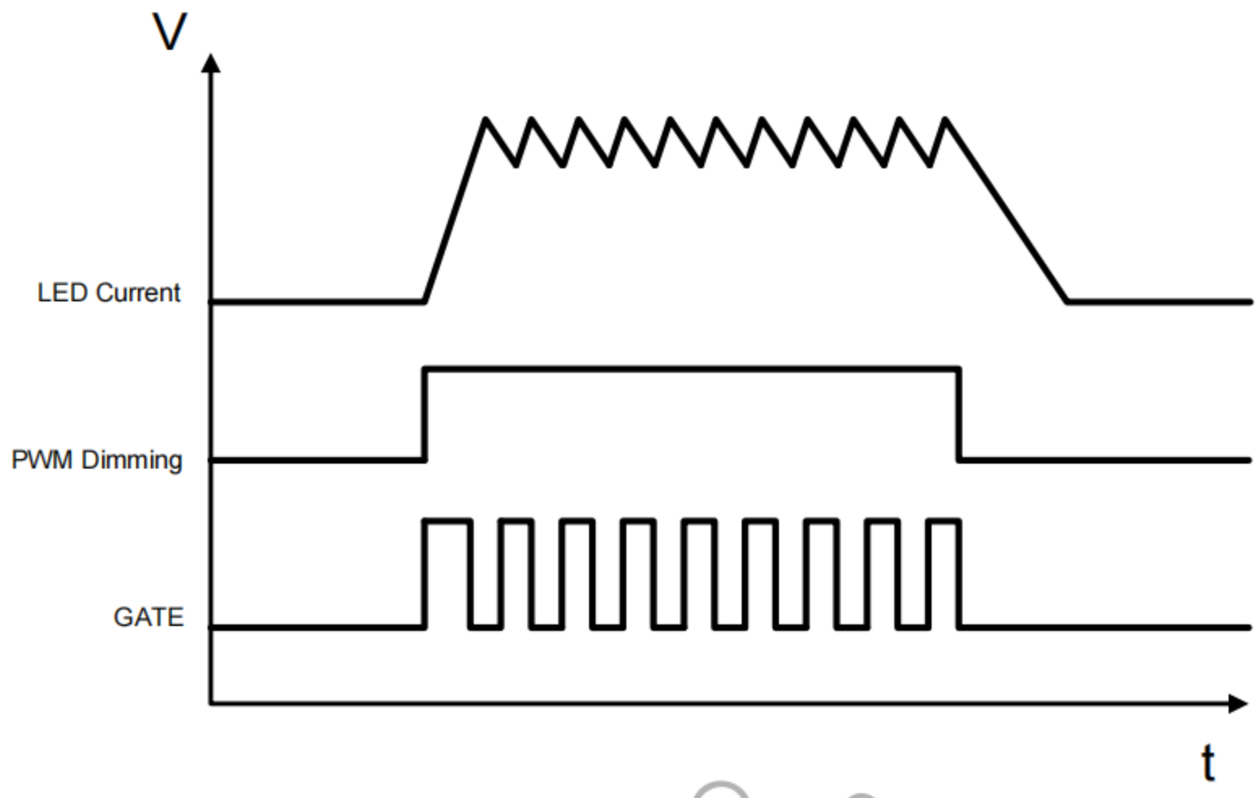
Linear Dimming

When the voltage at DIM falls below 1.5V, the internal 250mV reference to the constant-current feedback becomes overridden by V_{DIM} • 0.167. As long as the current in the inductor remains continuous, the LED current is given by the equation above. However, when V_{DIM} falls below 200mV, the GATE output becomes disabled. The GATE signal recovers, when V_{DIM} exceeds 250mV. This is required in some applications to be able to shut the LED lamp off with the same signal input that controls the brightness.



PWM Dimming

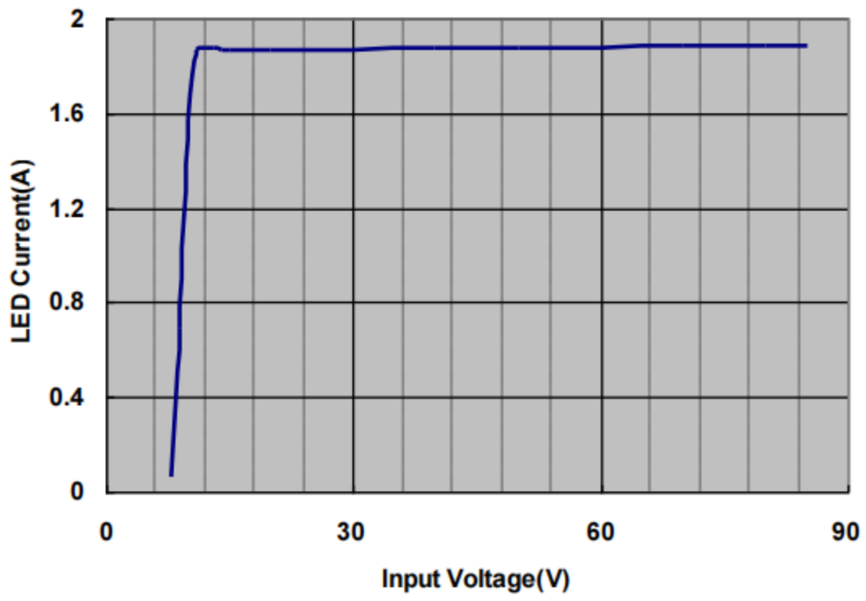
Due to the fast open-loop response of the average-current control loop of the FP7125, its PWM dimming performance nearly matches that of the FP7171.



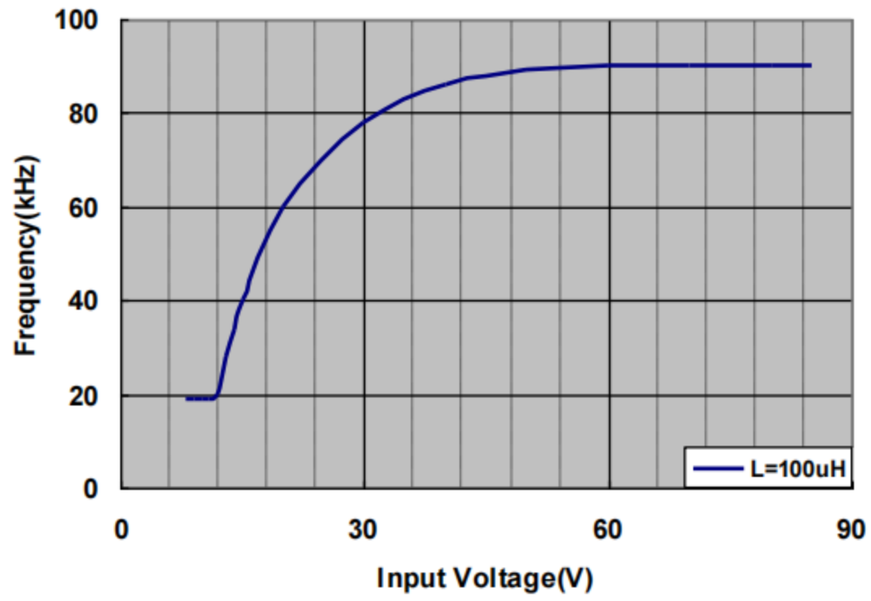
The rising and falling edges are limited by the current slew rate in the inductor. The first switching cycle is terminated upon reaching the 250mV (V_{DIM} • 0.167) level at CS. The circuit is further reaching its steady-state within 1 switching cycles regardless of the switching frequency.

※ V_{IN}=12V, LED=9.2V, T_A = 25°C, unless otherwise noted

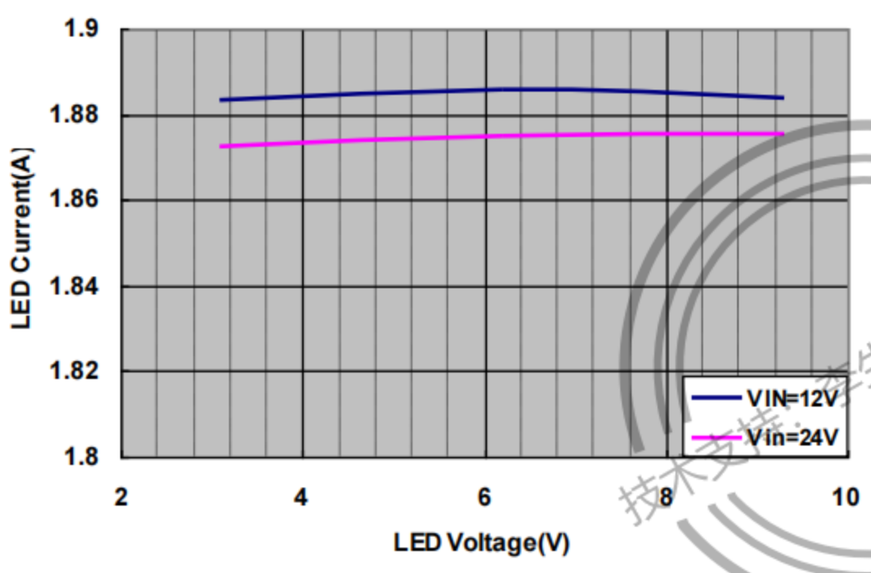
Input Voltage VS LED Current



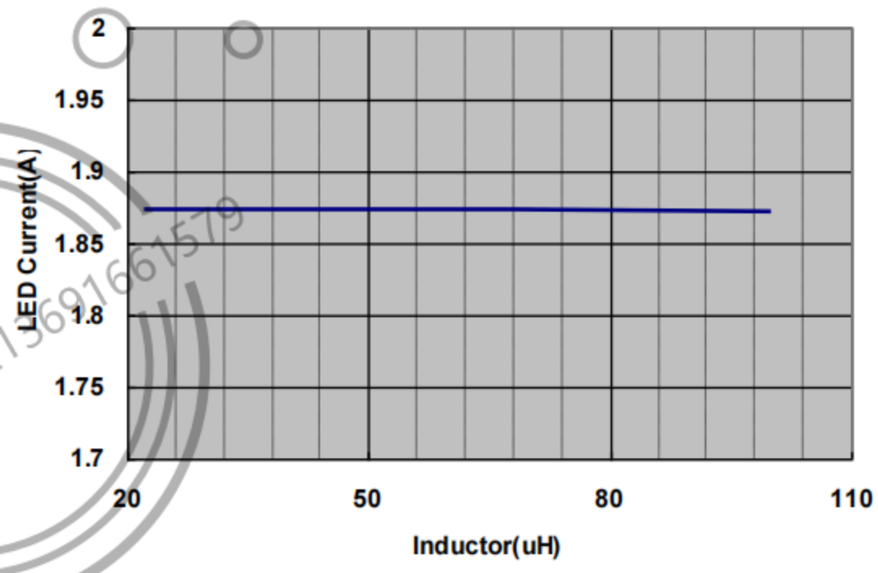
Input Voltage VS Frequency



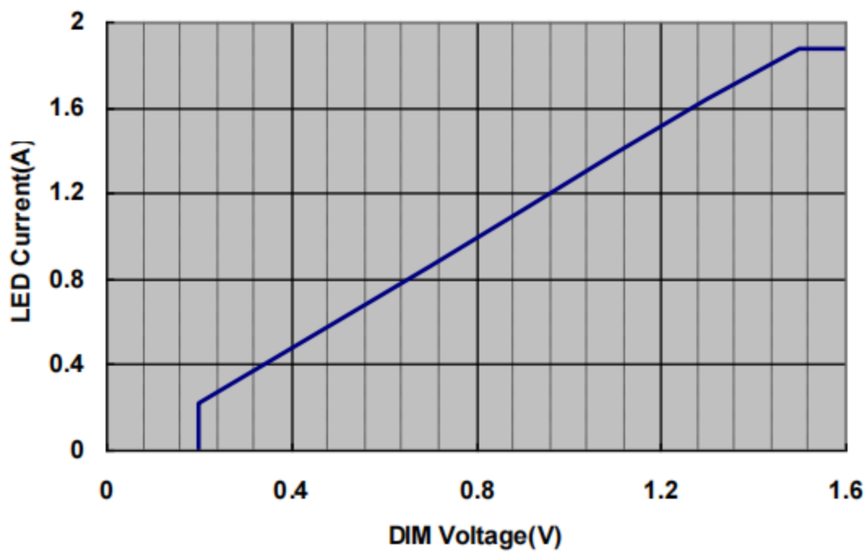
LED Voltage VS LED Current



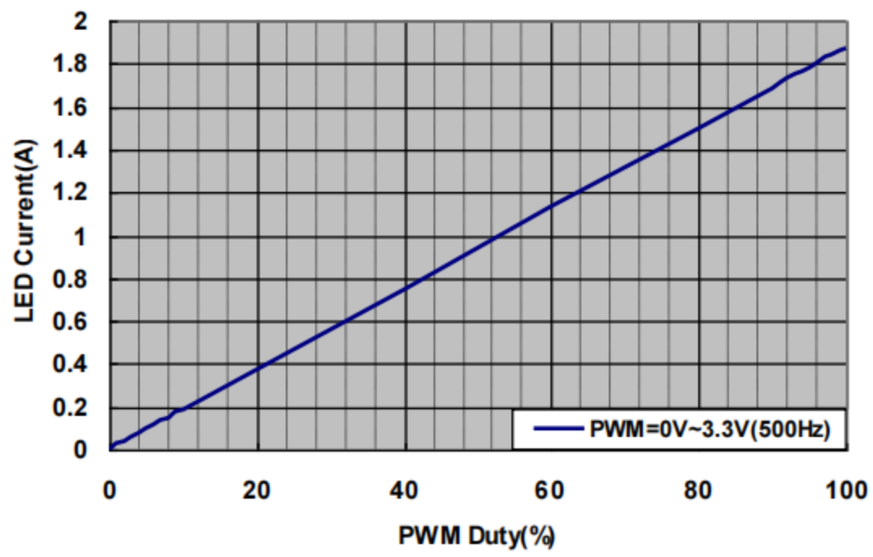
Inductor VS LED Current



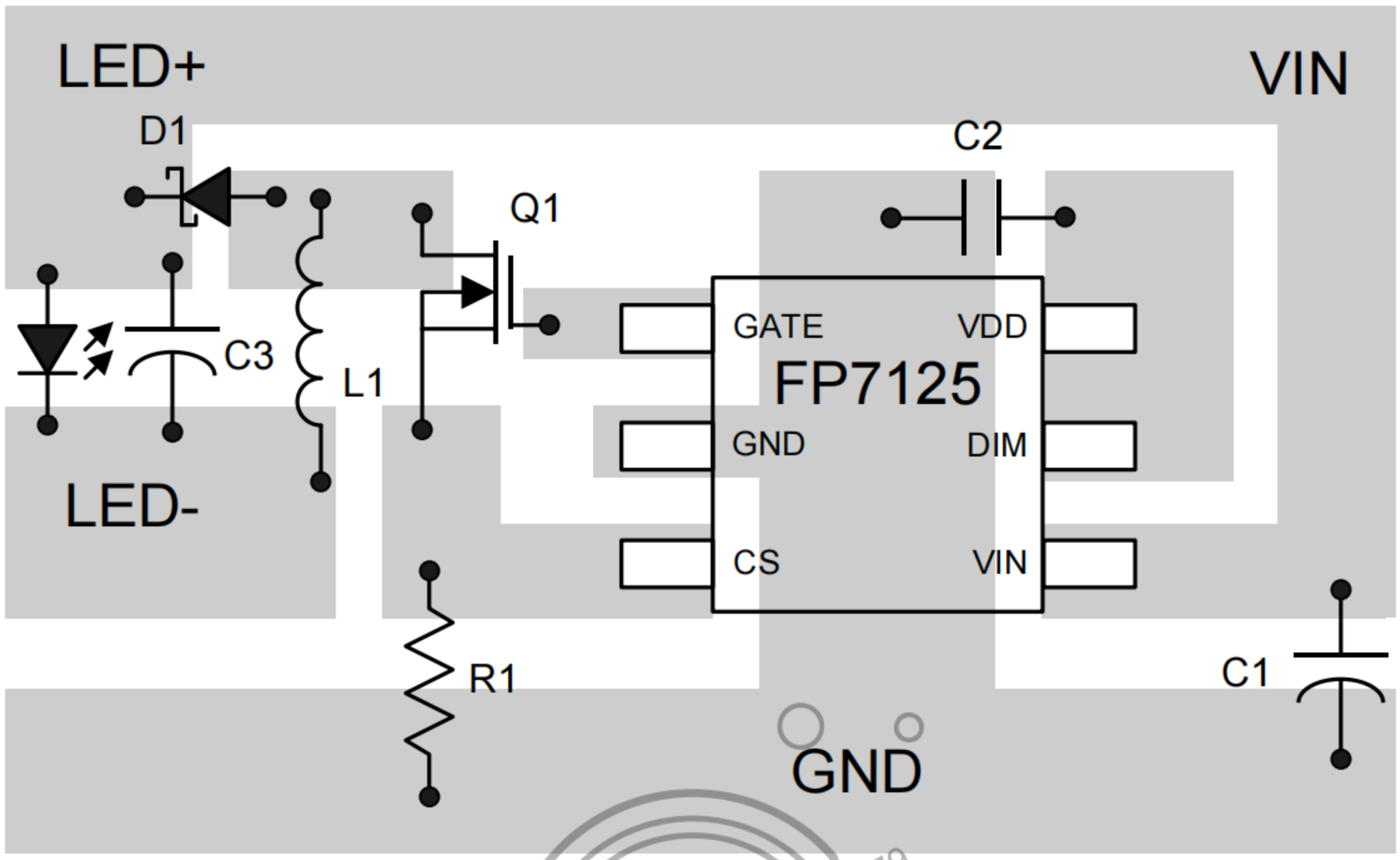
DIM Voltage VS LED Current



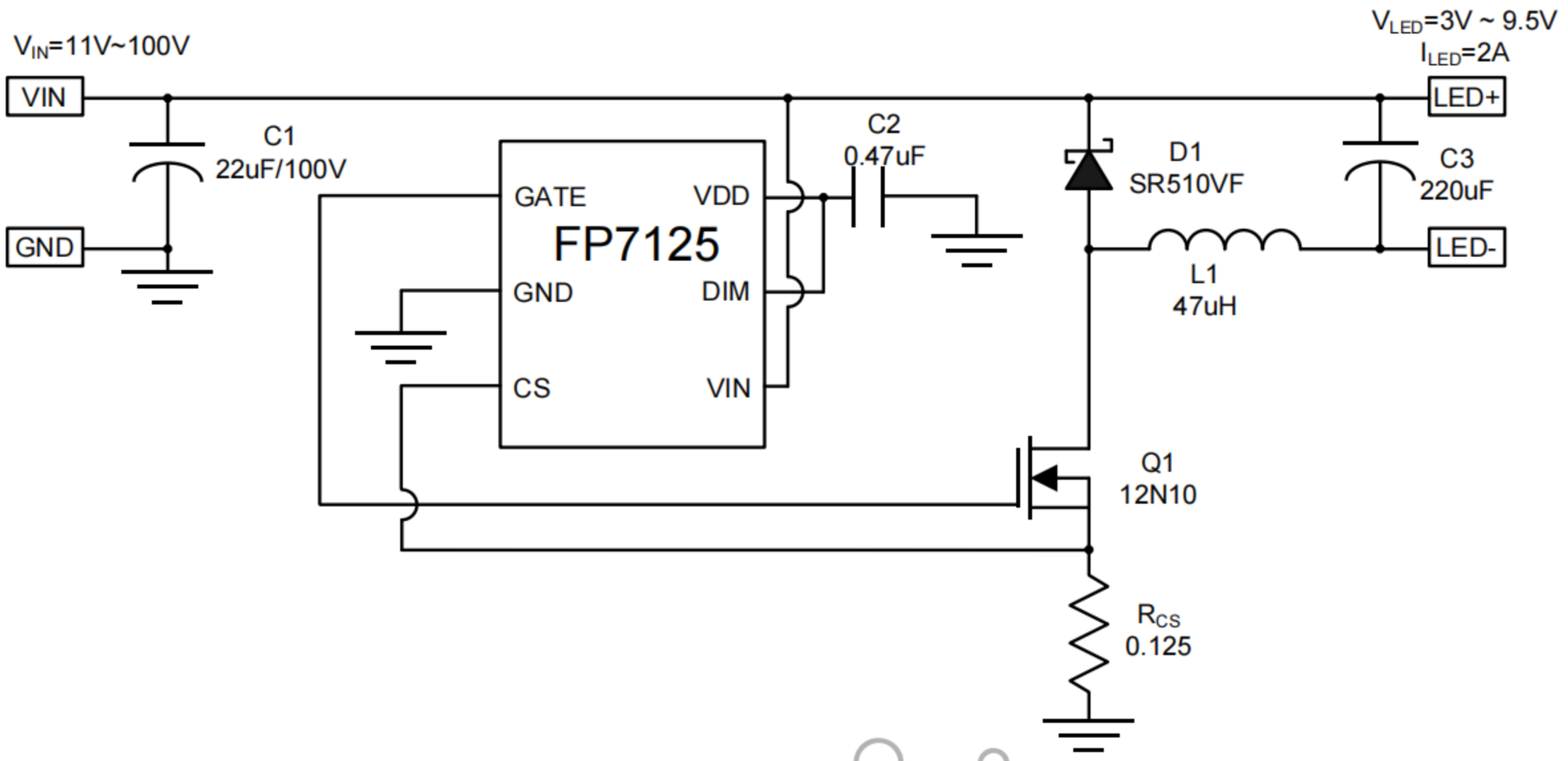
PWM Duty VS LED Current



Suggested Layout

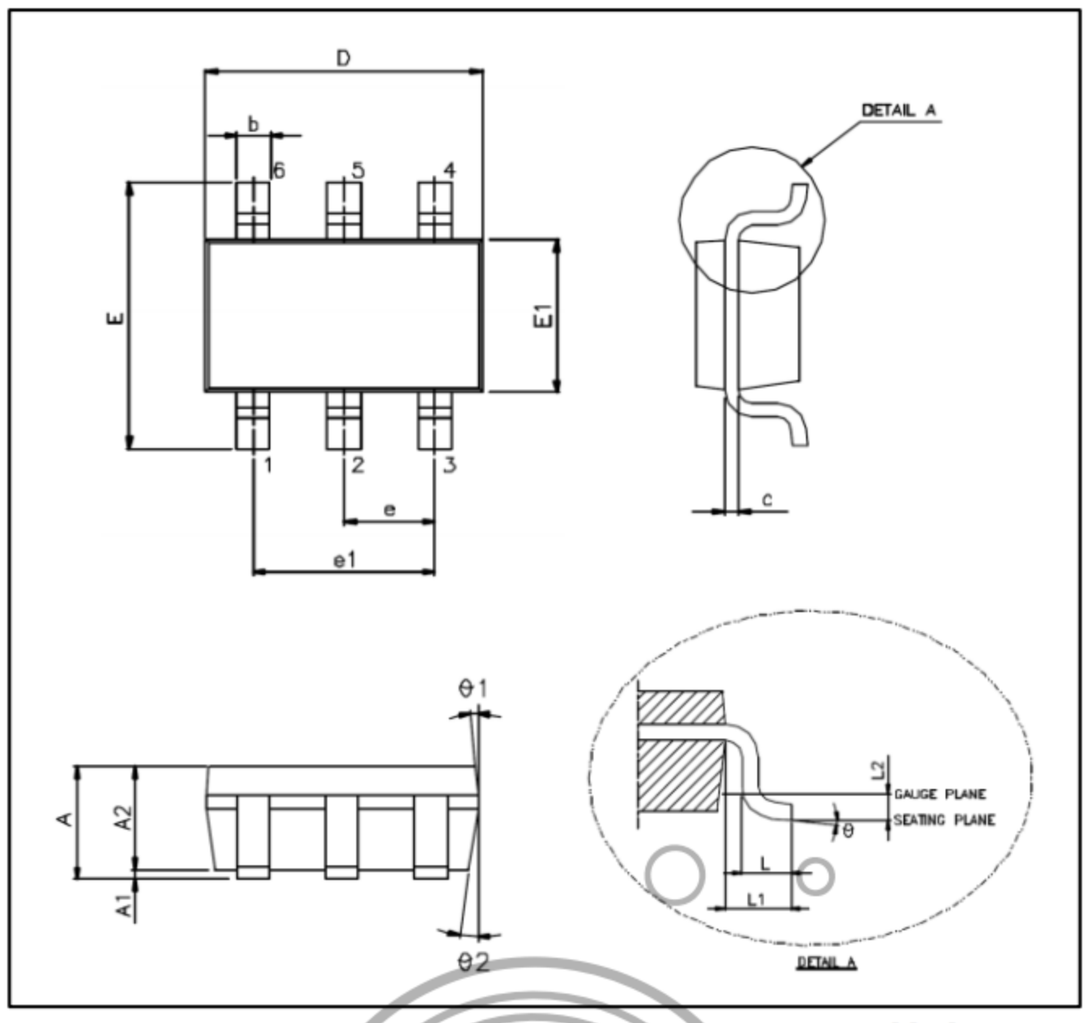


Typical Application Circuit



Package Outline

SOT23-6L



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	1.050	1.450
A1	0.050	0.150
A2	0.900	1.300
b	0.300	0.500
c	0.080	0.220
D	2.900 BSC	
E	2.800 BSC	
E1	1.600 BSC	
e	0.950 BSC	
e1	1.900 BSC	
L	0.300	0.600
L1	0.600 REF	
L2	0.250 BSC	
θ°	0°	8°
θ1°	3°	7°
θ2°	6°	15°

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-178 AB.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E1” does not include inter-lead flash or protrusions.