

LED Driver with Average-Mode Constant Current Control



General Description

The FP7189 is an average current mode control LED driver IC operating in a constant off-time mode. FP7189 does not produce a peak-to-average error, and therefore greatly improves accuracy, line and load regulation of the LED current without any need for loop compensation or high-side current sensing. The output LED current accuracy is $\pm 2\%$.

The FP7189 can be powered from an 8.0 - 100V supply. A PWM dimming input is provided that accepts an external control TTL compatible signal. The output current can be programmed by an internal 250mV reference, or controlled externally through a 0.2 – 1.5V dimming input.

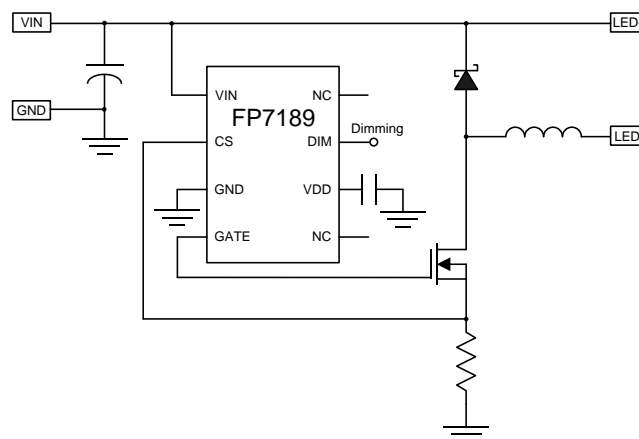
Features

- Fast average current control
- Internal 8 to 100V linear regulator
- Linear and PWM dimming capability
- Output short circuit protection with skip mode
- Requires few external components for operation

Applications

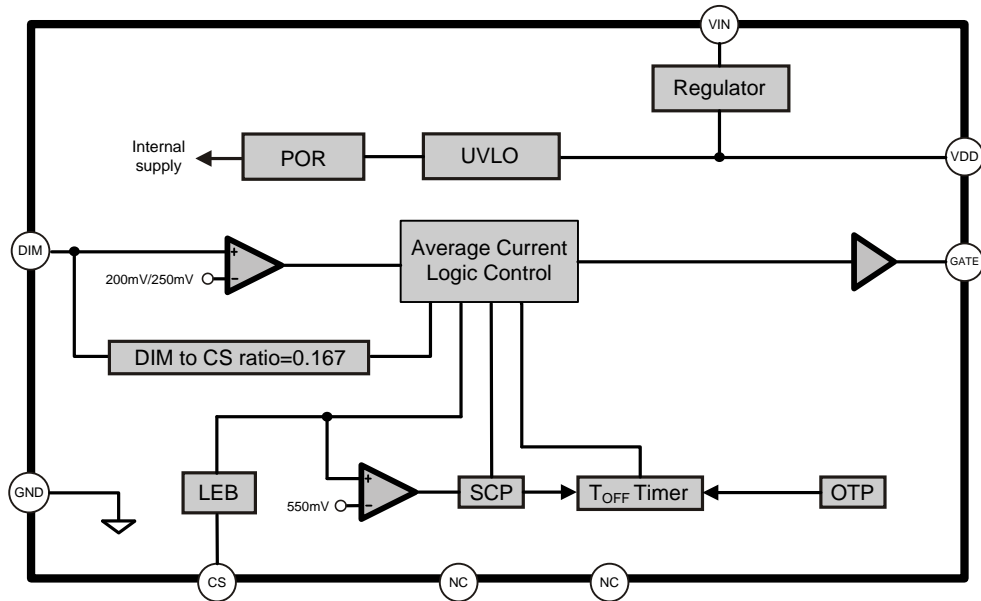
- DC/DC LED driver applications
- LED street lighting
- Back lighting of flat panel displays
- General purpose constant current source
- Signage and decorative LED lighting
- Chargers

Typical Application Circuit



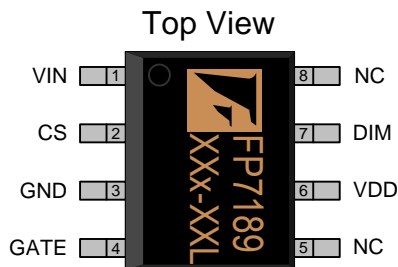
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Function Block Diagram



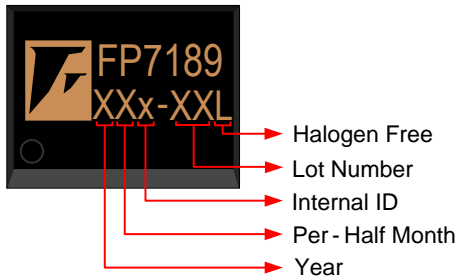
Pin Descriptions

SOP-8L



Name	No.	I / O	Description
VIN	1	P	This pin is the input of an 8 - 100V linear regulator.
CS	2	I	This pin is the current sense pin used to sense the FET current by means of an external sense resistor.
GND	3	P	Ground return for all internal circuitry.
GATE	4	O	This pin is the output GATE driver for an external N-channel power MOSFET.
NC	5	-	No connect.
VDD	6	P	This is the power supply pin for all internal circuits.
DIM	7	I	This pin is the linear and PWM dimming input of the IC.
NC	8	-	No connect.

Marking Information



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example → Lot : 123456 → XXx-56L

Internal ID: Internal Identification Code

Per-Half Month: Production period indicator in half month time unit

For Example : A → First Half Month of January
B → Second Half Month of January
C → First Half Month of February
D → Second Half Month of February

Year: Production year's last digit

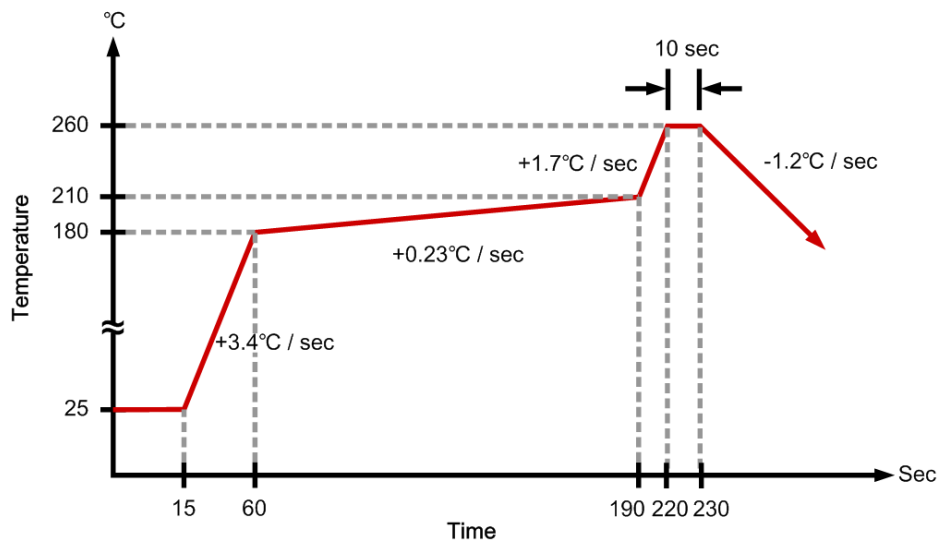
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP7189DR-G1	-25°C ~ +85°C	SOP-8L	2500 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{IN}	V_{IN} to GND			100	V
	V_{DD}	V_{DD} to GND			8.5	V
CS, DIM, GATE,			-0.3		$V_{DD}-0.3V$	V
Allowable Power Dissipation	P_D	SOP-8L $T_A \leq +25^\circ C$			630	mW
Junction to Ambient Thermal Resistance	θ_{JA}			128		$^\circ C / W$
Operating Temperature			-25		+85	$^\circ C$
Storage Temperature	T_S	SOP-8L	-40		+150	$^\circ C$
SOP-8L Lead Temperature		(soldering, 10 sec)			+260	$^\circ C$

IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}		8.5		100	V
Operating Temperature			-25		85	°C

DC Electrical Characteristics ($V_{IN}=11V, T_A = 25^\circ C$, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal Regulator						
Internally regulated voltage	V_{DD}	$V_{IN} = 8V, I_{DD(ext)} = 0, 500pF$ at GATE; DIM = VDD	7.25	7.5	7.75	V
Line regulation of VDD	$\Delta V_{DD,line}$	$V_{IN} = 8 - 100V, I_{DD(ext)} = 0, 500pF$ at GATE; DIM = VDD	0	-	1.0	V
Load regulation of V_{DD}	$\Delta V_{DD,load}$	$I_{DD(ext)} = 0 - 0.6mA, 500pF$ at GATE; DIM = VDD	0		100	mV
V_{DD} undervoltage lockout threshold	UVLO	V_{DD} rising	5.75	6.0	6.25	V
V_{DD} undervoltage lockout hysteresis	$\Delta UVLO$	V_{DD} falling		500		mV
PWM Dimming						
Pin DIM input low voltage	$V_{EN(lo)}$	$V_{IN} = 8 - 100V$			0.1	V
Pin DIM input high voltage	$V_{EN(hi)}$	$V_{IN} = 8 - 100V$	1.6			V
Average Current Sense Logic						
Current sense reference voltage	V_{CS}		0.245	0.25	0.255	mV
DIM-to-CS voltage ratio	$A_{V(DIM)}$		0.164	0.167	0.17	
DIM-to-CS voltage offset	$A_{V(DIM)}$ (OFFSET)	Offset = $V_{CS} - A_{V(DIM)} \cdot V_{DIM}$ $V_{DIM}=1.2V$	0		10	mV
CS threshold temp regulation #					5	mV
DIM input voltage, shutdown	$V_{DIM(OFF)}$			200		mV
DIM input voltage, enable	$\Delta V_{DIM(OFF)}$			250		mV
Current sense blanking interval	T_{BLANK}		250		350	ns
Minimum on-time	$T_{ON(min)}$	$CS = V_{CS} + 30mV$			1000	ns
Short Circuit Protection						
Hiccup threshold voltage	V_{CS}		495	550	605	mV
Current limit delay CS – GATE #	T_{DELAY}	$CS = V_{CS} + 30mV$			150	ns
Short circuit hiccup time	T_{HICCUP}		450	550	650	us
Minimum on-time (short circuit)	$T_{ON(min)}$	$CS = V_{DD}$			600	ns

Notes:

Guaranteed by design

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
T_{OFF} Timer						
Minimum off time	T _{OFF(MIM)}			0.6		us
Maximum off time	T _{OFF(MAX)}			50		us
Maximum on time	T _{ON(MAX)}			60		us
GATE Driver						
GATE sourcing current	I _{SOURCE}	V _{GATE} = 0V, V _{DD} = 7.5V	165			mA
GATE sinking current	I _{SINK}	V _{GATE} = V _{DD} , V _{DD} = 7.5V	165			mA
GATE output rise time	t _{RISE}	C _{GATE} = 500pF, V _{DD} = 7.5V		30	50	ns
GATE output fall time	t _{FALL}	C _{GATE} = 500pF, V _{DD} = 7.5V		30	50	ns

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Function Description

Input Voltage Regulator

The FP7189 can be powered directly from its VIN pin and can work from 8.5 - 100VDC at its VIN pin. When a voltage is applied at the VIN pin, the FP7189 maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The FP7189 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the FP7189 will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 8.5V.

In the above equation, f_s is the switching frequency and QG is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

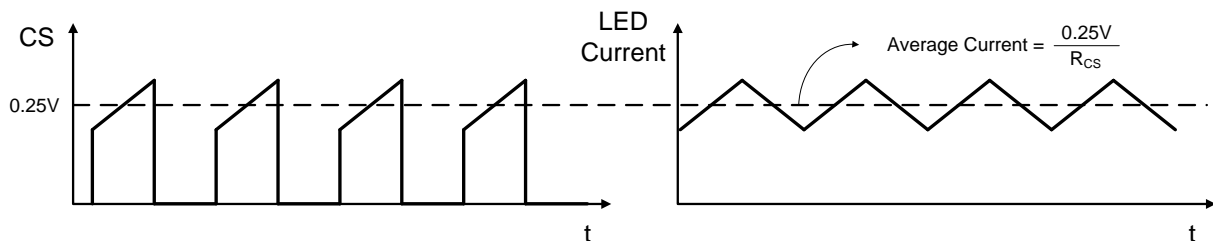
Average Current Control

The LED current is detected using a sense resistor at the CS pin. The feedback operates in a fast open-loop mode. No compensation is required. When the voltage at the DIM input $V_{DIM} \geq 1.5V$, output current is programmed simply as:

$$I_{LED}(A) = \frac{0.25V}{R_{CS}(\Omega)}$$

Otherwise:

$$I_{LED}(A) = \frac{V_{DIM}(V) \times 0.167}{R_{CS}(\Omega)}$$



The above equations are only valid for continuous conduction of the output inductor. It is a good practice to design the inductor such that the switching ripple current in it is 30% of its average peak-to-peak, full load, DC current. Hence, the recommended inductance can be calculated as:

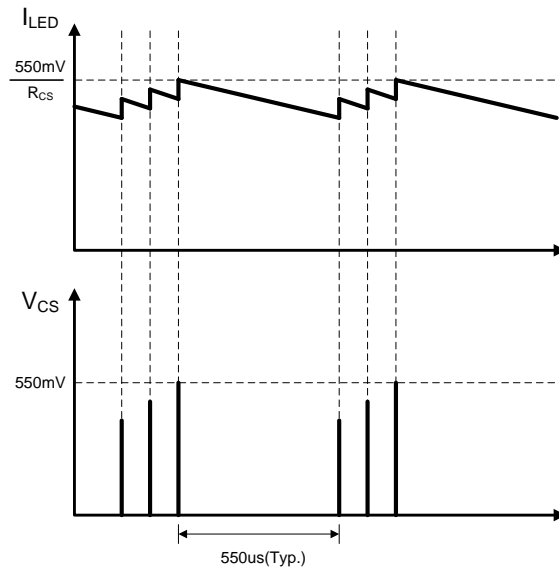
$$L = \frac{V_{LED(MAX)} \times T_{OFF}}{0.4 \times I_{LED}}$$

GATE Output

The GATE output of the FP7189 is used to drive an external MOSFET. It is recommended that the gate charge QG of the external MOSFET be less than 25nC for switching frequencies $\leq 100kHz$ and less than 15nC for switching frequencies $> 100kHz$.

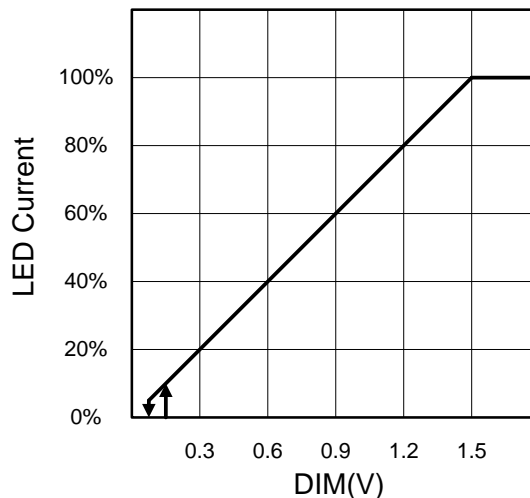
Output Short Circuit Protection

The short circuit protection comparator trips when the voltage at CS exceeds 0.55V. When this occurs, the GATE off-time $T_{HICCUP} = 550\mu s$ is generated to prevent stair-casing of the inductor current and potentially its saturation due to insufficient output voltage.



Linear Dimming

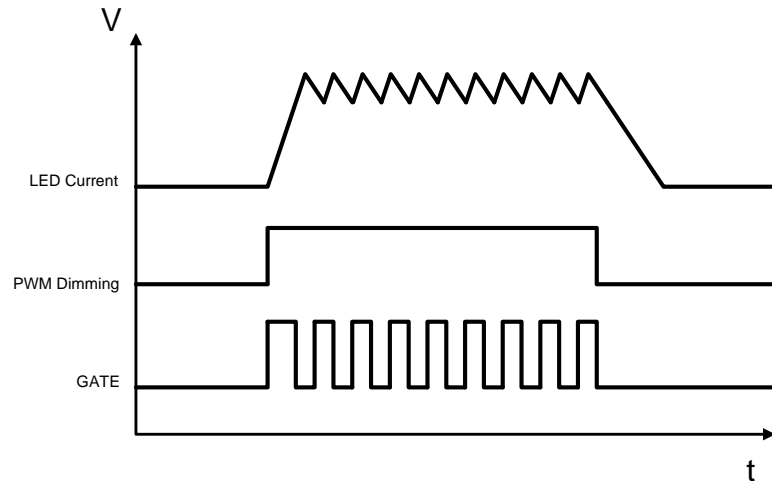
When the voltage at DIM falls below 1.5V, the internal 250mV reference to the constant-current feedback becomes overridden by $V_{DIM} \cdot 0.167$. As long as the current in the inductor remains continuous, the LED current is given by the equation above. However, when V_{DIM} falls below 200mV, the GATE output becomes disabled. The GATE signal recovers, when V_{DIM} exceeds 250mV. This is required in some applications to be able to shut the LED lamp off with the same signal input that controls the brightness.



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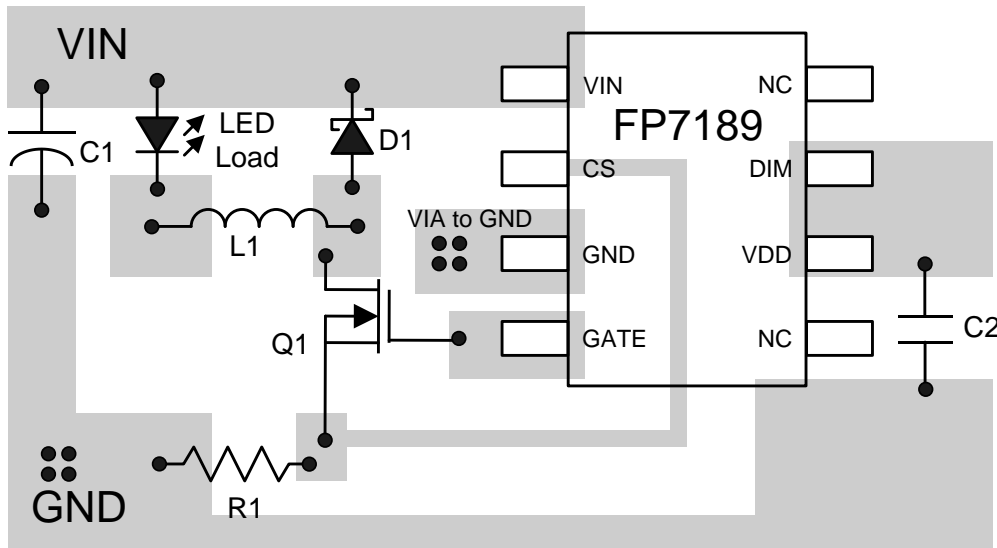
PWM Dimming

Due to the fast open-loop response of the average-current control loop of the FP7189, its PWM dimming performance nearly matches that of the FP7171.



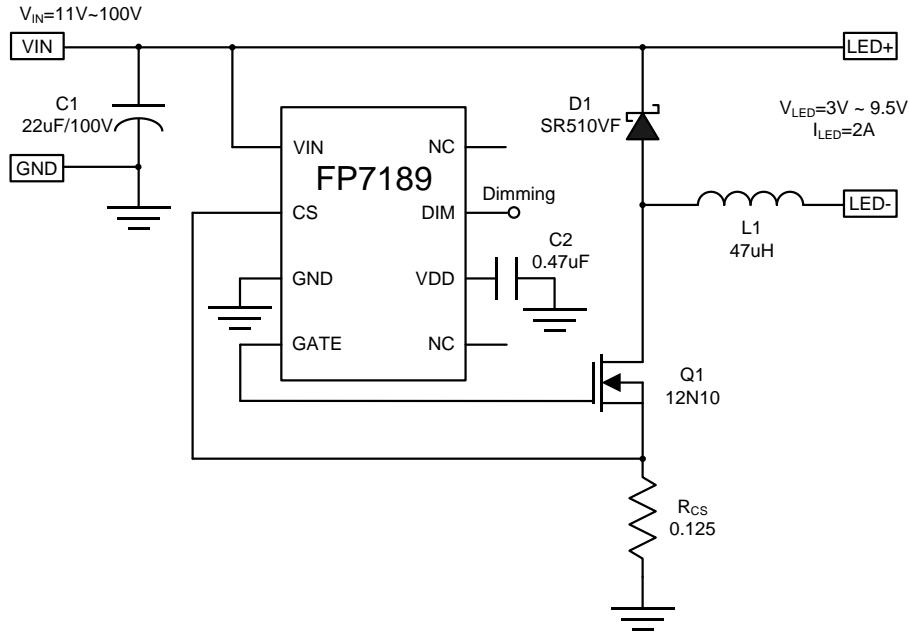
The rising and falling edges are limited by the current slew rate in the inductor. The first switching cycle is terminated upon reaching the 250mV ($V_{DIM} \cdot 0.167$) level at CS. The circuit is further reaching its steady-state within 1 switching cycles regardless of the switching frequency.

Suggested Layout



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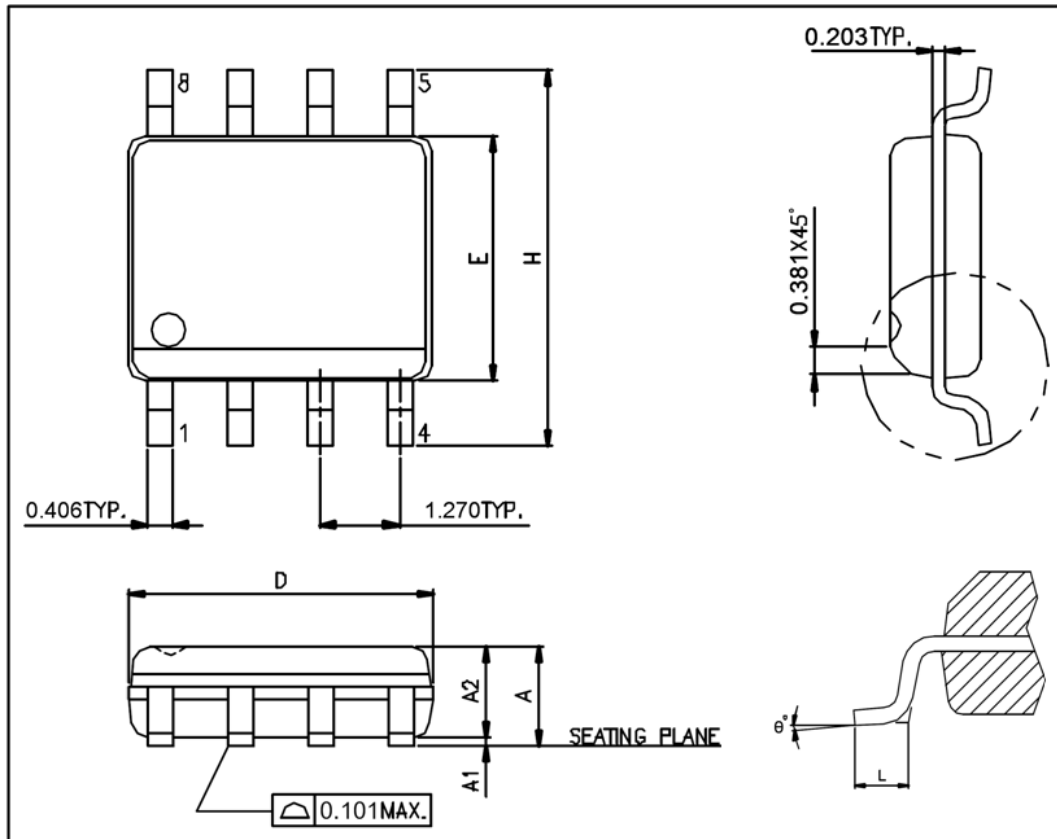
Typical Application Circuit



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Package Outline

SOP-8L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC Outline: MS-012 AA.
2. Dimension "D" does not include molding flash, protrusions or gate burrs.
3. Dimension "E" does not include inter-lead flash, or protrusions.

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