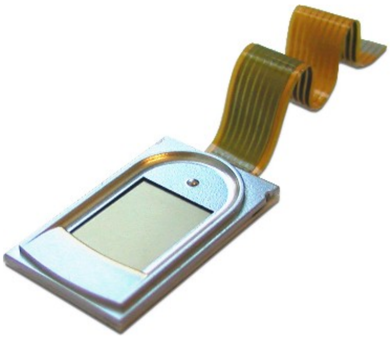
FPC1011C Area Sensor Package

Product Specification

Features

- Fingerprint area sensor
- Internal A/D
- High speed SPI interface
- Reduced readout time
- 3.3 and 2.5 volt operation
- Improved image quality
- Robust surface coating
- >15kV ESD protection
- >1 million wear cycles
- RoHS compliant



Application examples

- Physical access control
- Time and attendance
- Security application

General description

FPC1011C is a new leading-edge capacitive fingerprint sensor, based on the Certus Sensor Platform.

The Certus Sensor Platform offers several strong advantages; acknowledged high image quality, 256 gray scale values in every single pixel and especially, the reflective capacitive measurement method enables the use of a thick protective surface coating, preventing the user from directly touching the CMOS circuitry.

Thanks to the unique coating, FPC1011C is protected against ESD well above 15 kV and the everyday wear-and-tear. FPC1011C also includes a micro-ergonomic guidance, simplifying proper fingerprint alignment and hence improving algorithm performance.

FPC1011C is interfaced through a flexible printed circuit (8-pin) and therefore easy to integrate into a system using standard low-cost connectors.

Quick reference data

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Digital supply voltage		2.35	2.5/3.3	3.45	V
I_{DD}	Supply current total	V_{DD} = 2.5 V @ 4MHz V_{DD} = 2.5 V @ 32MHz V_{DD} = 3.3 V @ 4MHz V_{DD} = 3.3 V @ 32MHz		7 9 7 12	14 -- 14 --	mA
	Operating temperature	Normal operation	- 20		+ 60	°C
	Storage temperature		- 40		+ 85	°C
	Active sensing area		10.64 x 14.00			mm
	Image size		152 x 200			pixel
	Spatial resolution		363			dpi
	Pixel resolution		8			bit
L x W x T	Dimension	Sensor body	30.0 x 18.0 x 3.4			mm
		Flexible printed circuit	66.5 x 8.9 x 0.15			mm

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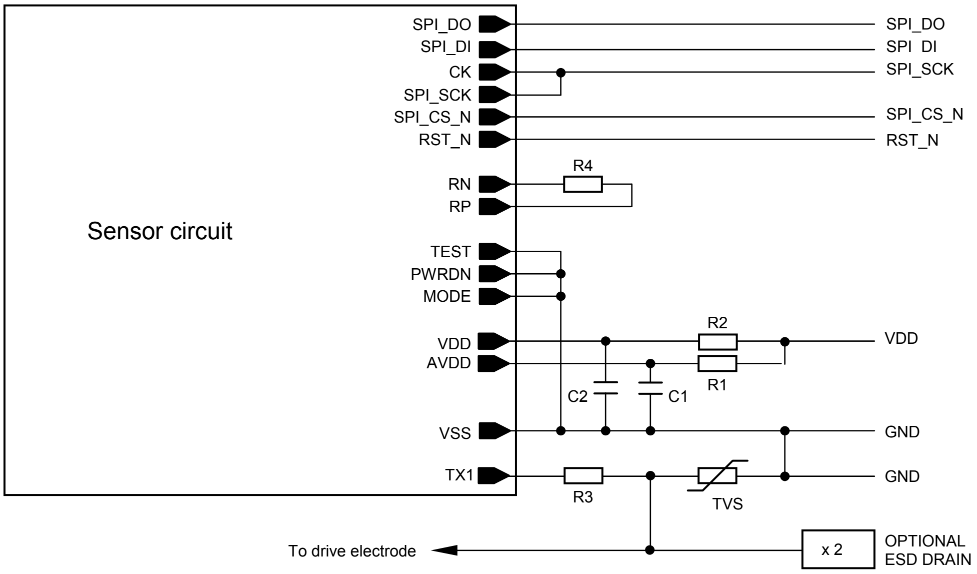
Functional description

Block diagram



Electrical properties

Absolute maximum ratings

Operating temperature	-20°C to +85°C
Storage temperature	-40°C to +85°C
Supply voltage	-0.5 V to +7.0 V
Input voltage	-0.5 V to V_{DD} + 0.5 V
Output voltage	-0.5 V to V_{DD} + 0.5 V
Total power dissipation	50 mW
ESD on IO's	±2 kV

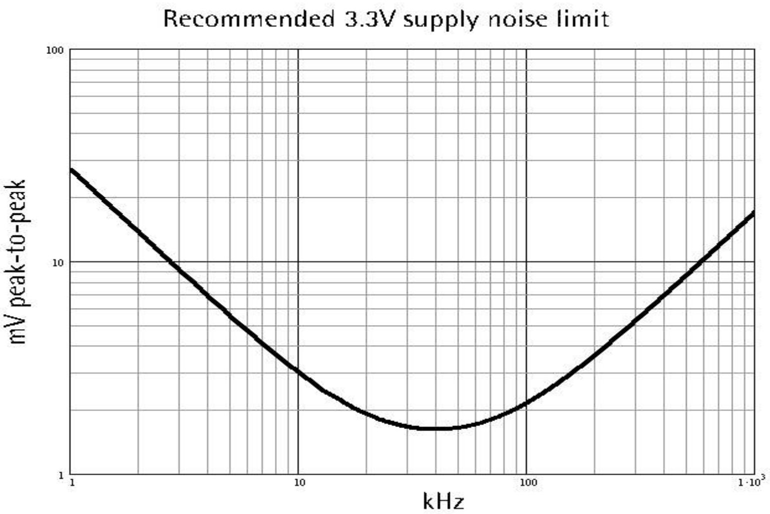
Note:
Stress beyond values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated as normal operation this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical characteristics

Measured at room temperature (RT)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		2.35	2.5/3.3	3.45	V
I_{DD}	Supply current, total	V_{DD} = 2.5V@4MHz	-	11	16	mA
		V_{DD} = 3.3V@4MHz	-	13	18	mA
Digital inputs						
V_{IL}	Logic '0' voltage		-	-	$0.2V_{DD}$	V
V_{IH}	Logic '1' voltage		$0.8V_{DD}$	-	-	V
I_{IL}	Logic '0' current (V_I = GND)		-	-	±10	µA
I_{IH}	Logic '1' current (V_I = V_{DD})		-	-	±10	µA
C_{IND}	Input capacitance		-	6	-	pF
Digital outputs						
V_{OL}	Logic '0' output voltage		-	0.2	0.4	V
V_{OH}	Logic '1' output voltage		$0.85V_{DD}$	$0.90V_{DD}$	-	V

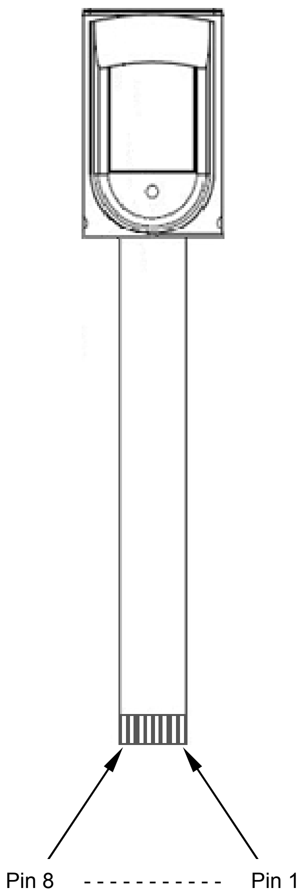
Differential power supply disturbance



Graph shows the supply disturbance level (sinus rms), which will give less than one grey level rms disturbance in the fingerprint readout. If the supply voltage is noisy, additional filtering may be required.

Pin configuration

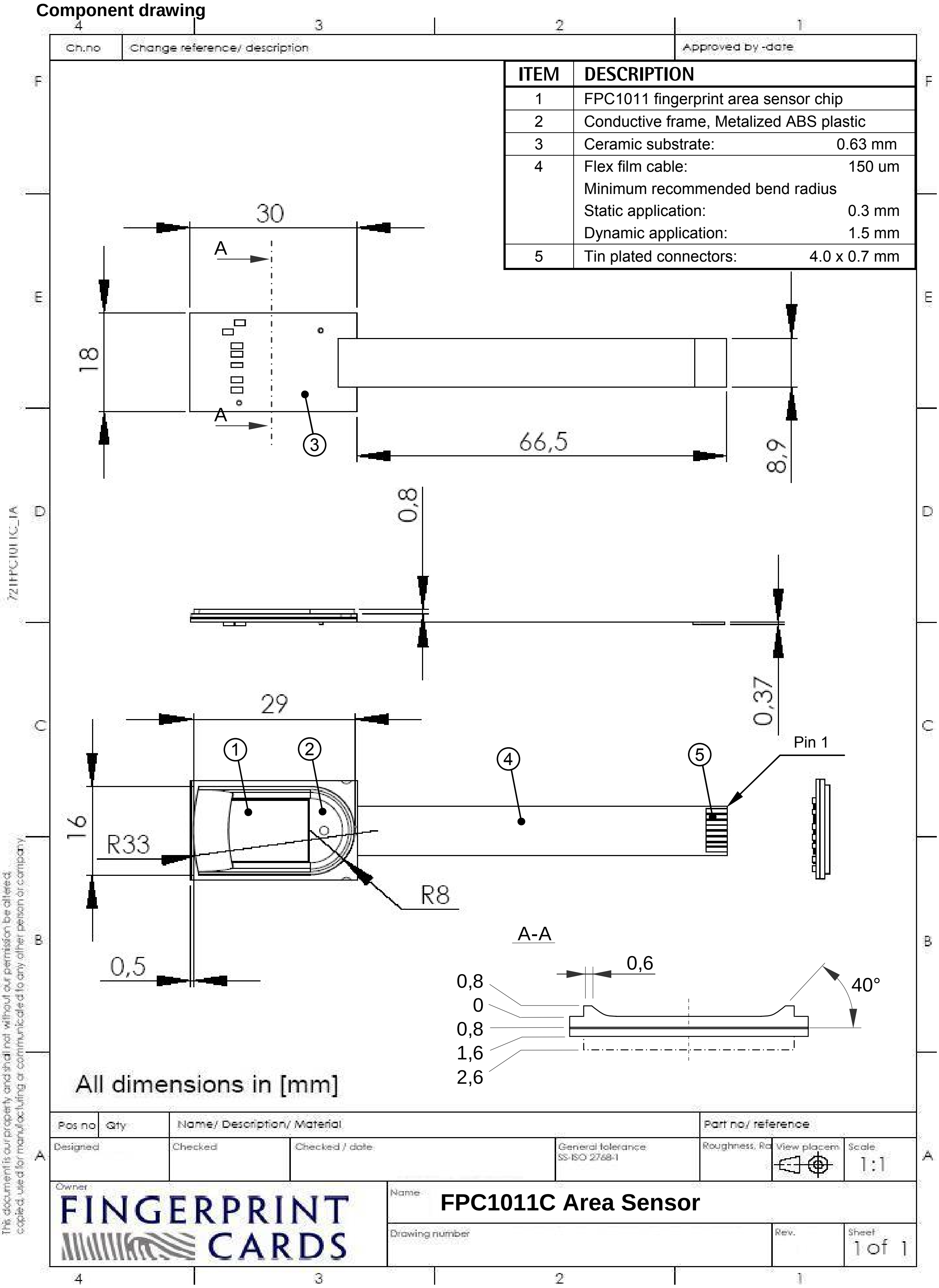
PIN	SIGNAL NAME	DESCRIPTION
1	SPI_DO	SPI data output. Tri state when SPI_CS_N is high.
2	VDD	Power supply, 2.5 or 3.3 V
3	RST_N	Reset, active low.
4	SPI_SCK	SPI clock input. Internal pull down.
5	GND	Signal ground
6	SPI_DI	SPI data input
7	SPI_CS_N	Chip select, active low. Resets the SPI interface when high.
8	GND	Signal ground



Mechanical properties

Component drawing

ITEM	DESCRIPTION	
1	FPC1011 fingerprint area sensor chip	
2	Conductive frame, Metalized ABS plastic	
3	Ceramic substrate:	0.63 mm
4	Flex film cable:	150 um
	Minimum recommended bend radius	
	Static application:	0.3 mm
	Dynamic application:	1.5 mm
5	Tin plated connectors:	4.0 x 0.7 mm



FPC1011C package drawing - Product outline. Drawing is not to scale.

Operation

Introduction
The FPC1011C sensor component is suitable for numerous types of authentication systems. Systems may be based on highly integrated low power solutions utilizing Fingerprint Cards (*Fingerprints*) companion chip, a large variety of standard micro-controllers or a high performance DSP.

In normal cases when the sensor is used together with a companion chip from *Fingerprints*, no detailed knowledge about the sensor circuit/matrix is required in order to operate the sensor component properly. However, if the sensor component is used together with e.g. a standard micro-controller or a DSP, a detailed understanding of the sensor operation is necessary.

Interface
The FPC1011C sensor package is built around a versatile CMOS circuit, based on *Fingerprints* Certus Sensor Platform. The CMOS circuit offers both a serial SPI interface and parallel asynchronus interface. The FPC1011C is operated with serial SPI interface.

Overview
The sensor component uses an architecture where the individual sensor elements sense a charge from the finger. A general block diagram for the sensor circuit is shown in the Figure 1.

The TX1-signal is used to supply a drive signal to the finger. Hence this signal is connected to an electrode (metalized frame) directly surrounding the sensor area. This electrode is also part of the ESD protection.

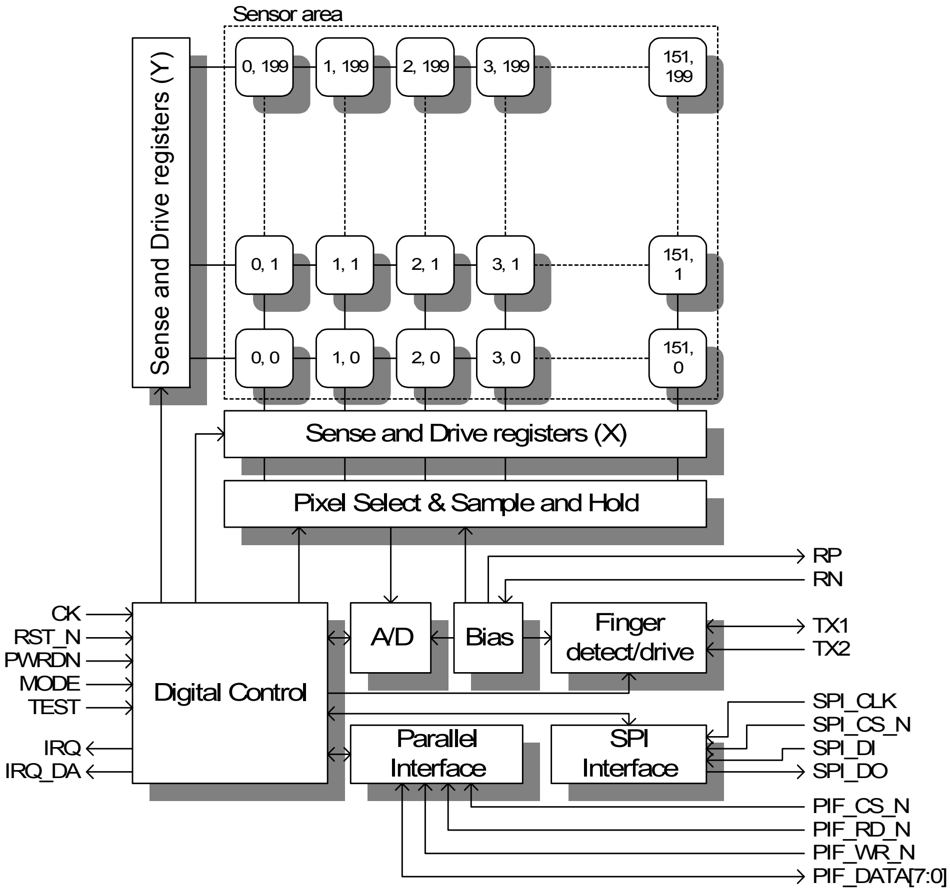


Figure 1
Block diagram - Sensor circuit

Interface

The sensor component contains a Serial Peripheral Interface (SPI).

The SPI interface enables high-speed readout of data with a minimum of wires. The SPI interface supports a speed of up to the current system clock speed. This feature makes the sensor usable for a wide range of control units. The SPI interface is a slave interface with CPHA = '0' and CPOL = '0'.

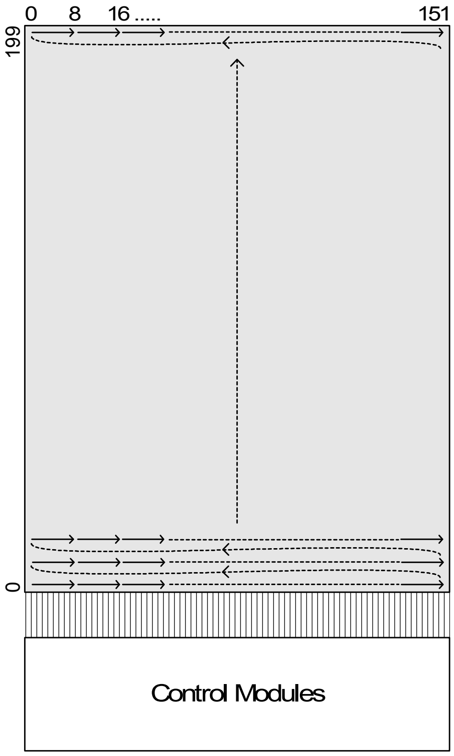
Through the communication interface, pixel data from the sensor circuit is entered into a FIFO, which in turn is read by applying read instructions.

The maximum readout speed in serial mode is 4 Mpixel/sec.

Sensor readout

The sensor matrix consists of 152 x 200 sensor elements. The entire sensor, or a part of it, is read by applying a read sensor instruction. The size of the active area is set by the values of the XSHIFT and YSHIFT registers.

The default values for these registers select the complete sensor area to be read once. The readout sequence is illustrated in the figure below.

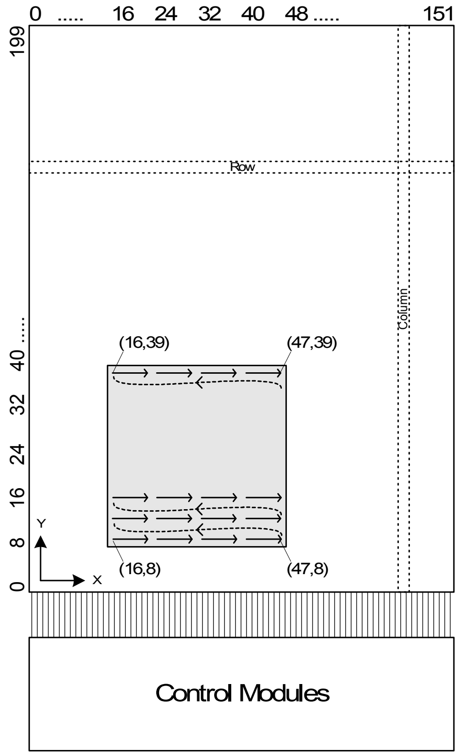


During all read operations, 8 pixels are captured simultaneously. By default the first 8 pixels being read are pixel (0,0) to (7,0), followed by pixels (8,0) to (15,0).

The readout area can be reduced by setting the XSHIFT and YSHIFT registers.

The sense area (a row of 8 pixels) is shifted in the x-direction XSHIFT times before it is shifted in the y-direction. The default start position can be changed by manually loading the SENSEX and SENSEY registers.

By setting XSENSE and YSENSE to start with pixels (16,8) to (23,8) and setting XSHIFT to 3 and YSHIFT to 31 the rectangle defined by the pixels (16,8) and (47,39) will be read, giving a total of 1024 pixels. Partial readout is illustrated in the figure below.



It is possible to read one row of pixels several times before shifting to the next row. This is done by setting the XREADS register.

The number of pixels being read is given by the following formula:

$$\#pixels = 8 \cdot (XSHIFT+1) \cdot (YSHIFT+1)$$

Figure 10 shows the read sequence in detail.

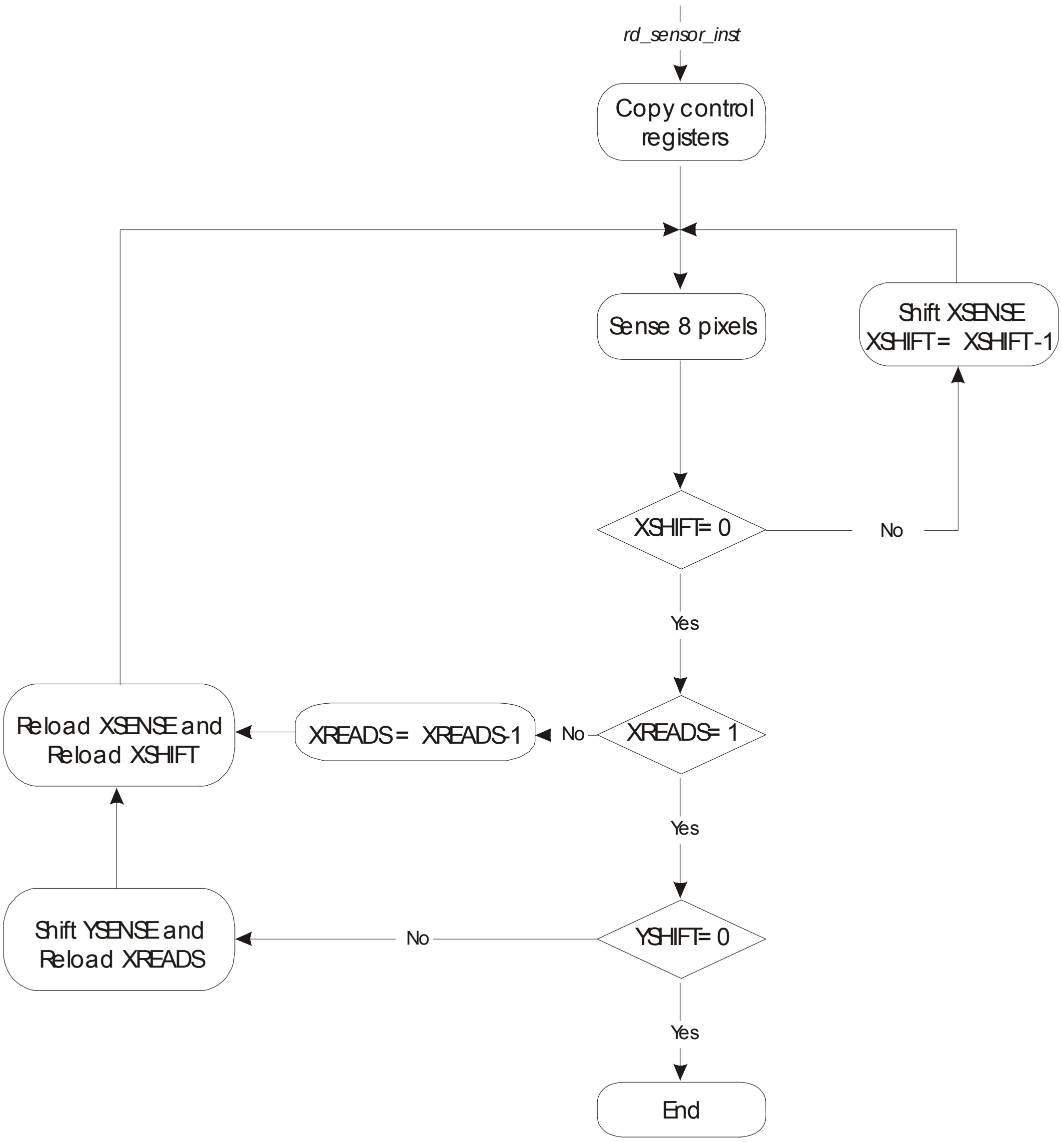


Figure 2
Internal sensor read out sequence

Serial mode

In serial mode all communication is done through the serial SPI interface. The available commands are described in this section.

Instruction summary

INSTRUCTION	INSTRUCTION CODE	DESCRIPTION
rd_sensor	11_H	Start sensing of finger. (Data is placed in the FIFO.)
rd_spidata	20_H	Read from FIFO (only applicable when the SPI interface is used.)
rd_spistat	21_H	Read internal status registers in the SPI interface (only applicable when the SPI interface is used.)
rd_regs	50_H	Read internal registers. (All registers are read in one operation. The register contents is placed in the FIFO.)
wr_drivc	75_H	Write DRIVC register. Set finger drive amplitude.
wr_adcref	76_H	Write ADCREF register. Set ADC sensitivity.
wr_sensem	77_H	Write SENSEMODE register. Set self-test mode.
wr_fifo_th	$7C_H$	Write FIFO_TH register. Set the FIFO fill threshold for activation of the data available signal (DA bit in the SPI_STAT register).
wr_xsense	$7F_H$	Shift data into the XSENSE register.
wr_ysense	81_H	Shift data into the YSENSE register.
wr_xshift	82_H	Write XSHIFT register. Set number of shifts to be performed in the x-direction.
wr_yshift	83_H	Write YSHIFT register. Set number of shifts to be performed in the y-direction.
wr_xreads	84_H	Write XREADS register. Set number of times the same row should be read before shifting the YSENSE register.

Serial mode instructions
Below all instructions are described in detail. Relevant timing diagrams are showed in the section *Timing properties*.

In addition to the long shift-registers controlling the pixels in the sensor array, the sensor component contains one SPI status register and 13 control registers. Instructions writing to a register all operate in the same way. The FIFO-pointers are reset when any instruction except <rd_spidata> and <rd_spistat> is applied.

Read sensor instruction

INSTRUCTION	rd_sensor (11_H)
Mode	serial
Input parameters	1 dummy byte
Data delay*	$(363\pm2)t_{CLK}$
Returned bytes	0

**Data delay is the delay from the instruction is given until data is available in the FIFO.*

This instruction is used to read the entire sensor or a part of it. Timing for reading in serial mode is defined in the section *Timing properties*.

The read sensor instruction is only used to start the sense-sequence, and the instruction itself does not return any data. The first data from the sensor array will enter the FIFO after approximately 363 clock-cycles. After that, a new byte will enter the FIFO every 8th clock-cycle until the area defined by the XSENSE, YSENSE, XSHIFT and YSHIFT registers has been read.

When the FIFO is filled to a level equal to or greater than the value set by the FIFO_TH register, the SPI_STAT register will indicate that data is ready for fetching.

If the FIFO is filled up with data, overflow is avoided by stalling sensing until data is read from the FIFO. During this stall-period all analog modules are active, and the ASIC will draw current as during a regular sense operation.

Read SPI data instruction

INSTRUCTION	rd_spidata (20_H)
Mode	serial
Input parameters	1 dummy byte
Data delay	0
Returned bytes	n

After the read SPI data instruction is sent, <rd_spidata>, pixel data will be returned as shown in Figure 11. Data will continue to be returned as long as SPI_CS_N and SPI_DI are kept low.

SPI_DI should be kept low after the <rd_spidata>, instruction is entered to avoid the subsequent byte to be interpreted as a new instruction.

The reading of data can be stopped at any time without data-loss by setting SPI_CS_N high, as long as SPI_CS_N is set high between the last bit of the current byte being read and the first bit in the next byte.

If SPI_CS_N is released at any other time (e.g. during a byte transfer) one or more bytes will be lost. To continue readout after a stop caused by setting SPI_CS_N high, the <rd_spidata> instruction has to be applied again.

Read SPI status instruction

INSTRUCTION	rd_spistat (21_H)
Mode	serial
Input parameters	1 dummy byte
Data delay	0
Returned bytes	1

The SPI status register holds status information for the SPI interface. When the read SPI status instruction is applied, the content of the SPI_STAT register is returned. Applying this instruction does not interrupt sensor readout if sensor readout is in progress.

REGISTER			SPI_STAT				
Size (active bits)			3				
7	6	5	4	3	2	1	0
-	-	-	-	-	UFL	STL	DA
Reset			00_H (default value)				
001			Data available in FIFO.				
010			Stall. Bit is set if sensing is stalled due to a full FIFO.				
100			Underflow. Bit is set if underflow occurs.				

Read registers instruction

INSTRUCTION	rd_regs (50_H)
Mode	serial
Input parameters	1 dummy byte
Data delay	0
Returned bytes	13 bytes

The read register instruction fills the FIFO with the value of all the internal control registers. The order in which the registers are entered into the FIFO is given in table below.

This instruction does not return any pixel data. Data has to be read with the <rd_spidata> instruction The read SPI data instruction can directly follow this instruction for readout of register data.

RETURN ORDER	REGISTER
1	STATUS
2	NOT USED
3	DRIVC
4	ADCREF
5	SENSEMODE
6	FIFO_TH
7	NOT USED
8	XSHIFT
9	YSHIFT
10	XREADS
11	NOT USED
12	NOT USED
13	NOT USED
14	00_H
15	00_H
16	00_H

Return order for register values

The STATUS register is a read only register, which holds the status information for the FIFO.

REGISTER			STATUS				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	STL	UFL
Reset			00_H (default value)				
01			Underflow. Bit is set if underflow occurs.				
10			Stall. Bit is set if sensing is stalled due to a full FIFO.				

Remaining control registers (3-10) can be operated with both read and write instructions. Details on these registers are available together with the write instructions for each register.

All flag generation is based on comparing write-pointer with read pointer synchronized to SPI clock. This means that if a read instruction, resulting in an underflow, occurs one clock period before new data enters the FIFO, an undetected underflow will occur. To avoid this, the procedure for reading from the FIFO, which is outlined in FIFO_TH register description, should be followed.

The entire register is reset when a <rd_regs> instruction is executed.

Write to DRIVC register

INSTRUCTION	wr_drivc (75_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The DRIVC register sets the amplitude for the frame drive. Please note that two different versions of the sensor die are present. The recommended DRIVC setting for each type is listed in the *Sensor setup* section. With default value set, the frame drive is disabled.

REGISTER			DRIVC				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			00_H (default value)				
0_D			Min voltage, Frame drive off				
127_D			Approximately $V_{DD}/2$				
128_D - 255_D			Max voltage, approx V_{DD}				

Write to SENSEMODE register

INSTRUCTION	wr_sensem (77_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The SENSEMODE register is a 2-bit register, which sets the test mode. In normal operation, this register should be cleared.

REGISTER			SENSEMODE				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	x	x
Reset			00_H (default value)				
00			White test pattern (normal)				
01			Checker board test				
10			Inverted checker board test				
11			Black test				

Write to ADCREF register

INSTRUCTION	wr_adcref (76_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The ADCREF register sets the dynamic range for the internal A/D converter. This register is set to '11' at reset. Please note that two different versions of the sensor die are present. The recommended ADCREF setting for each type is listed in the *Sensor setup* section.

REGISTER			ADCREF				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	x	x
Reset			00_H (default value)				
00			0.125 x V_{DD}				
01			0.250 x V_{DD}				
10			0.375 x V_{DD}				
11			0.500 x V_{DD}				

Write to FIFO_TH register

INSTRUCTION	wr_fifo_th ($7C_H$)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The FIFO_TH register holds the threshold value for the FIFO. When the fill level for the FIFO is higher than or equal to this value, the DA bit in the SPI_STAT register is set.

The internal sensor data FIFO is 16 bytes deep and the threshold level can be set between 1 and 16. If this register is set to 00_H the DA bit will be set to indicate when all 16 bytes are holding valid data. The relation between the register value and the threshold level is shown below.

REGISTER			FIFO_TH				
Size (active bits)			4				
7	6	5	4	3	2	1	0
-	-	-	-	x	x	x	x
Reset			08_H (default value)				
0000			Threshold level 16				
0001			Threshold level 1				
0010			Threshold level 2				
:			:				
1111			Threshold level 15				

Write to XSENSE/YSENSE register

INSTRUCTION	wr_xsense ($7F_H$)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

INSTRUCTION	wr_ysense (81_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

These registers are used to select which pixels are active during sensing.

The values of these registers can be changed using the <wr_xsense> and <wr_ysense> instructions. When any of these instructions are applied, the XSENSE and YSENSE register, respectively, are shifted 8 bits towards the MSB and the 8 LSB's are replaced with the new byte. The sensor circuit contains 8 sample-and-hold modules. Column n·8+m, where n={0..18} and m={0..7}, are connected to the sample-and-hold module number m, through pass gates.

These pass gates are controlled by the XSENSE register. It is important not to let two pixels drive the same sample-and-hold module when loading a non-default value to these registers.

It is important that only one row is active at a time. The YSENSE register controls which row is active. Please make sure that only one bit in the YSENSE register is set to '1' at any time. If more that one bit in the YSENSE register is set to '1', the returned picture will be invalid, and current-consumption will increase.

To activate a pixel (sensing), the associated bits in both the XSENSE and the YSENSE registers have to be set.

During the fingerprint sensing period, the 8 sample-and-hold modules sample data simultaneously. This data is then digitized before a new sample-and-hold operation is performed. Data is always returned starting with sample-and-hold number 0 and ending with sample-and-hold number 7.

This means that if XSENSE is set to start sensing column 3 to 10 (instead of 0 to 7 which is default) and the shift mode is set to shift 8 positions, the pixels will be read out in the following order (by column number): 8, 9, 10, 3, 4, 5, 6, 7, 16, 17, 18, 11, 12, 13, 14, 15 and so on. This is illustrated in table 1.

REGISTER	XSENSE
Size (bit/bytes)	152 / 19
Reset	00 ... $00FF_H$ (default value)

REGISTER	YSENSE
Size (bit/bytes)	200 / 25
Reset	00 ... 0001_H (default value)

XSENSE START VALUE	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
COLUMN NO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CONNECTED TO SH NO	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
SAMPLE CYCLE NO				1								2								3				

Table 1
Illustration of readout sequence with a non-standard start value for XSENSE.

Write to XSHIFT register

INSTRUCTION	wr_xshift (82_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The XSHIFT register holds the number of shifts performed in the x direction. The number of sense operations performed in one row exceeds the value stored in this register by one.

REGISTER			XSHIFT				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			12_H (18_D) (default value)				

Write to XREADS register

INSTRUCTION	wr_xreads (84_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The XREADS register holds the number of times the same row is read before shifting to the next.

REGISTER			XREADS				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			01_H (default value)				

Write to YSHIFT register

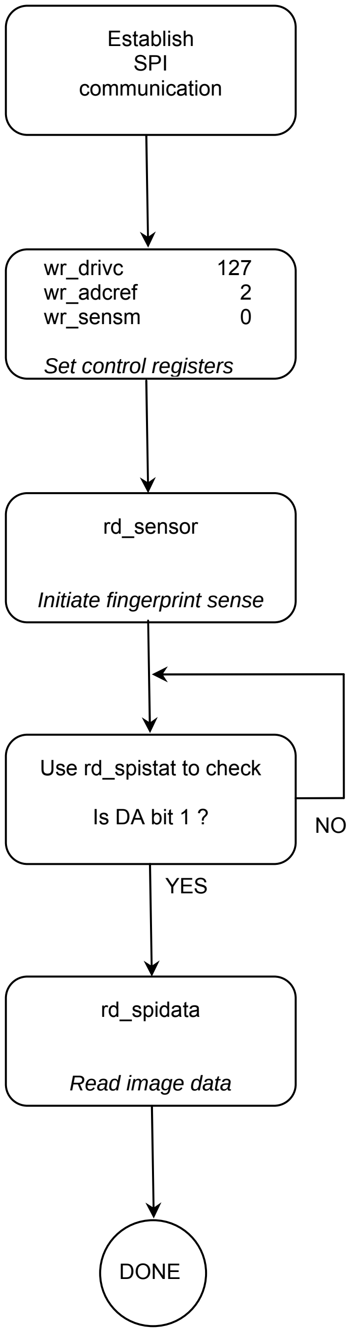
INSTRUCTION	wr_yshift (83_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The YSHIFT register holds the number of shifts performed in the y-direction. The number of lines sensed exceeds the value stored in this register by one.

REGISTER			YSHIFT				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			$C7_H$ (199_D) (default value)				

Sample Implementation

This section describes step-by-step how the SPI interface of FPC1011C can be used to perform a basic image readout process. We will outline in detail which commands the SPI host needs to transmit to receive the full sensor image.



a) Establish a SPI connection between the SPI host and slave, using CPHA='0' and CPOL='0', at any clock speed <32MHz, and big endian bit order. Also, let the host enable the Chip Select signal in the SPI interface.

b) Send the three instructions <wr_drivc>, <wr_adcref>, and <wr_sensemode> with corresponding parameter values 127, 2, and 0 (depending on product revision), to set the readout parameters of the sensor to their recommended values.

Please note that different register settings apply depending on product revision. Detailed descriptions of corresponding settings are listed in section *Sensor setup*.

TYPE	DRIVC	ADCREF	SENSEMODE
"Old"	255	1	0
"New"	127	2	0

c) Tell the sensor to capture an image by sending the instruction <rd_sensor>, with a dummy parameter value.

d) Next, we have to (in some way) let the SPI clock run for 363±2 cycles, before we can start reading actual image data. One way to achieve this without actually counting cycles is to repeatedly read bit 0 in the SPI_STATUS register, use the <rd_spistat> instruction. When the DA bit (data available bit) is 1, the sensor image is ready for readout.

e) Now, use the <rd_spidata> instruction to read 30400 bytes of pixel data. The read pixel data is delivered row by row, with 1 byte per pixel, forming an image with dimensions 152 columns times 200 rows.

f) Finally, let the host disable the Chip Select Signal, and (if applicable) shut down the connection to FPC1011C.

Sensor setup
If the FPC1011C sensor is **NOT** used together with *Fingerprints* companion chip, but instead with a standard micro-controller, a DSP or similar, an easy register setup is necessary.

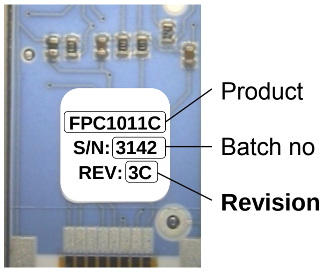
There are three types/versions of the sensors component available on the market. They are clearly distinguished with different labels on the sensor backside.

Please note that all sensor versions **are entirely compatible**. There are no differences in "form, fit or function". One type can replace another.

However different register settings are necessary. The appropriate parameters are indicated in tables below.

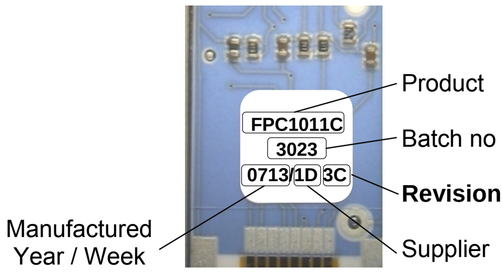
For detailed instructions on how to perform the actual register setup, please refer to the *Serial mode instructions* section in this document.

Type 1 - Marked with batch no (S/N):



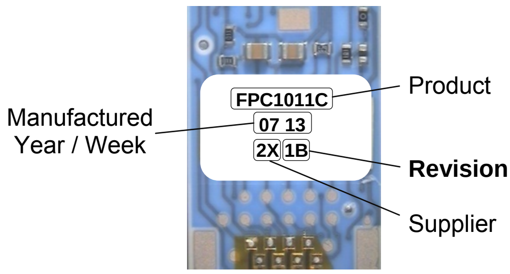
PRODUCT	REV	DRIVC	ADCREF
FPC1011C	1A, 2A, 2B, 2C, 2D, 2E	255	1
FPC1011C	2F, 3A, 3B, 3C	127	2

Type 2 - Marked with date and supplier (1D):



PRODUCT	REV	DRIVC	ADCREF
FPC1011C	3C, 3D, 3E, 3F	127	2

Type 3 - Marked with date and supplier (2X):



PRODUCT	REV	DRIVC	ADCREF
FPC1011C	1A, 1B	127	2

Timing properties

General timing

SYMBOL	PARAMETER (CONDITION)	NOTE	MIN	TYP	MAX	UNIT
f_{CK}	Clock frequency	1	2.5	-	32	MHz
t_{RSTPD}	Time from RST_N low to PWRDN low	1	30	-	-	ns
t_{RST}	Reset time	1	30*	-	-	ns
t_{PDS}	PWRDN setup time. Start-up time for ASIC.	2	10	-	-	µs
t_{PDH}	PWRDN hold time.	2	0	-	-	ns
t_{PDD}	PWRDN disable time. Shut-down time for ASIC.	2	15	-	-	ns
t_{RD}	Rise time for digital inputs	2		-	3	ns
t_{FD} P_{PDS}	Fall time for digital inputs PWRDN setup energy	2 1		6	3	ns nJ

Note 1: Estimated value

Note 2: Simulated value

**Reset is guaranteed for this duration, but may occur for shorter pulses.*

Serial mode timing

SYMBOL	PARAMETER (CONDITION)	NOTE	MIN	TYP	MAX	UNIT
f_{SPI_CK}	Frequency for SPI clock.	1	0		f_{CK}	MHz
t_{SCKL}	Part of SPI_CK clock period, during which SPI_CK is low.	1	14			ns
t_{SCKH}	Part of SPI_CK clock period, during which SPI_CK is high.	1	14			ns
t_{CSCKF}	Time from falling edge on SPI_CK to edge on SPI_CS_N	1	4			ns
t_{CSCKR}	Time from edge on SPI_CS_N to rising edge on SPI_CK	1	4			ns
t_{DSU}	Setup time for data before rising edge of SPI_CK	1	5			ns
t_{DH}	Hold time for data after rising edge of SPI_CK	1	5			ns
t_{SCKD}	Delay from falling clock to data available.	1	0		8	ns
t_{SSU}	Delay from SPI_CS_N low to SPI_DI mode change.	1	0		5	ns

Note 1: Estimated value

Figure 3 shows the general timing for the SPI interface. The figure only shows input and output of 1 byte, but can be extended to more bytes by keeping SPI_CS_N low for more clock cycles. Dependencies between SPI_DI, SPI_DO and SPI_CK are only shown once, but apply to all clock cycles.

All instructions applied consist of one instruction byte and one data byte. This is illustrated in Figure 4 and Figure 5 for instructions without and with return parameters.

The first byte applied after the SPI_CS_N signal is set low, is interpreted as an instruction byte. After that every other byte is interpreted as a new instruction. This makes it possible to apply new instructions without releasing SPI_CS_N.

If no new instruction should be applied after the first, e.g. during data readout, the following bytes should all be zeroes. The first byte after an all-zero byte is always interpreted as an instruction-byte.

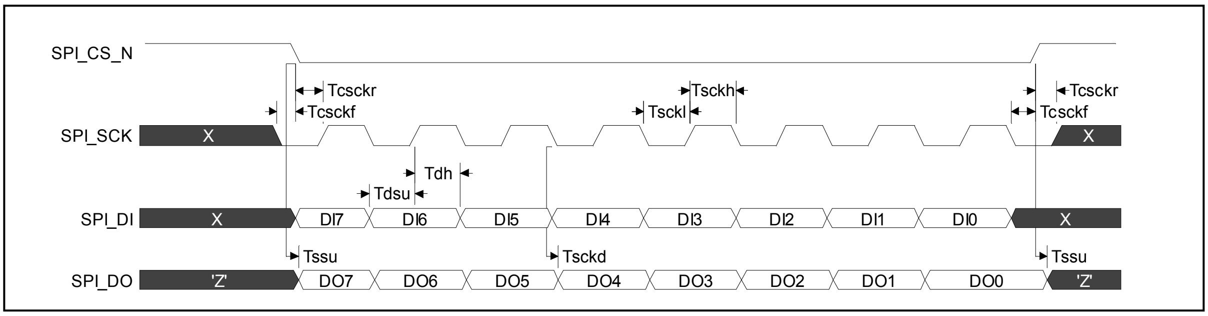


Figure 3
General SPI timing

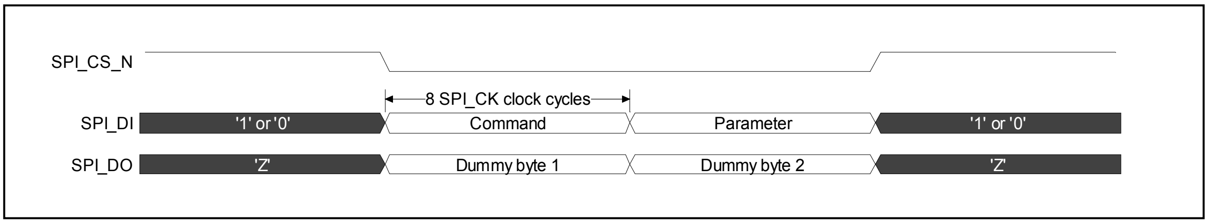


Figure 4
Applying an instruction without return data.

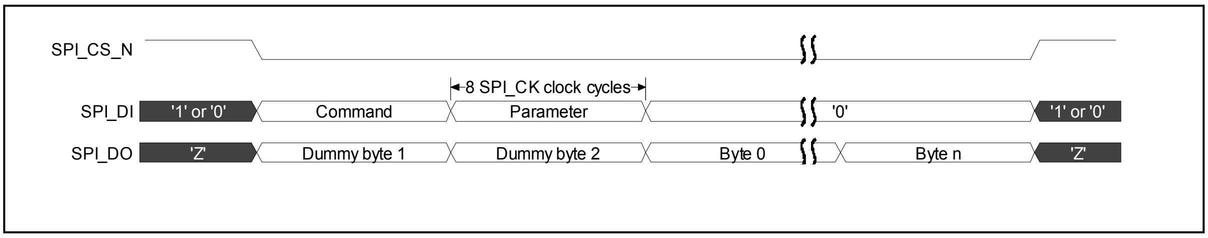


Figure 5
Applying an instruction with one or more return data.

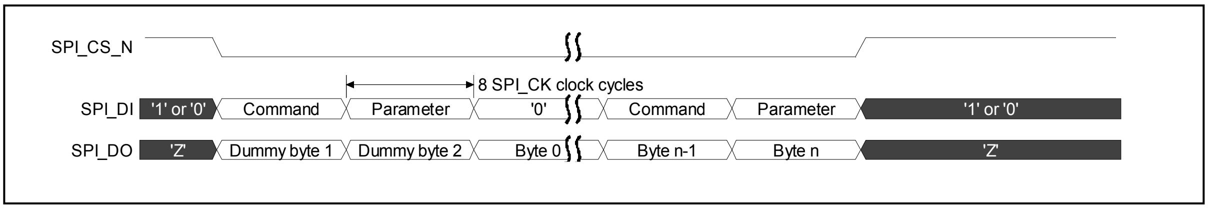


Figure 6
Terminating read by applying a new command.

Figure 6 shows the case where a new instruction stops the execution of the previous instruction.

The only difference between signals for the first and second instruction, is that during the first instruction SPI_DO holds dummy data during instruction and parameter entry, while SPI_DO continues to return data during the second instruction and parameter entry.

There are no restrictions on how many instruction can be entered during the same SPI_CS_N low period, or which instruction can be entered.

Environmental standards

PARAMETER	REFERENCE	CONDITION	MIN	MAX	UNIT
Solar radiation					
Outdoor exposure	IEC60068-2-5 Sa Procedure C			32	hours
Indoor exposure	IEC60068-2-5 Sa Procedure C	Filtered		56	hours
Temperature					
Cold operational	IEC60068-2-1 Ab	16h	-20		°C
Hot operational	IEC60068-2-1 Bb	16h		+85	°C
Cold storage	IEC60068-2-1 AB	16h	-40		°C
Temperature cycling	IEC60068-2-14 Na	30min/30min, 200 cycles	-40	+85	°C
Humid heat	IEC60068-2-67 Cy	85°C/85%RH		1000	hours

Table 2
Climate

SUBSTANCE	CONDITION	RESULT	COMMENT
Oil	200 cycles@6N	OK	
Petrol	200 cycles@6N	OK	Whitening of sensor surface. Normal performance.
Acetone	200 cycles@6N	OK	Whitening of sensor surface. Normal performance.
Artificial sweat	200 cycles@6N	OK	
Soap	200 cycles@6N	OK	
Ethanol	200 cycles@6N	OK	
Mosquito repellant	200 cycles@6N	OK	

Table 3
Fluids

PARAMETER	CONDITION	VALUE	UNIT
Pen drop height	Bic ball-point pen. Assembly weight 13 grams.	> 15	cm
Finger rubbing	Silicon finger. Rubbing force 6N.	> 1 000 000	cycles

Table 4
Abrasion

PARAMETER	REFERENCE	CONDITION	VALUE	UNIT
ESD	IEC61000-4-2	Air discharge	> ±15	kV

Table 5
Electro static discharge

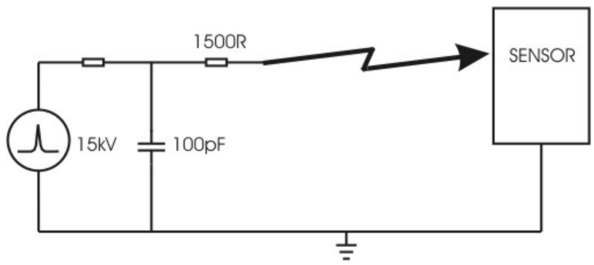
Application information

ESD immunity

The importance of ESD protection
Capacitive fingerprint sensors require a finger in contact with the sensor surface. This will expose all capacitive sensors to severe ESD discharges, as they usually are the "first point of contact". ESD discharge voltages are often under-estimated and the actual voltage levels may be surprisingly high. Discharges in the 1 to 2 kV range will typically not even be noticed, i.e. felt in the finger.

All FPC sensors incorporate extensive internal ESD protection for all accessible front surfaces. The protection level is well in excess of 15kV using a standard Human Body Model discharge.

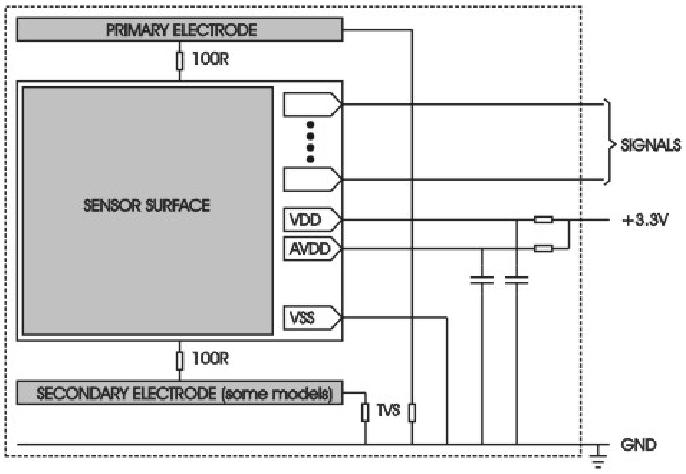
Human Body Model
The Human Body Model consists of a 100 pF capacitor, which simulates the capacitance between body and ground. This capacitor is charged to a test voltage. The resistance of the finger and skin is approximated by a 1500 ohm series resistor. The discharge will have a time constant of, 100pF x 1500 ohm = 150 nS. For a 15 kV discharge the peak current would be 15kV/1500 = 10A.



Although the ESD-specification is given as a voltage level it is important to realize that an ESD test is more of a current discharge test.

Internal sensor protection
ESD discharge issues are best illustrated by considering the simplified internal schematic in the figure below.

Sensors from FPC have a robust sensor surface coating, which will deflect discharges to the sensor frame. From the frame, the discharge current will be conducted via the Transient Voltage Suppressor (TVS) to the local sensor ground. The voltage at the frame is thereby limited. The 100 ohm resistor will limit the current towards the sensor chip to very safe levels.



Voltages induced by the ESD current
In a simplified model, two currents occur during an ESD event - the main ESD current flowing through the TVS to the sensor ground, and the much smaller current flowing through the 100 ohm resistor back into sensor chip input protection.

The current flow through the 100 ohm resistor will depend on the clamping voltage over the TVS. A 15kV discharge will generate a 200 mA current pulse into the chip protection diodes, well within the chip ESD rating. The duration of the pulse will be in the order of 600nS. After this time the current will decay exponentially.

The charge through the protection diode can be estimated to 0.15 nC.

Sensor cable extensions
When using longer sensor cable lengths, the electromagnetic coupling between the current in the ground connection and other signal and supply connections need to be considered.

This coupling is rather complicated and will depend on the cable geometry. With the standard, short connection between the sensor and the receiving electronics, these effects are not significant and can be ignored.

Longer cable lengths between sensor and the receiving electronics can in some cases be acceptable. Exact guidelines are not possible since the ESD effects will depend on the actual installation but up to 0.2 meter would in general not cause any problems.

Extensions will also affect signal fidelity and the digital waveforms need to be checked for adverse reflections. Problems with ringing become more evident as the length increases. At 1 m the ringing will cause waveforms that are questionable.

Minimizing effects on downstream electronics
The ESD pulse will continue past the sensor connection and spread into the receiving electronics ground plane and most likely further on to a "protective earth" ground via a connecting cable. This connection will often have considerable length and hence potential ESD problems.

To help alleviate the risk of electromagnetic coupling a separate ESD return to divert the ESD current to some "suitable" point is recommended. One way to prevent problems with stray currents due to the dual ground path, is to front the separate ESD return with a TVS in order to break this current path at low voltages while allowing the ESD pulse to pass freely.

Even higher ESD diversion can be achieved by also increasing the inductance of the signal cable connection from the receiving electronics. The common mode inductance forms a "barrier" to help steer the ESD current over to the separate ESD return. One of the easiest means is to mount an EMI ferrite core on the cable near the electronics.

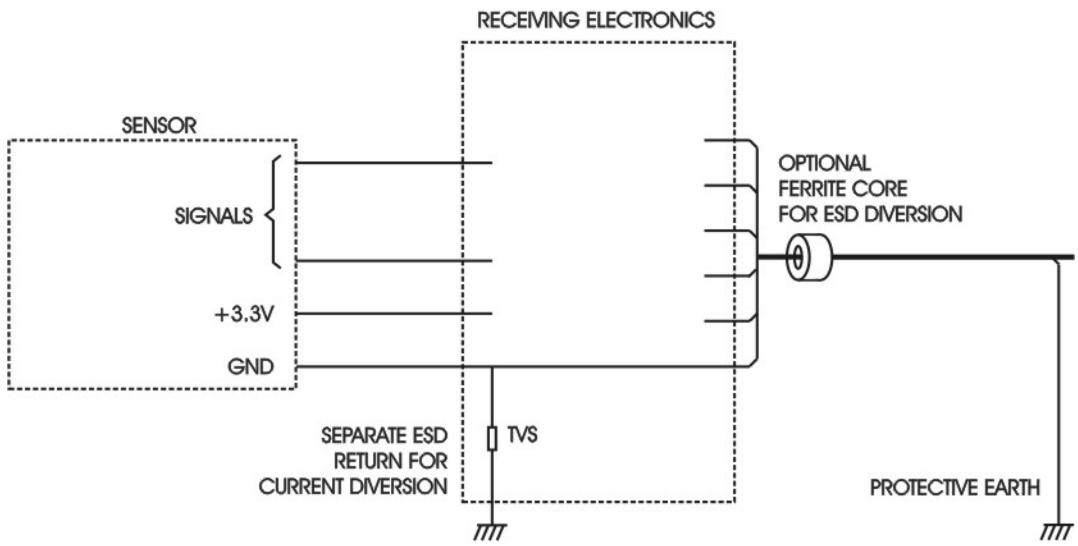
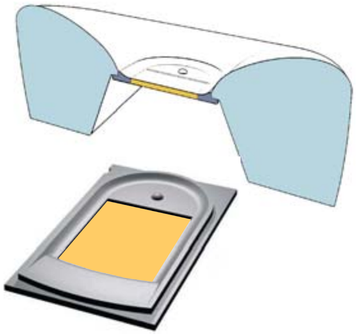


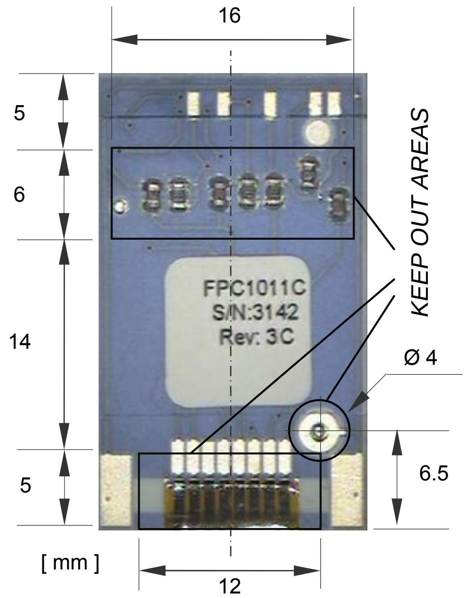
Figure 7
Recommended ESD precaution in application / External TVS
(e.g. Transguard VC060309A200, www.avx.com)

Sensor assembly
Thanks to the conductive frame containing Micro-ergonomics, a smooth transition to exterior mechanics can easily be obtained.



Note that the sensor and its conductive frame must be mounted in such way that electrical isolation to adjacent conductive surfaces is achieved. Otherwise the sensor operation may be degraded.

On the backside of the sensor substrate a number of passive components are placed. The overall maximum height is **1,0 mm**.



The best way to ensure a solid sensor mount is to apply a stable support to the back side of the sensor component. This can preferably be attached to the upper region (above passives) and in the centre area (label).

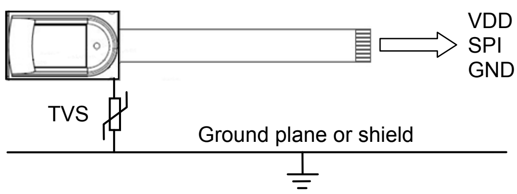
Mating connector
FPC1011C is fitted with a common flex film connector. Several mating connectors are possible, for example: Molex 52207-0890

Optional ESD drain
In normal cases a possible ESD discharge is diverted from the sensor component, through the signal ground wires (pin 5 and 8) in the flex, to the receiving electronics board. But for some applications, e.g. long connection between sensor component and ground plane, additional ESD drain paths may be desired (see section on *Sensor cable extensions*).

The FPC1011C sensor component is fitted with two extra ESD pads on the back side. Both pads are directly connected to the metalized frame.

Optional ESD drain pads

This makes it possible to divert an ESD current, via a secondary TSV component, directly to an adjacent ground plan or shield. If the clamping voltage is selected with care (< 67 volts), the secondary TVS will safely consume the major part of the discharge.



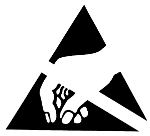
Pads are connected using clamps or similar. Soldering is not permitted since this will raise the sensor temperature outside *Maximum ratings* and most likely cause permanent damage to the sensor component.

Ordering information

Product number:	FPC1011C
Description:	Area sensor with C package
Minimum Order Quantity (MOQ):	200 sensor units

ESD sensitivity

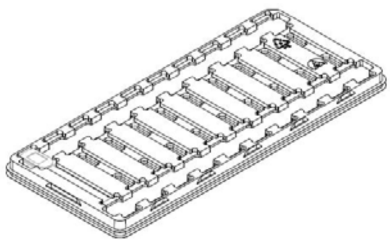
Electrostatically sensitive device. Ensure proper handling of the device during assembly.

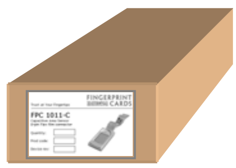


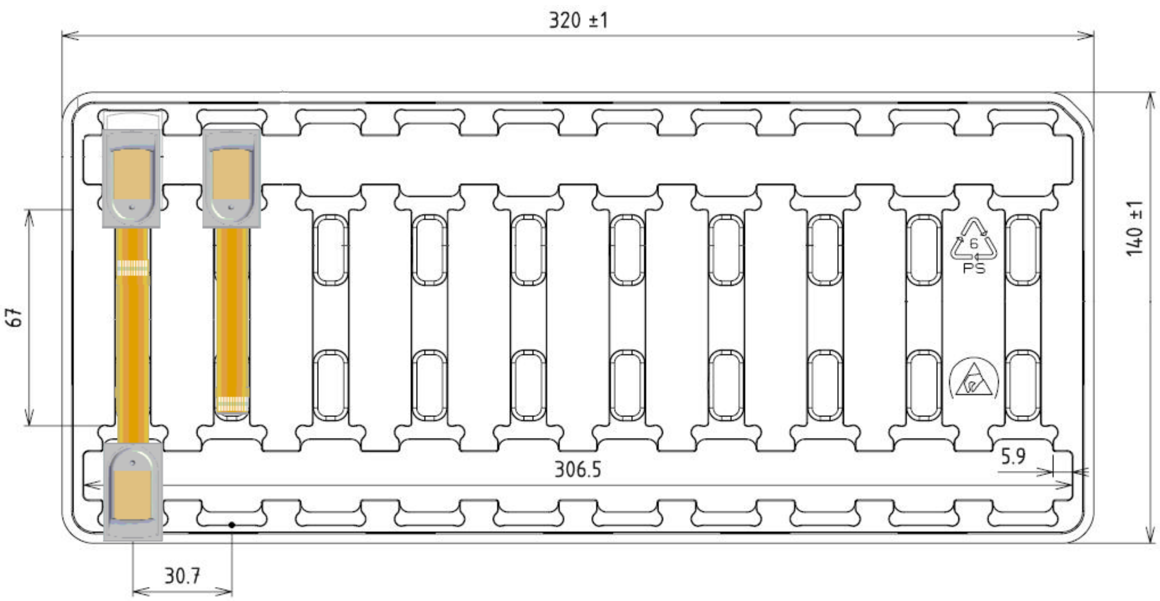
Package information

Products are supplied in ESD safe blister packs, 20 sensor units per tray. Every cardboard box contains eleven trays (one lid), which equals 200 units. Products are also sealed with an ESD safe bag. All cardboard boxes are marked with necessary product information; product no, quantity, date code and product revision.

Quantity:	200	- No of units inside box
Date code:	0729	- Production year (yy) and week (ww)
Version code:	1D3C	- Supplier code (nn) and revision (xx)







Document revision history

REVISION	DATE	CHANGE	AUTHOR	APPROVED
A	Mar 4, 2004	First release, internal document	DFR	PSV
B	Mar 18, 2004	New release, general updates	MSL	PSV
C	Nov 11, 2004	New release, general updates	MSL	PSV
D	Mar 15, 2005	Temp range clarified, ergonomics removed	MSL	PSV
E	Mar 1, 2006	Recommended DRIVC and ADCREF settings added	MSL	PSV
F	Mar 14, 2006	New ADCREF setting, RoHS compliance added	MSL	PSV
G	Mar 21, 2006	Register settings, update	MSL	PSV
H	June 4, 2007	Typical supply current changed, packing added	MSL	PSV
I	Aug 14, 2007	Info on additional supplier added	MSL	PSV
J	Sep 06, 2007	Detailed info on sensor operation added	MSL	PSV
K	Feb 13, 2008	Keep out area added in *Sensor assembly* section	MSL	PSV
L	Mar 18, 2008	New sensor revisions added in *Sensor setup* section	MSL	PSV

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