FPC1011F Area Sensor Package

Product Specification

FINGERPRINTS

Features

- Fingerprint area sensor
- NEW hard and scratch resistant protective surface coating
- Superior image quality
- 3D image with 256 true gray scale values
- Ergonomic frame for optimized finger guidance
- High speed SPI interface or Parallel interface
- Flex connector or BGA
- 3.3 and 2.5 volt operation
- >15kV ESD protection
- >1 million wear cycles

RoHS Compliant Directive 2002/95/EC

LEAD FREE

Application examples

- Computer peripheral
- Physical access control
- Time and attendance
- Wireless devices
- Security application
- Medical equipment & storage

General description

FPC1011F is a new compact CMOS fingerprint sensor with several significant advantages. FPC1011F deliveries superior image quality, with 256 gray scale values in every single pixel. The reflective measurement method sends an electrical signal via the frame directly into the finger. This technique enables the use of an unbeatably hard and thick protective surface coating. The sensor with its 3D pixel sensing technology can read virtually any finger; dry or wet.

Thanks to the new extremely hard and durable surface coating, FPC1011F is protected against ESD well above 15 kV, as well as scratches, impact and everyday wear-and-tear. FPC1011F is delivered with a designed micro-ergonomic guidance frame, simplifying proper fingerprint guidance and hence improving algorithm performance.

FPC1011F is available in two configurations; either a versatile flex connector version, FPC1011F1, with a serial SPI interface or a standard BGA component, FPC1011F2, with both serial and parallel interface. In higher volumes, the micro-ergonomic frame can be made available in different colors and textures.

Quick reference data

PARAMETER	DESCRIPTION	VALUE	UNIT
Dimension	Sensor body (W x L x T)	20.4 x 33.4 x 2.3	mm
Interface	Serial SPI or Parallel	8 / 32	pin
Supply voltage	VDC	2.5 - 3.3	V
Supply current	Typical at 3.3V, 4MHz and RT	7	mA
Supply current sleep mode	Power down	10	µA
Clock frequency	Serial SPI or Parallel	32	MHz
Read out speed	Serial SPI or Parallel	4	Mpixel/s
Active sensing area	Pixel matrix	10.64 x 14.00	mm
Size sensing array	Pixel matrix (363 dpi)	152 x 200	pixel
Pixel resolution	256 gray scale values	8	bit
ESD protection	IEC61000-4-2, level 4, air discharge	> 15	kV
Wear-and-tear	No of wear cycles at 6N	> 1 million	cycle

Table of contents

1 Functional description

1.1 Introduction

The FPC1011F sensor component is suitable for numerous types of authentication systems. These systems may be based on highly integrated low power solutions utilizing Fingerprint Cards' (*Fingerprints*) companion chip, or a large variety of standard micro-controllers or high performance DSPs.

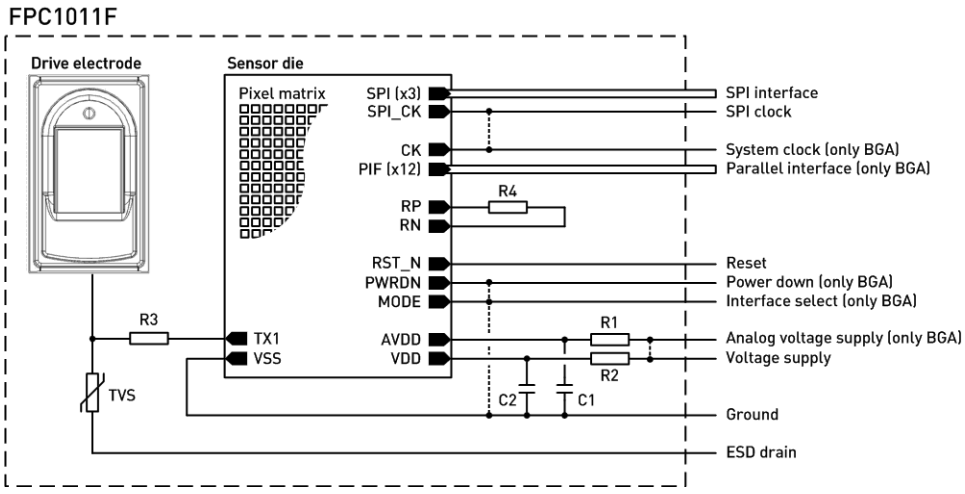
The sensor package is built around Fingerprint Cards' sophisticated 3rd generation CMOS implementation FPC1011. The FPC1011 offers both a serial SPI interface and a parallel asynchronous interface. The communication interface is easily selected by means of a separate interface selection pin (MODE).

Two package configurations are available; an 8 pin flex connector (FPC1011F1) or a 32 ball BGA (FPC1011F2).

1.2 Block diagram

Depending on selected package configuration; two separate hardware interfaces are available. Both interfaces are indicated in the figure below. Signals marked "only BGA" are only available in FPC1011F2, the 32 ball BGA version. In FPC1011F1 these signals are preset or re-routed to obtain an 8 pin serial interface.

FPC1011F1 preset configuration:
- Analog and digital power supply are combined
- System clock and SPI clock are combined
- Power down is disabled
- Mode pin is preset to serial interface
- Parallel interface cannot be accessed



Block diagram - Overview

1.3 Technical features

PARAMETER	DESCRIPTION	VALUE	UNIT
Dimension	Sensor body	20.4 x 33.4 x 2.3	mm
	Flex connector type, sensor body plus connector	20.4 x 33.4 x 5.4	mm
	BGA type, sensor body plus solder balls	20.4 x 33.4 x 2.7	mm
Active sensing area		10.64 x 14.00	mm
Size sensing array		152 x 200	pixel
Spatial resolution		363	dpi
Pixel resolution	256 gray scale levels	8	bit
Operating temperature		- 20 ... + 60	°C
Storage temperature		- 40 ... + 85	°C
ESD	IEC61000-4-2 level 4, air discharge	> ±15	kV
Package type	FPC1011F1 - 8 pin flex connector, 1mm pitch, Non-ZIF	8	pin
	FPC1011F2 - 32 ball BGA	32	pin

1.4 Sensor surface robustness

PARAMETER	DESCRIPTION	CONDITION	RESULT
Mechanical wear-and-tear	Repetitive wear-and-tear cycles	> 1 000 000 cycles @ 6N	PASS
Foreign substances	Repetitive strokes with: Acetone, Artificial sweat, Coca cola, Coffee, Isopropyl, Ethanol, Ketchup, Mosquito repellent, Oil, Petrol, Soap	200 cycles @ 6N	PASS

1.5 Application limits

The FPC1011F package is designed for indoor, non-condensing, applications. Do not subject the sensor component to direct sunlight for extended periods. The sensor surface is hard and extremely robust, and will withstand years of normal wear-and-tear. However, do not subject the sensor surface to sharp or hard objects since this might cause permanent damage.

Cleaning should be done with a soft cotton textile. Do not subject the sensor surface to excessive mechanical force. The fingerprint sensor is a high-performing SMD device and should be handled accordingly. Additional information on proper product integration is offered in the section *Sensor integration*.

1.6 Absolute maximum ratings

Supply voltage V_{DD}	-0.5 V to +7.0 V
Input voltage	-0.5 V to V_{DD} + 0.5 V
Output voltage	-0.5 V to V_{DD} + 0.5 V
Total power dissipation	50 mW
ESD on IO's	±2 kV
Pressure on sensor[1]	25 N

Note:
Stress beyond values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device, at these or other conditions beyond those indicated as normal operation in this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods, may affect device reliability.

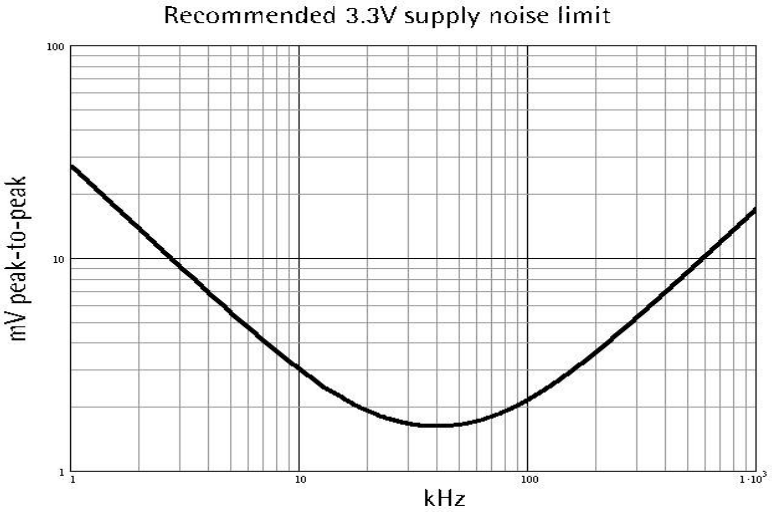
Note 1: Additional information on proper product integration is offered in the section, Sensor integration.

2 Electrical characteristics

Measured at room temperature (RT)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
FPC1011F1 - serial mode is preset						
V_{DD}	Voltage supply (total)		2.35	2.5/3.3	3.45	V
I_{DD}	Current supply, total	V_{DD} = 2.5V@4MHz	-	7	14	mA
		V_{DD} = 2.5V@32MHz	-	9	-	mA
		V_{DD} = 3.3V@4MHz	-	7	14	mA
		V_{DD} = 3.3V@32MHz	-	12	-	mA
FPC1011F2 - serial mode						
V_{DD}	Voltage supply (digital)		2.35	2.5/3.3	3.45	V
AV_{DD}	Analog voltage supply		2.35	2.5/3.3	3.45	V
I_{DD}	Current supply, total	V_{DD} = 2.5V@4MHz	-	7	-	mA
		V_{DD} = 2.5V@32MHz	-	9	-	mA
		V_{DD} = 3.3V@4MHz	-	7	-	mA
		V_{DD} = 3.3V@32MHz	-	12	-	mA
I_{DDS}	Current supply, sleep mode	PWRDN high	-	10	-	uA
FPC1011F2 - parallell mode						
V_{DD}	Voltage supply (digital)		2.35	2.5/3.3	3.45	V
AV_{DD}	Analog voltage supply		2.35	2.5/3.3	3.45	V
I_{DD}	Current supply, total	V_{DD} = 3.3V@8MHz	-	TBD	-	mA
I_{DDS}	Current supply, sleep mode	PWRDN high	-	10	-	uA
FPC1011F1/F2 - digital inputs						
V_{IL}	Logic '0' voltage		N/A	N/A	$0.2V_{DD}$	V
V_{IH}	Logic '1' voltage		$0.8V_{DD}$	N/A	N/A	V
I_{IL}	Logic '0' current (V_I = GND)		-	-	±10	uA
I_{IH}	Logic '1' current (V_I = V_{DD})		-	-	±10	uA
C_{IND}	Input capacitance		-	6	-	pF
FPC1011F1/F2 - digital outputs						
V_{OL}	Logic '0' output voltage		-	0.2	0.4	V
V_{OH}	Logic '1' output voltage		$0.85V_{DD}$	$0.90V_{DD}$	-	V

Note: Details on clock frequency is available in the General Timing section.



Differential power supply disturbance

The graph shows the supply disturbance level (sinus rms), which will give less than one gray level rms disturbance in the fingerprint image readout. If the supply voltage is noisy, additional filtering may be required.

If separate (splitted) power supplies or long connection leads are used, it is important to maintain a synchronized power on voltage curve (equivalent ramp), for both V_{DD} and AV_{DD}. This care is necessary to avoid possible latch-up problems.

3 Operation

3.1 Introduction

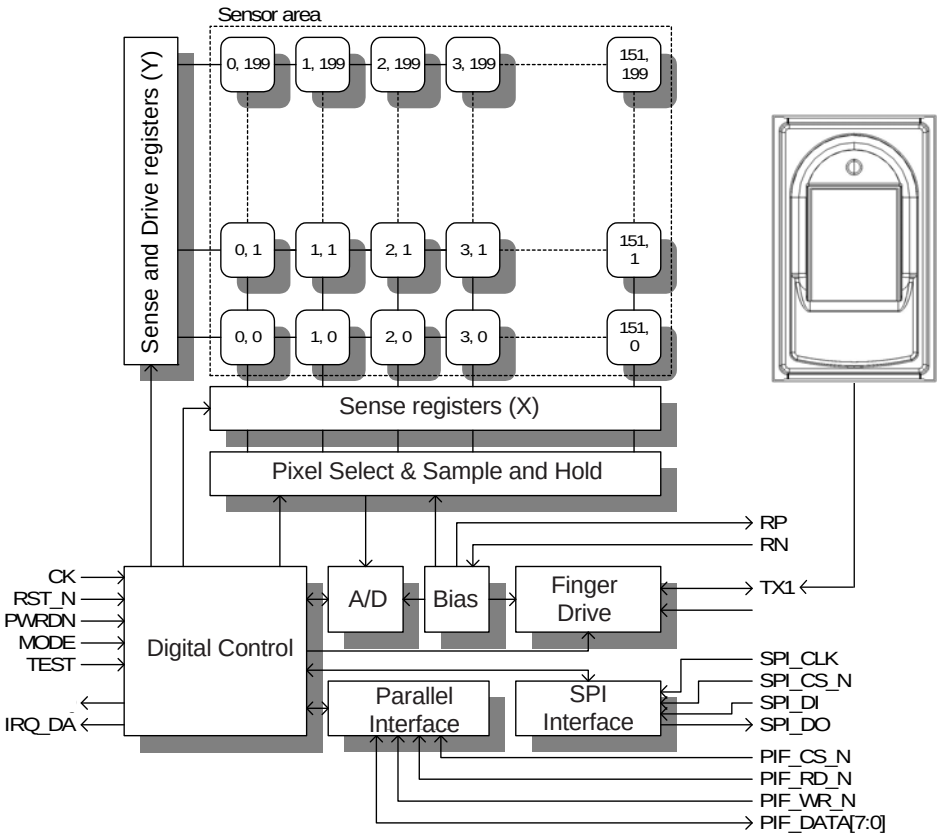
If the sensor is used together with a companion chip from Fingerprint Cards, no detailed knowledge about the sensor circuit/matrix is required in order to operate the sensor component properly.

However, if the sensor component is used together with e.g. a standard micro-controller or a DSP, a detailed understanding of the sensor operation is recommended.

3.2 Sensor technology

The sensor component uses an architecture where individual sensor elements sense a separate charge from the finger. A general block diagram for the sensor circuit is shown in the figure below.

The TX1-signal is used to supply a drive signal to the finger. Hence this signal is connected to an electrode (frame) directly surrounding the sensor area. This electrode (frame) is also part of the ESD protection.



Block diagram - Sensor circuit

3.3 Image properties

The FPC1011F sensor matrix contains 30400 pixels. On rare occasions some pixels may not be fully operational, called pixel errors (PE). A small number of imperfections do NOT degrade biometric performance. All sensors are thoroughly tested to ensure excellent image quality.

To verify the image quality and establish a proper signal-to-noise ratio (SNR), internal test functionality based on test patterns is implemented; Checkerboard and Inverted Checkerboard. To ensure conformity of the results, tests are always performed on these two internal test patterns, generated by the SENSEMODE parameter.

To meet image quality standards, test patterns must satisfy the following requirements:

PARAMETER	VALUE
PE total	≤ 60 pixels
PE on any single row	≤ 30 pixels
PE in any single column	≤ 40 pixels
PE within any 12x12 pixel area	≤ 4 pixels

Note: Entire non-operational columns or rows are not accepted and hence scrapped.

A pixel error is defined as a pixel value that differs more than 20 grayscale levels from its local image median. The local image median is the median value over a sub-image consisting of 5 complete rows, where one of the rows contains the error pixel. (The sub-images are defined as rows 1-5, 6-10, 11-15, ..., 196-200).

A proper Checkerboard (CB) pattern and Inverted Checkerboard (ICB) pattern is generated with the following parameters:

DRIVC	ADCREF	SENSEMODE
70	3	1 (CB)
70	3	2 (ICB)

Note: Further details are available in the SENSEMODE register setup.

3.4 Interface

The sensor circuit contains two separate interfaces; - a Serial Peripheral Interface (SPI) and - a fast parallel asynchronous interface.

The SPI interface enables high-speed readout of data with a minimum of wires. The SPI interface supports a speed up to the current system clock speed. This feature makes the sensor usable for a wide range of control units. The SPI interface is a slave interface with CPHA = '0' and CPOL = '0'.

The parallel interface is included to enable even faster communication with a large variety of micro-controllers. The parallel interface is asynchronous and uses RD_N and WR_N as read and write strobes when accessing the sensor.

Through the communication interface, pixel data from the sensor circuit is entered into a FIFO, which in turn is read by applying read instructions. This FIFO enables a burst read out speed of up to 32 Mpixel/s in parallel mode. The maximum average readout speed in parallel mode is 4 Mpixel/s. The maximum readout speed in serial mode is 4 Mpixel/s.

A mode pin selects between the two interfaces (Interface select). Only one interface may be used at a time.

MODE	ENABLER	DESCRIPTION
Serial	MODE = '0'	SPI interface enabled
Parallel	MODE = '1'	Parallel interface enabled

Interface selection using the mode pin

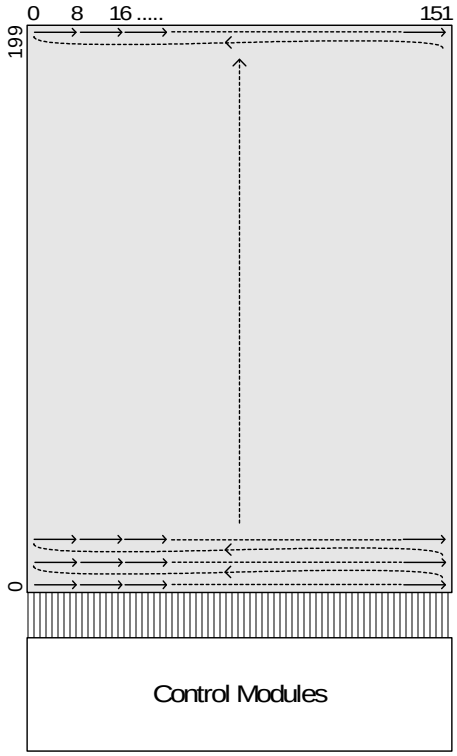
TYPE	SERIAL	PARALLEL
FPC1011F1	Yes	No (mode is preset)
FPC1011F2	Yes	Yes

Available interfaces - select with mode pin

3.5 Sensor readout

The sensor matrix consists of 152 x 200 sensor elements. The entire sensor, or a part of it, is read by applying a read sensor instruction. The size of the active area is set by the values of the XSHIFT and YSHIFT registers.

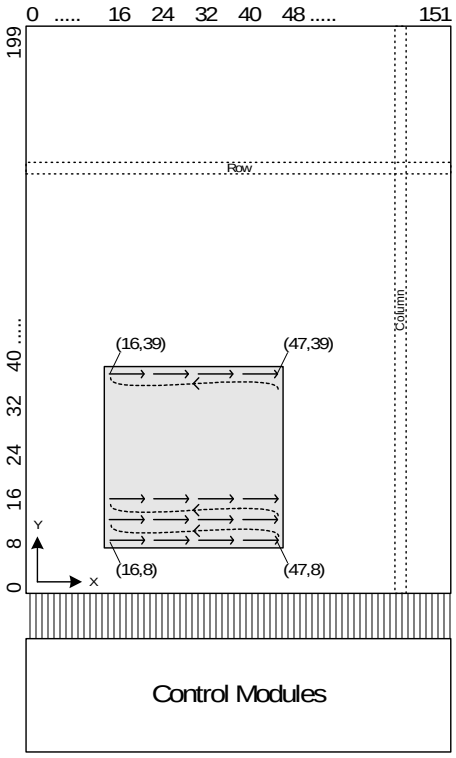
The default values for these registers select the complete sensor area to be read once. The readout sequence is illustrated in the figure below.



During all read operations, 8 pixels are captured simultaneously. By default the first 8 pixels being read are pixel (0,0) to (7,0), followed by pixels (8,0) to (15,0).

The readout area can be reduced by setting the XSHIFT and YSHIFT registers.

The sense area (a row of 8 pixels) is shifted in the x-direction XSHIFT times before it is shifted in the y-direction. The default start position can be changed by manually loading the SENSEX and SENSEY registers.



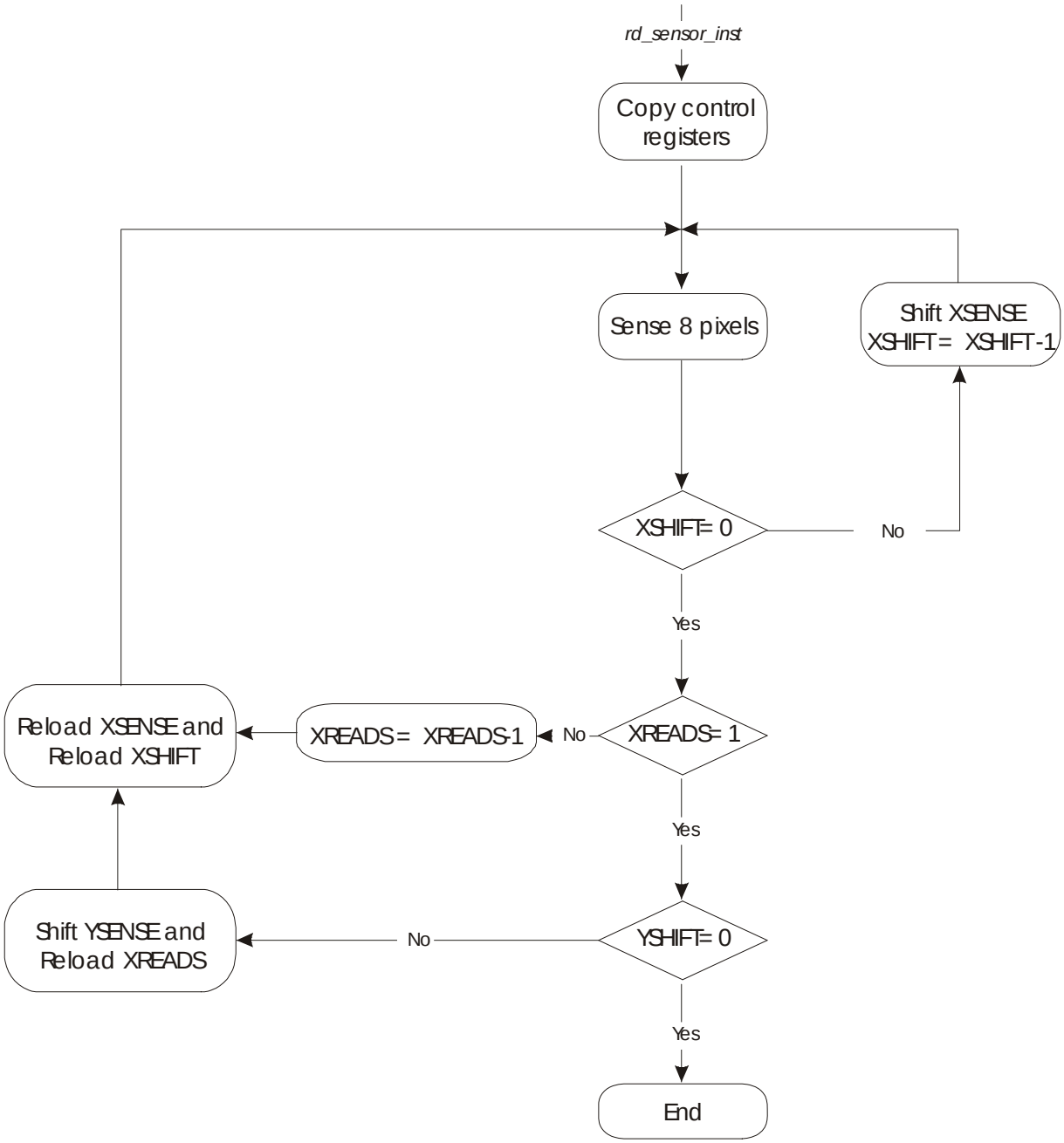
By setting XSENSE and YSENSE to start with pixels (16,8) to (23,8) and setting XSHIFT to 3 and YSHIFT to 31 the rectangle defined by the pixels (16,8) and (47,39) will be read, giving a total of 1024 pixels. Partial readout is illustrated in the figure above.

It is possible to read one row of pixels several times before shifting to the next row. This is done by setting the XREADS register.

The number of pixels being read is given by the following formula:

$$\#pixels = 8 \cdot (XSHIFT+1) \cdot (YSHIFT+1)$$

Figure on next page shows the read sequence in detail.



Sensor read sequence

4 Serial mode

In serial mode all communication is done through the serial SPI interface.
The available commands are described in this section.

4.1 Instruction summary

INSTRUCTION	INSTRUCTION CODE	DESCRIPTION
rd_sensor	11_H	Start sensing of finger. Data is placed in the FIFO.
rd_spidata	20_H	Read from FIFO (only applicable when the SPI interface is used)
rd_spistat	21_H	Read internal status registers in the SPI interface (only applicable when the SPI interface is used)
rd_regs	50_H	Read internal registers. All registers are read in one operation. The register content is placed in the FIFO.
wr_drivc	75_H	Write DRIVC register. Set finger drive amplitude.
wr_adcref	76_H	Write ADCREF register. Set ADC sensitivity.
wr_sensem	77_H	Write SENSEMODE register. Set self-test mode.
wr_fifo_th	$7C_H$	Write FIFO_TH register. Set the FIFO fill threshold for activation of data available signal, DA bit in SPI_STAT register or IRQ_DA (FPC1011F2).
wr_xsense	$7F_H$	Shift data into the XSENSE register.
wr_ysense	81_H	Shift data into the YSENSE register.
wr_xshift	82_H	Write XSHIFT register. Set number of shifts to be performed in the x-direction.
wr_yshift	83_H	Write YSHIFT register. Set number of shifts to be performed in the y-direction.
wr_xreads	84_H	Write XREADS register. Set number of times the same row should be read before shifting the YSENSE register.

4.2 Sensor setup

If the FPC1011F sensor is **NOT** used together with a companion chip from Fingerprint Cards, but instead with a standard micro-controller, a DSP or similar, an easy register setup is necessary.

The appropriate default parameters are indicated in table below. For detailed instructions on how to perform the actual register setup, please refer to the *Serial mode instructions* section in this document.

DRIVC	ADCREF	SENSEMODE
127	2	0

4.3 Serial mode instructions

Below all instructions are described in detail. Relevant timing diagrams are showed in the section *Timing properties*.

In addition to the long shift-registers controlling the pixels in the sensor array, the sensor component contains one SPI status register and 13 control registers. All write instructions to registers operate in the same way. The FIFO-pointers are reset when any instruction except <rd_spidata> and <rd_spistat> is applied.

Read sensor instruction

INSTRUCTION	rd_sensor (11_H)
Mode	serial
Input parameters	1 dummy byte
Data delay[1]	(363±2)t_{CLK}
Returned bytes	0

Note 1: Data delay is the delay time from when the instruction is given, until data is available in the FIFO. The uncertainty, ±2 clock cycles, is only valid if separate SPI and system clocks are used (only possible in FPC1011F2 in serial mode).

This instruction is used to read the entire sensor or a part of it. Timing for reading in serial mode is defined in the section *Timing properties*.

The read sensor instruction is only used to start the sense-sequence, and the instruction itself does not return any data. The first data from the sensor array will enter the FIFO after approximately 363 clock-cycles. After that, a new byte will enter the FIFO every 8th clock-cycle until the area defined by the XSENSE, YSENSE, XSHIFT and YSHIFT registers has been read.

When the FIFO is filled to a level equal to or greater than the value set by the FIFO_TH register, the SPI_STAT register will indicate that data is ready for fetching.

If the FIFO is filled up with data, overflow is avoided by stalling sensing until data is read from the FIFO. During this stall-period all analog modules are active, and the ASIC will draw current as during a regular sense operation.

Read SPI data instruction

INSTRUCTION	rd_spidata (20_H)
Mode	serial
Input parameters	1 dummy byte
Data delay	0
Returned bytes	n

After the read SPI data instruction is sent, <rd_spidata>, pixel data will be returned as shown in Figure 11. Data will continue to be returned as long as SPI_CS_N and SPI_DI are kept low.

SPI_DI should be kept low after the <rd_spidata>, instruction is entered to avoid the subsequent byte to be interpreted as a new instruction.

The reading of data can be stopped at any time without data-loss by setting SPI_CS_N high, as long as SPI_CS_N is set high between the last bit of the current byte being read and the first bit in the next byte.

If SPI_CS_N is released at any other time (e.g. during a byte transfer) one or more bytes will be lost. To continue readout after a stop caused by setting SPI_CS_N high, the <rd_spidata> instruction has to be applied again.

Read SPI status instruction

INSTRUCTION	**rd_spistat** (21_H)
Mode	serial
Input parameters	1 dummy byte
Data delay	0
Returned bytes	1

The SPI status register holds status information for the SPI interface. When the read SPI status instruction is applied, the content of the SPI_STAT register is returned. Applying this instruction does not interrupt sensor readout if sensor readout is in progress.

When the FIFO fill threshold is reached, the DA bit in the SPI_STAT register and the IRQ_DA signal will be set. The IRQ_DA signal pin is not available in FPC1011F1, only in FPC1011F2.

REGISTER			**SPI_STAT**				
Size (active bits)			3				
7	6	5	4	3	2	1	0
-	-	-	-	-	UFL	STL	DA
Reset			00_H (default value)				
001			Data available in FIFO.				
010			Stall. Bit is set if sensing is stalled due to a full FIFO.				
100			Underflow. Bit is set if underflow occurs.				

Read registers instruction

INSTRUCTION	rd_regs (50_H)
Mode	serial
Input parameters	1 dummy byte
Data delay	0
Returned bytes	0

The read register instruction fills the FIFO with the value of all the internal control registers. The order in which the registers are entered into the FIFO is given in the table below.

This instruction does not return any data. Data has to be read with the <rd_spidata> instruction The read SPI data instruction can directly follow this instruction for readout of register data.

RETURN ORDER	REGISTER
1	STATUS
2	NOT USED
3	DRIVC
4	ADCREF
5	SENSEMODE
6	FIFO_TH
7	NOT USED
8	XSHIFT
9	YSHIFT
10	XREADS
11	NOT USED
12	NOT USED
13	NOT USED
14	00_H
15	00_H
16	00_H

Return order for register values

The STATUS register is a read only register, which holds the status information for the FIFO.

REGISTER			STATUS				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	STL	UFL
Reset			00_H (default value)				
01			Underflow. Bit is set if underflow occurs.				
10			Stall. Bit is set if sensing is stalled due to a full FIFO.				

Remaining control registers (3-10) can be operated with both read and write instructions. Details on these registers are available together with the write instructions for each register.

All flag generation is based on comparing write-pointer with read pointer synchronized to SPI clock. This means that if a read instruction, resulting in an underflow, occurs one clock period before new data enters the FIFO, an undetected underflow will occur. To avoid this, the procedure for reading from the FIFO, which is outlined in FIFO_TH register description, should be followed.

The entire register is reset when a <rd_regs> instruction is executed.

Write to DRIVC register

INSTRUCTION	wr_drivc (75_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The DRIVC register sets the amplitude for the drive signal, active on the drive electrode (frame).

The recommended DRIVC setting is listed in the *Sensor setup* section. With default value set, the drive signal is disabled.

REGISTER			DRIVC				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			00_H (default value)				
0_D			Min voltage, Electrode drive off				
127_D			Approximately $V_{DD}/2$				
128_D - 255_D			Max voltage, approx V_{DD}				

Write to ADCREF register

INSTRUCTION	wr_adcref (76_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The ADCREF register sets the dynamic range for the internal A/D converter. This register is set to '11' at reset.

The recommended ADCREF setting is listed in the *Sensor setup* section.

REGISTER			ADCREF				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	x	x
Reset			00_H (default value)				
00			0.125 x V_{DD}				
01			0.250 x V_{DD}				
10			0.375 x V_{DD}				
11			0.500 x V_{DD}				

Write to SENSEMODE register

INSTRUCTION	wr_sensem (77_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The SENSEMODE register is a 2-bit register, which sets the test mode. In normal operation, this register should be cleared.

REGISTER			SENSEMODE				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	x	x
Reset			00_H (default value)				
00			Regular image capture mode (default)				
01			Checker board test				
10			Inverted checker board test				
11			Black test				

If the SENSEMODE register value is non-zero, different types of test patterns are generated internally in the sensor when an image is captured. The Checkerboard test pattern has high grayscale values for pixels on all even columns on even rows, and odd columns of odd rows. Subsequently, pixels on even columns on odd rows, and odd columns on even rows has a low grayscale value, creating a checkerboard pattern all over the image area.

Similarly, the Inverted checker board test pattern has high grayscale values where the regular checkerboard test pattern has low grayscale values, and vice versa.

Finally, the Black test pattern mode makes all grayscale values high. (The normal procedure when looking at a captured image is to first invert the image, since this makes an image of an actual finger look like an inked fingerprint. Therefore an image with all grayscale values high is considered to be an all black image.)

Write to FIFO_TH register

INSTRUCTION	wr_fifo_th ($7C_H$)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The FIFO_TH register holds the threshold value for the FIFO. When the fill level for the FIFO is higher than or equal to this value, the DA bit in the SPI_STAT register is set.

The internal sensor data FIFO is 16 bytes deep and the threshold level can be set between 1 and 16. If this register is set to 00_H the DA bit will be set to indicate when all 16 bytes are holding valid data. The relation between the register value and the threshold level is shown below.

REGISTER			FIFO_TH				
Size (active bits)			4				
7	6	5	4	3	2	1	0
-	-	-	-	x	x	x	x
Reset			08_H (default value)				
0000			Threshold level 16				
0001			Threshold level 1				
0010			Threshold level 2				
:			:				
1111			Threshold level 15				

Write to XSENSE/YSENSE register

INSTRUCTION	wr_xsense ($7F_H$)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

INSTRUCTION	wr_ysense (81_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

These registers are used to select which pixels are active during sensing.

The values of these registers can be changed using the <wr_xsense> and <wr_ysense> instructions. When any of these instructions are applied, the XSENSE and YSENSE register, respectively, are shifted 8 bits towards the MSB and the 8 LSB's are replaced with the new byte.
The sensor circuit contains 8 sample-and-hold modules. Column n·8+m, where n={0..18} and m={0..7}, are connected to the sample-and-hold module number m, through pass gates.

These pass gates are controlled by the XSENSE register. It is important not to let two pixels drive the same sample-and-hold module when loading a non-default value to these registers.

It is also important that only one row is active at a time. The YSENSE register controls which row is active. Please make sure that only one bit in the YSENSE register is set to '1' at any time. If more that one bit in the YSENSE register is set to '1', the returned picture will be invalid, and current-consumption will increase.

To activate a pixel (sensing), the associated bits in both the XSENSE and the YSENSE registers have to be set.

During the fingerprint sensing period, the 8 sample-and-hold modules sample data simultaneously. This data is then digitized before a new sample-and-hold operation is performed. Data is always returned starting with sample-and-hold number 0 and ending with sample-and-hold number 7.

This means that if XSENSE is set to start sensing column 3 to 10 (instead of 0 to 7 which is default) and the shift mode is set to shift 8 positions, the pixels will be read out in the following order (by column number): 8, 9, 10, 3, 4, 5, 6, 7, 16, 17, 18, 11, 12, 13, 14, 15 and so on. This is illustrated in the table below.

REGISTER	XSENSE
Size (bit/bytes)	152 / 19
Reset	00 ... $00FF_H$ (default value)

REGISTER	YSENSE
Size (bit/bytes)	200 / 25
Reset	00 ... 0001_H (default value)

XSENSE START VALUE	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
COLUMN NO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CONNECTED TO SH NO	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
SAMPLE CYCLE NO				1								2								3				

Illustration of readout sequence with a non-standard start value for XSENSE

Write to XSHIFT register

INSTRUCTION	wr_xshift (82_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The XSHIFT register holds the number of shifts performed in the x direction. The number of sense operations performed in one row exceeds the value stored in this register by one.

REGISTER			XSHIFT				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			12_H (18_D) (default value)				

Write to XREADS register

INSTRUCTION	wr_xreads (84_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The XREADS register holds the number of times the same row is read before shifting to the next.

REGISTER			XREADS				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			01_H (default value)				

Write to YSHIFT register

INSTRUCTION	wr_yshift (83_H)
Mode	serial
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The YSHIFT register holds the number of shifts performed in the y-direction. The number of lines sensed exceeds the value stored in this register by one.

REGISTER			YSHIFT				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			$C7_H$ (199_D) (default value)				

4.4 Sample Implementation

This section describes step-by-step how the SPI interface of FPC1011F can be used to perform a basic image readout process. We will outline in detail which commands the SPI host needs to transmit to receive the full sensor image.

a) Establish a SPI connection between the SPI host and slave, using CPHA='0' and CPOL='0', at any clock speed <32MHz, and big endian bit order. Also, let the host enable the Chip Select signal in the SPI interface.

b) Send the three instructions <wr_drivc>, <wr_adcref>, and <wr_sensemode> with corresponding parameter values **127**, **2**, and **0** (recommended default values) to set the sensor readout parameters.

DRIVC	ADCREF	SENSEMODE
127	2	0

If all other registers are left at their default values, the complete image area is read.

c) Tell the sensor to capture an image by sending the instruction <rd_sensor>, with a dummy parameter value.

d) It will take some time before the first pixel data is available for reading in the FIFO. In SPI mode there are three ways to know when to start reading pixel data:

- *Counting cycles*, after 363 +/- 2 cycles the first pixel data will be available for reading. The FIFO gives a flexibility to safely start reading pixel data in cycle 365 - 489.

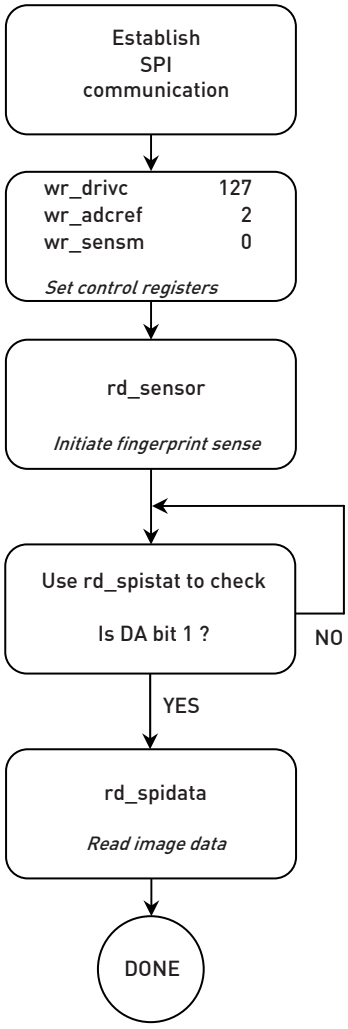
- *IRQ_DA signal* (only FPC1011F2), when the FIFO threshold (FIFO_TH register) is reached, the IRQ_DA signal is set (high). The default value for the FIFO_TH register is 8 (the FIFO is 16 bytes in total).

- *Polling the SPI_STATUS register*, when the FIFO threshold (FIFO_TH register) is reached, the DA bit (data available bit) is set (high).

Further details on how to operate the FIFO_TH register is available in the section *Serial mode instruction*.

e) Now, use the <rd_spidata> instruction to read 30400 bytes of pixel data. The read pixel data is delivered row by row, with 1 byte per pixel, forming an image with dimensions 152 columns times 200 rows.

f) Finally, let the host disable the Chip Select Signal, and (if applicable) shut down the connection to FPC1011F.



5 Parallel mode

In parallel mode all communication is done through the parallel asynchronous interface.
The available commands are described in this section.

5.1 Instruction summary

INSTRUCTION	INSTRUCTION CODE	DESCRIPTION
rd_sensor	11_H	Start sensing of finger. Data is placed in the FIFO.
rd_regs	50_H	Read internal registers. All registers are read in one operation. The register content is placed in the FIFO.
wr_drivc	75_H	Write DRIVC register. Set finger drive amplitude.
wr_adcref	76_H	Write ADCREF register. Set ADC sensitivity.
wr_sensem	77_H	Write SENSEMODE register. Set self-test mode.
wr_fifo_th	$7C_H$	Write FIFO_TH register. Set the FIFO fill threshold for activation of the data available signal, IRQ_DA.
wr_xsense	$7F_H$	Shift data into the XSENSE register.
wr_ysense	81_H	Shift data into the YSENSE register.
wr_xshift	82_H	Write XSHIFT register. Set number of shifts to be performed in the x-direction.
wr_yshift	83_H	Write YSHIFT register. Set number of shifts to be performed in the y-direction.
wr_xreads	84_H	Write XREADS register. Set number of times the same row should be read before shifting the YSENSE register.

5.2 Sensor setup

When using the parallel interface, a register setup is always required.

The appropriate default parameters are indicated in the table below. For detailed instructions on how to perform the actual register setup, please refer to the *Parallel mode instructions* section in this document.

DRIVC	ADCREF	SENSEMODE
127	2	0

5.3 Parallel mode instructions

Below all instructions are described in detail. Relevant timing diagrams are showed in the section *Timing properties*.

In addition to the long shift-registers controlling the pixels in the sensor array, the sensor component contains 13 control registers. All write instructions to registers operate in the same way. The FIFO-pointers are reset when any instruction is applied.

Read sensor instruction

INSTRUCTION	rd_sensor (11_H)
Mode	parallel
Input parameters	1 dummy byte
Data delay[1]	(363±2)t_{CK}
Returned bytes	0

*Note1: Data delay is the delay time from when the instruction is given, until data is available in the FIFO. The uncertainty, ±*2 clock cycles, is due to the asynchronous nature of the interface (only valid for FPC1011F2).

This instruction is used to read the entire sensor or a part of it. Timing for reading in parallel mode is defined in the section *Timing properties*.

The read sensor instruction is only used to start the sense-sequence, and the instruction itself does not return any data. The first data from the sensor array will enter the FIFO after approximately 363 clock-cycles. After that, a new byte will enter the FIFO every 8th clock-cycle until the area defined by the XSENSE, YSENSE, XSHIFT and YSHIFT registers has been read.

When the FIFO is filled to a level equal to or greater than the value set by the FIFO_TH register, the IRQ_DA signal comes high to indicate that data is ready for fetching. Reading data from the FIFO in parallel mode is done using the PIF_RD_N signal. Details are available in the section *Parallel mode timing.*

If the FIFO is filled up with data, overflow is avoided by stalling sensing until data is read from the FIFO. During this stall-period all analog modules are active, and the ASIC will draw current as during a regular sense operation.

Read registers instruction

INSTRUCTION	rd_regs (50_H)
Mode	parallel
Input parameters	1 dummy byte
Data delay	$2\pm2t_{CK}$
Returned bytes	0

The read register instruction fills the FIFO with the value of all the internal control registers. The order in which the registers are entered into the FIFO is given in the table below.

Reading data from the FIFO in parallel mode is done using the PIF_RD_N signal. Details are available in the section *Parallel mode timing.*

Contents of the registers are available no later than $4 \cdot t_{CK}$ after the input parameter for this instruction is applied.

This instruction will completely fill the FIFO as shown in the table to the right. As a result of this, the IRQ_DA signal will go high when data is available in the FIFO. Readout of the data in the FIFO can be stopped at any time.

RETURN ORDER	REGISTER
1	STATUS
2	NOT USED
3	DRIVC
4	ADCREF
5	SENSEMODE
6	FIFO_TH
7	NOT USED
8	XSHIFT
9	YSHIFT
10	XREADS
11	NOT USED
12	NOT USED
13	NOT USED
14	00_H
15	00_H
16	00_H

Return order for register values

The STATUS register is a read only register, which holds the status information for the FIFO.

REGISTER			STATUS				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	STL	UFL
Reset			00_H (default value)				
01			Underflow. Bit is set if underflow occurs.				
10			Stall. Bit is set if sensing is stalled due to a full FIFO.				

Remaining control registers (3-10) can be operated with both read and write instructions. Details on these registers are available together with the write instructions for each register.

All flag generation is based on comparing write-pointer with read pointer synchronized to the system clock CK. This means that if a read instruction, resulting in an underflow, occurs one clock period before new data enters the FIFO, an undetected underflow will occur. To avoid this, the procedure for reading from the FIFO, which is outlined in FIFO_TH register description, should be followed.

The entire register is reset when a <rd_regs> instruction is executed.

Write to DRIVC register

INSTRUCTION	wr_drivc (75_H)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The DRIVC register sets the amplitude for the drive signal, active on the drive electrode (frame).

The recommended DRIVC setting is listed in the *Sensor setup* section. With default value set, the drive signal is disabled.

REGISTER			DRIVC				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			00_H (default value)				
0_D			Min voltage, Electrode drive off				
127_D			Approximately $V_{DD}/2$				
128_D - 255_D			Max voltage, approx V_{DD}				

Write to ADCREF register

INSTRUCTION	wr_adcref (76_H)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The ADCREF register sets the dynamic range for the internal A/D converter. This register is set to '11' at reset.

The recommended ADCREF setting is listed in the *Sensor setup* section.

REGISTER			ADCREF				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	x	x
Reset			00_H (default value)				
00			0.125 x V_{DD}				
01			0.250 x V_{DD}				
10			0.375 x V_{DD}				
11			0.500 x V_{DD}				

Write to SENSEMODE register

INSTRUCTION	wr_sensem (77_H)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The SENSEMODE register is a 2-bit register, which sets the test mode. In normal operation, this register should be cleared.

REGISTER			SENSEMODE				
Size (active bits)			2				
7	6	5	4	3	2	1	0
-	-	-	-	-	-	x	x
Reset			00_H (default value)				
00			Regular image capture mode (default)				
01			Checker board test				
10			Inverted checker board test				
11			Black test				

If the SENSEMODE register value is non-zero, different types of test patterns are generated internally in the sensor when an image is captured. The Checkerboard test pattern has high grayscale values for pixels on all even columns on even rows, and odd columns of odd rows. Subsequently, pixels on even columns on odd rows, and odd columns on even rows has a low grayscale value, creating a checkerboard pattern all over the image area.

Similarly, the Inverted checker board test pattern has high grayscale values where the regular checkerboard test pattern has low grayscale values, and vice versa.

Finally, the Black test pattern mode makes all grayscale values high. (The normal procedure when looking at a captured image is to first invert the image, since this makes an image of an actual finger look like an inked fingerprint. Therefore an image with all grayscale values high is considered to be an all black image.)

Write to FIFO_TH register

INSTRUCTION	wr_fifo_th ($7C_H$)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The FIFO_TH register holds the threshold value for the FIFO. When the fill level for the FIFO is higher than or equal to this value, the IRQ_DA signal is comes high.

The internal sensor data FIFO is 16 bytes deep and the threshold level can be set between 1 and 16. If this register is set to 00_H the IRQ_DA signal will come high to indicate when all 16 bytes are holding valid data. The relation between the register value and the threshold level is shown below.

REGISTER			FIFO_TH				
Size (active bits)			4				
7	6	5	4	3	2	1	0
-	-	-	-	x	x	x	x
Reset			08_H (default value)				
0000			Threshold level 16				
0001			Threshold level 1				
0010			Threshold level 2				
:			:				
1111			Threshold level 15				

Write to XSENSE/YSENSE register

INSTRUCTION	wr_xsense ($7F_H$)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

INSTRUCTION	wr_ysense (81_H)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

These registers are used to select which pixels are active during sensing.

The values of these registers can be changed using the <wr_xsense> and <wr_ysense> instructions. When any of these instructions are applied, the XSENSE and YSENSE register, respectively, are shifted 8 bits towards the MSB and the 8 LSB's are replaced with the new byte.
The sensor circuit contains 8 sample-and-hold modules. Column n·8+m, where n={0..18} and m={0..7}, are connected to the sample-and-hold module number m, through pass gates.

These pass gates are controlled by the XSENSE register. It is important not to let two pixels drive the same sample-and-hold module when loading a non-default value to these registers.

It is also important that only one row is active at a time. The YSENSE register controls which row is active. Please make sure that only one bit in the YSENSE register is set to '1' at any time. If more that one bit in the YSENSE register is set to '1', the returned picture will be invalid, and current-consumption will increase.

To activate a pixel (sensing), the associated bits in both the XSENSE and the YSENSE registers have to be set.

During the fingerprint sensing period, the 8 sample-and-hold modules sample data simultaneously. This data is then digitized before a new sample-and-hold operation is performed. Data is always returned starting with sample-and-hold number 0 and ending with sample-and-hold number 7.

This means that if XSENSE is set to start sensing column 3 to 10 (instead of 0 to 7 which is default) and the shift mode is set to shift 8 positions, the pixels will be read out in the following order (by column number): 8, 9, 10, 3, 4, 5, 6, 7, 16, 17, 18, 11, 12, 13, 14, 15 and so on. This is illustrated in the table below.

REGISTER	XSENSE
Size (bit/bytes)	152 / 19
Reset	00 ... $00FF_H$ (default value)

REGISTER	YSENSE
Size (bit/bytes)	200 / 25
Reset	00 ... 0001_H (default value)

XSENSE START VALUE	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
COLUMN NO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CONNECTED TO SH NO	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
SAMPLE CYCLE NO				1								2								3				

Illustration of readout sequence with a non-standard start value for XSENSE

Write to XSHIFT register

INSTRUCTION	wr_xshift (82_H)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The XSHIFT register holds the number of shifts performed in the x direction. The number of sense operations performed in one row exceeds the value stored in this register by one.

REGISTER			XSHIFT				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			12_H (18_D) (default value)				

Write to XREADS register

INSTRUCTION	wr_xreads (84_H)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The XREADS register holds the number of times the same row is read before shifting to the next.

REGISTER			XREADS				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			01_H (default value)				

Write to YSHIFT register

INSTRUCTION	wr_yshift (83_H)
Mode	parallel
Input parameters	1 byte
Data delay	NA
Returned bytes	NA

The YSHIFT register holds the number of shifts performed in the y-direction. The number of lines sensed exceeds the value stored in this register by one.

REGISTER			YSHIFT				
Size (active bits)			8				
7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
Reset			$C7_H$ (199_D) (default value)				

5.4 Sample Implementation

This section describes step-by-step how the parallel interface (PIF) of FPC1011F can be used to perform a basic image readout process. We will outline in detail which commands the host needs to transmit to receive the full sensor image.

a) Enable the Chip Select signal in the PIF interface.

b) Send the three instructions <wr_drivc>, <wr_adcref>, and <wr_sensemode> with corresponding parameter values **127**, **2**, and **0** (recommended default values) to set the sensor readout parameters.

DRIVC	ADCREF	SENSEMODE
127	2	0

If all other registers are left at their default values, the complete image area is read.

c) Tell the sensor to capture an image by sending the instruction <rd_sensor>, with a dummy parameter value.

d) It will take some time before the first pixel data is available for reading from the FIFO. In parallel mode there are two ways to know when to start reading pixel data:

- *Counting cycles*, after 363 +/- 2 cycles the first pixel data will be available for reading. The FIFO gives a flexibility to safely start reading pixel data in cycle 365 - 489.

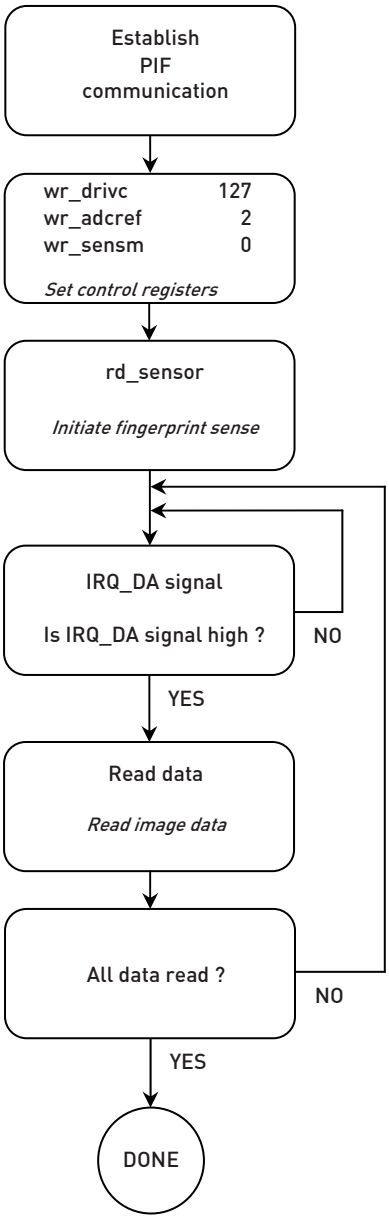
- *IRQ_DA signal*, when the FIFO threshold (FIFO_TH register) is reached the IRQ_DA signal is set (high). The default value for the FIFO_TH register is 8 (the FIFO is 16 bytes in total).

Further details on how to operate the FIFO_TH register is available in the *Parallel mode instruction* section.

e) Read the same number of bytes as the threshold level. To prevent stalling the sensor, it is best to do this before the FIFO is completely full. A new byte enters the FIFO every 8th clock-cycle.

When the number of bytes in the FIFO drops below the threshold, the IRQ_DA will go low and it is time to wait for a new interrupt.

f) Finally, let the host disable the Chip Select Signal, and (if applicable) shut down the connection to FPC1011F.



6 Timing requirements

6.1 General timing

Estimated values

SYMBOL	PARAMETER (CONDITION)	MIN	TYP	MAX	UNIT
f_{CK}	System clock frequency	2.5	-	32	MHz
t_{RSTPD}	Time from RST_N low to PWRDN low	30	-	-	ns
t_{RST}	Reset time	30[1]	-	-	ns
t_{PDS}	PWRDN setup time. Start-up time for ASIC.	10 [2]	-	-	µs
t_{PDH}	PWRDN hold time.	0 [2]	-	-	ns
t_{PDD}	PWRDN disable time. Shut-down time for ASIC.	15 [2]	-	-	ns
t_{RD}	Rise time for digital inputs	-	-	3 [2]	ns
t_{FD}	Fall time for digital inputs	-	-	3 [2]	ns
P_{PDS}	PWRDN setup energy	-	6	-	nJ

Note 1: Reset is guaranteed for this duration, but may occur for shorter pulses.

Note 2: Simulated value

6.2 Serial mode timing

Estimated values

SYMBOL	PARAMETER (CONDITION)	MIN	TYP	MAX	UNIT
f_{SPI_CK}[1]	Frequency for SPI clock.	0	-	f_{CK}[2]	MHz
t_{SCKL}	Part of SPI_CK clock period, during which SPI_CK is low.	14	-	-	ns
t_{SCKH}	Part of SPI_CK clock period, during which SPI_CK is high.	14	-	-	ns
t_{CSCKF}	Time from falling edge on SPI_CK to edge on SPI_CS_N	4	-	-	ns
t_{CSCKR}	Time from edge on SPI_CS_N to rising edge on SPI_CK	4	-	-	ns
t_{DSU}	Setup time for data before rising edge of SPI_CK	5	-	-	ns
t_{DH}	Hold time for data after rising edge of SPI_CK	5	-	-	ns
t_{SCKD}	Delay from falling clock to data available.	0	-	8	ns
t_{SSU}	Delay from SPI_CS_N low to SPI_DI mode change.	0	-	5	ns

Note 1: On FPC1011F1 the system clock CK is internally connected with SPI_CK and cannot be set separately.

Note 2: To reach the full SPI communication speed (32MHz), it is necessary to meet all timing requirements above.

Figure 1 shows the general timing for the SPI interface. The figure only shows input and output of 1 byte, but can be extended to more bytes by keeping SPI_CS_N low for more clock cycles. Dependencies between SPI_DI, SPI_DO and SPI_CK are only shown once, but apply to all clock cycles.

All instructions applied consist of one instruction byte and one data byte. This is illustrated in Figure 2 and Figure 3 for instructions without and with return parameters.

The first byte applied, after the SPI_CS_N signal is set low, is interpreted as an instruction byte. After that every other byte is interpreted as a new instruction. This makes it possible to apply new instructions without releasing SPI_CS_N.

If no new instruction should be applied after the first, e.g. during data readout, the following bytes should all be zeroes. The first byte after an all-zero byte is always interpreted as an instruction-byte.

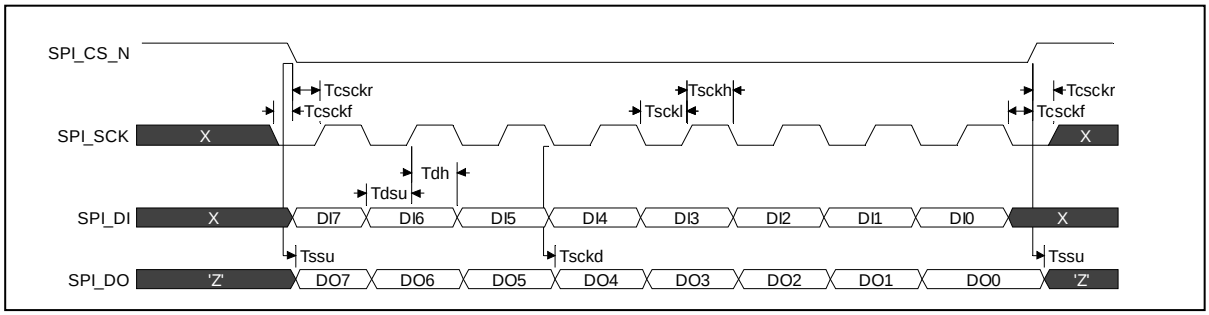


Figure 1
General SPI timing

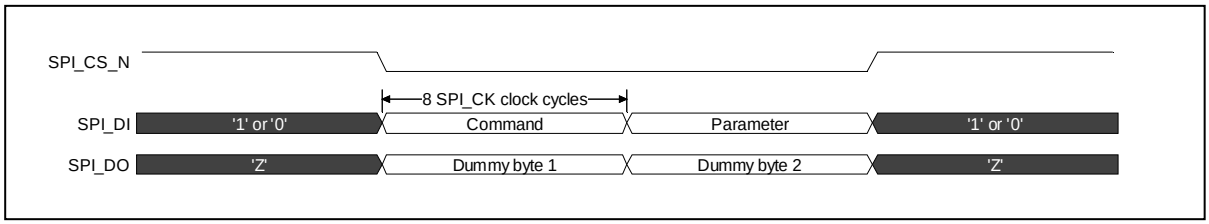


Figure 2
Applying an instruction without return data.

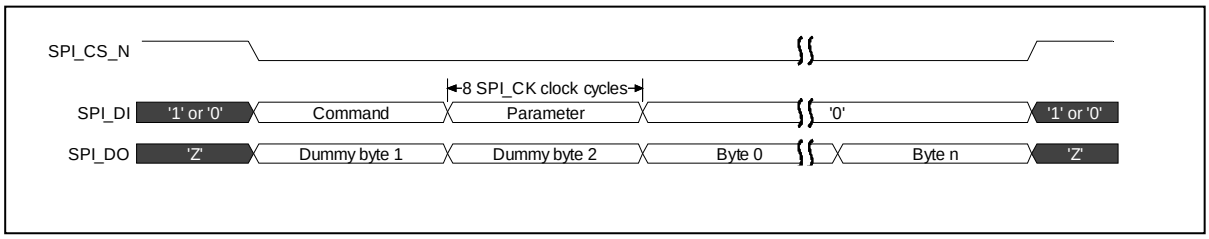


Figure 3
Applying an instruction with one or more return data.

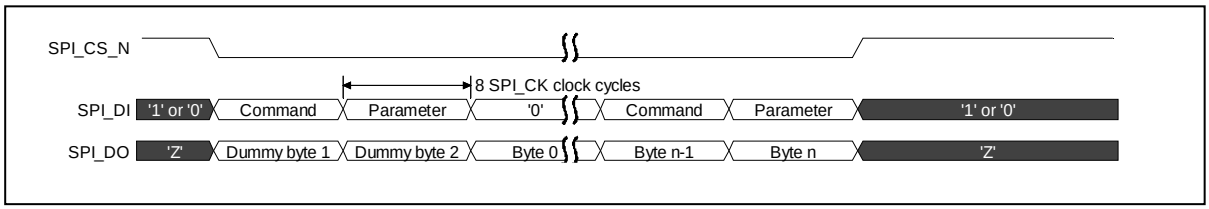


Figure 4
Terminating read by applying a new command.

Figure 4 shows the case where a new instruction stops the execution of the previous instruction.

The only difference between signals for the first and second instruction, is that during the first instruction SPI_DO holds dummy data during instruction and parameter entry, while SPI_DO continues to return data during the second instruction and parameter entry.

There are no restrictions on how many instructions, or which instruction, that can be entered during the same SPI_CS_N low period.

6.3 Parallel mode timing

Estimated values

SYMBOL	PARAMETER (CONDITION)	MIN	TYP	MAX	UNITS
f_{RD_N}	Frequency for RD_N signal	0	-	f_{CK}	MHz
f_{WR_N}	Frequency for WR_N signal	0	-	f_{CK}	MHz
t_{CRW}	Time from PIF_CS_N low to PIF_WR_N and PIF_RD_N high.	14	-	-	ns
t_{RWL}	Time for PIF_WR_N and PIF_RD_N low	14	-	-	ns
t_{RW}	Period for PIF_WR_N and PIF_RD_N signals	t_{CK}	-	-	ns
t_{RWH}	Time for PIF_WR_N and PIF_RD_N high	14	-	-	ns
t_{RWC}	Time from PIF_WR_N and PIF_RD_N high to PiF_CS_N high	0	-	-	ns
t_{WRW}	Time PIF_WR_N has to be high between instructions entries.	$4t_{CK}$	-	-	
t_{SUW}	Setup time for data written to ASIC	5	-	-	ns
t_{HW}	Hold time for data written to ASIC	5	-	-	ns
t_{SUR}	Delay from PIF_RD_N low to data valid, Z_{LOAD} = 10pF		-	10.5	ns
t_{HR}	Data valid time after RD_N high	0	-	-	ns
t_{WRRD}	Time from write pulse to read pulse.	$4t_{CK}$	-	-	ns
t_{RST_OFF}	Time from RST_N high to PIF_RD_N, PIF_WR_N or PIF_CS_N low.	30	-	-	ns

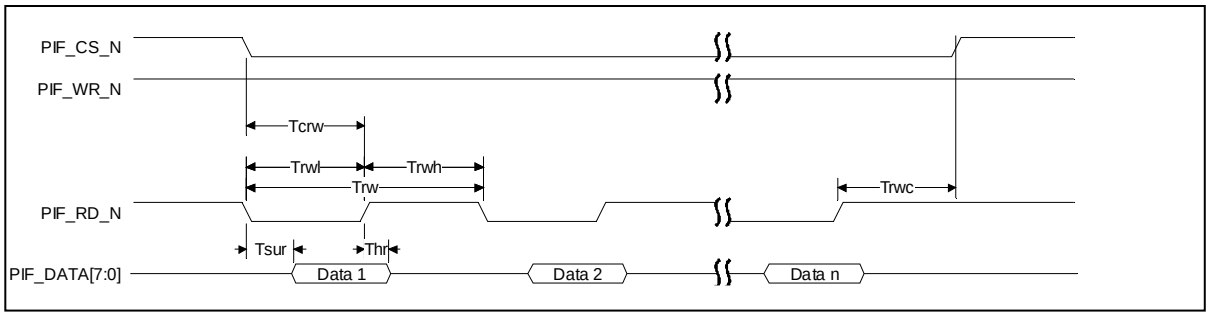


Figure 5
Timing for parallel read .

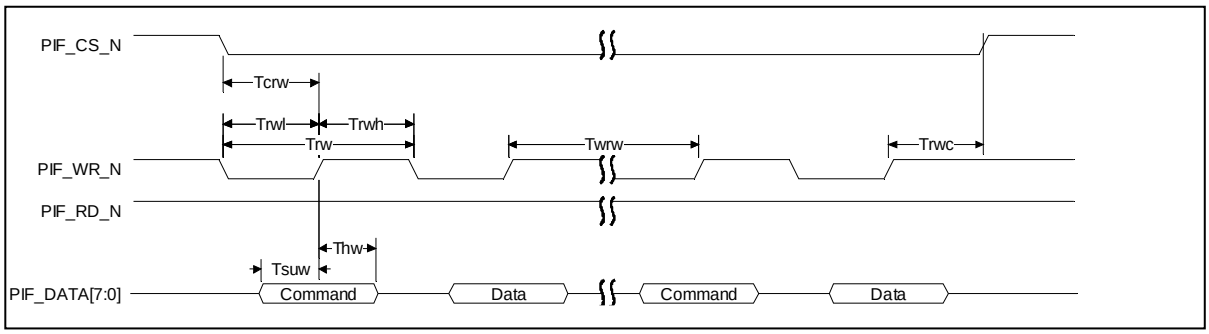


Figure 6
Timing for parallel write.

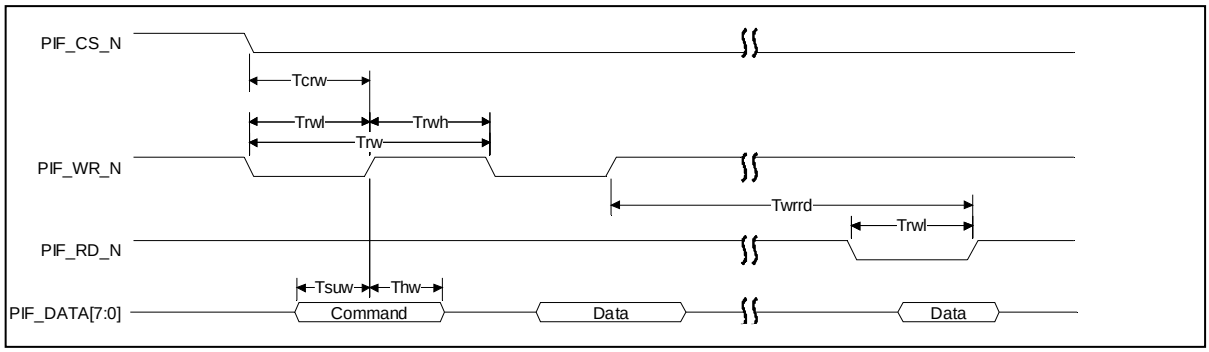
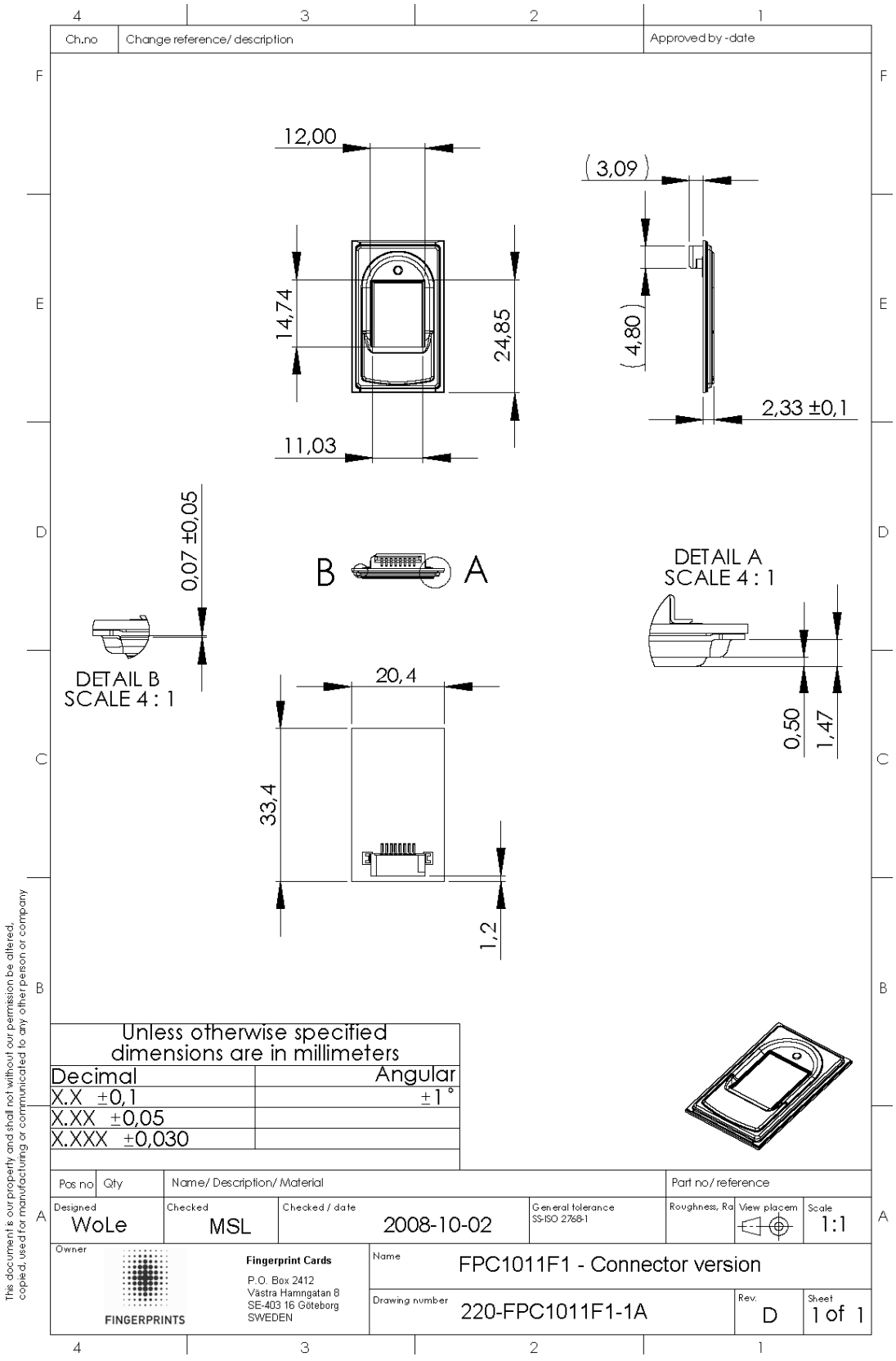


Figure 7
Delay from write to read in the parallel mode.

Both PIF_RD_N and PIF_CS_N have to be low for PIF_DATA to be defined as an output.

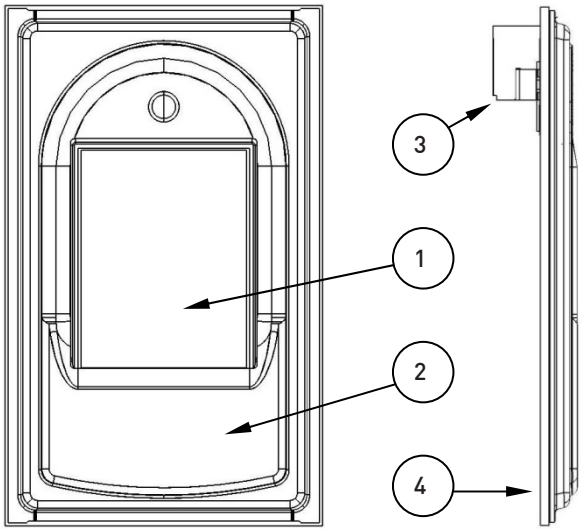
7 Mechanical properties

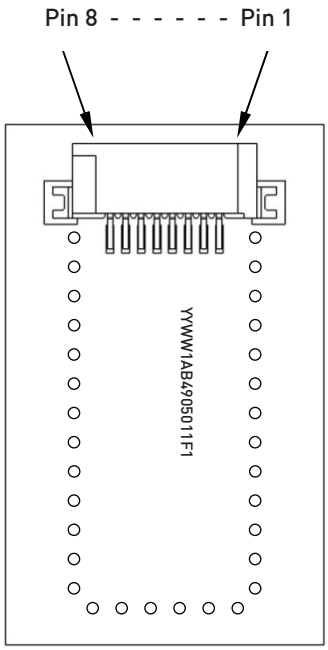
7.1 FPC1011F1 - part drawing



7.2 FPC1011F1 - pin configuration

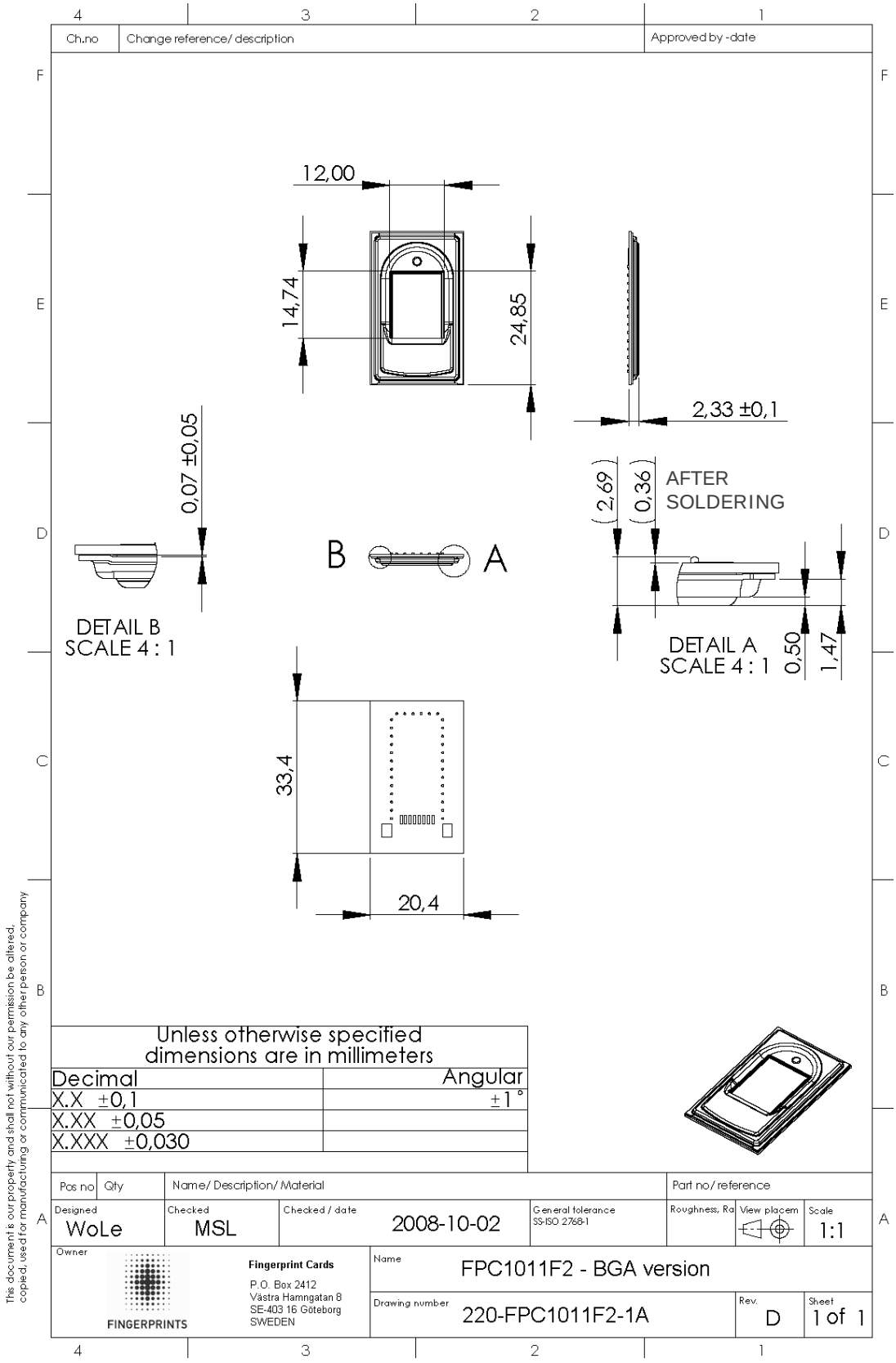
ITEM	DESCRIPTION
1	FPC1011 fingerprint area sensor chip
2	Drive electrode, called frame or bezel
3	Flex film connector: 8 pin, 1 mm pitch Molex / 0528520870 / low insertion force
4	BT substrate





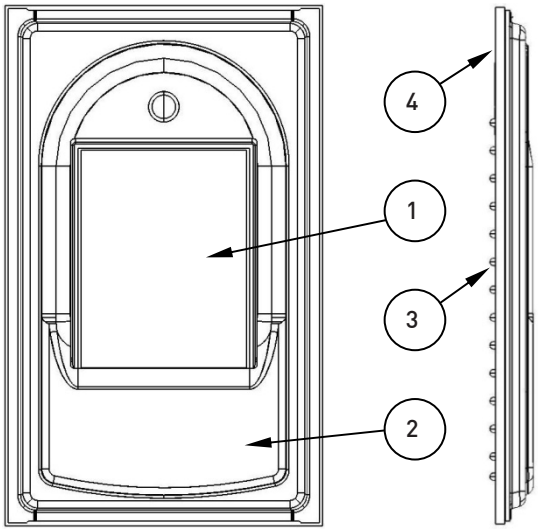
PIN	SIGNAL NAME	DESCRIPTION
1	SPI_DO	SPI data output. Tri state when SPI_CS_N is high.
2	VDD	Power supply, 2.5 or 3.3 V
3	RST_N	Reset, active low.
4	SPI_CK	SPI clock input. Internal pull down (system clock is connected to SPI clock internally).
5	GND	Signal ground
6	SPI_DI	SPI data input
7	SPI_CS_N	Chip select, active low. Resets the SPI interface when high.
8	ESD drain	ESD discharge path, connect to signal ground if no protective ground is accessible

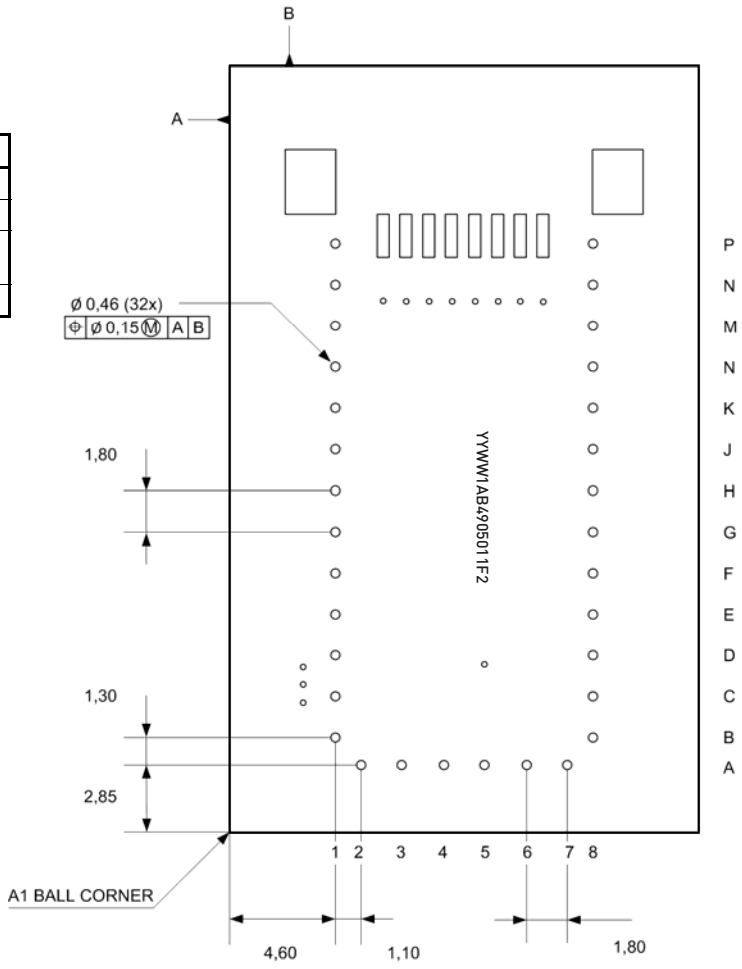
7.3 FPC1011F2 - part drawing



7.4 FPC1011F2 - pin configuration

ITEM	DESCRIPTION
1	FPC1011 fingerprint area sensor chip
2	Drive electrode, called frame or bezel
3	BGA solder balls: 32 pcs / Ø 0.46 mm (0.36 after soldering)
4	BT substrate





PIN	SIGNAL NAME	DESCRIPTION
P1	VSS	Signal ground
N1	AVDD [1]	Analog voltage supply
M1	PWRDN	Power down
L1	MODE	Interface selection pin
K1	-	Not used, leave open
J1	TEST [2]	Not used, connect to GND
H1	RST_N	Reset, active low
G1	ESD	ESD drain
F1	PIF_DATA1 [3]	Parallel data bus, DATA1
E1	PIF_DATA0 [3]	Parallel data bus, DATA0
D1	VSS	Signal ground
C1	PIF_WR_N	Write strobe, active low
B1	VDD	Voltage supply
A2	PIF_RD_N	Read strobe, active low
A3	PIF_CS_N	Chip select parallel mode
A4	SPI_CS_N	Chip select serial mode

PIN	SIGNAL NAME	DESCRIPTION
P8	VSS	Signal ground
N8	PIF_DATA2 [3]	Parallel data bus, DATA2
M8	PIF_DATA3 [3]	Parallel data bus, DATA3
L8	PIF_DATA4 [3]	Parallel data bus, DATA4
K8	PIF_DATA5 [3]	Parallel data bus, DATA5
J8	PIF_DATA6 [3]	Parallel data bus, DATA6
H8	PIF_DATA7 [3]	Parallel data bus, DATA7
G8	VSS	Signal ground
F8	SPI_CK	SPI clock input, internal pull down
E8	-	Not used, leave open
D8	TX1 [4]	Finger drive, connected to frame
C8	VSS	Signal ground
B8	CK	System clock
A7	IRQ_DA	Interrupt request, data available in FIFO
A6	SPI_DO [5]	SPI data output
A5	SPI_DI	SPI data input

Note 1: AVDD should be connected to VDD on receiving circuit board.
Note 2: TEST should be connected to GND, only used for production test.
Note 3: Bi-directional data bus. Output when PIF_CS_N and PIF_RD_N are low (active), otherwise input.
Note 4: Leave open, connected internally to the drive electrode (frame).
Note 5: Tri state when SPI_CS_N is high.

8 Cosmetic properties

8.1 Sensor surface quality

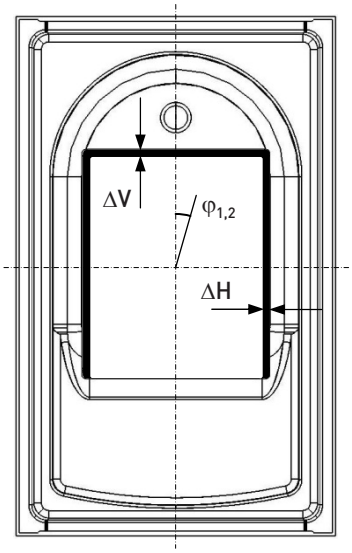
Minor defects not affecting the biometric performance are accepted.

This includes:

- Scratches not wider than 50 µm (0.05 mm).
- Spots, opaque or transparent, not larger than 2 pixels (0.01 mm^2).

8.2 Assembly accuracy

Relevant mechanical tolerances are specified in enclosed part drawings. Besides specified tolerances, variations in the die-to-frame assembly accuracy might occur.



Accepted variations are specified below.

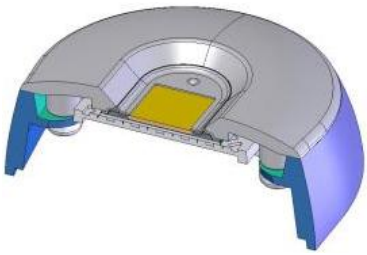
- Horizontal width (ΔH):	0,485 ± 0,200 mm
- Vertical width (ΔV):	0,545 ± 0,200 mm
- Die rotation (φ_1):	± 1,0 °
- Frame rotation (φ_2):	± 1,0 °

9 Application information

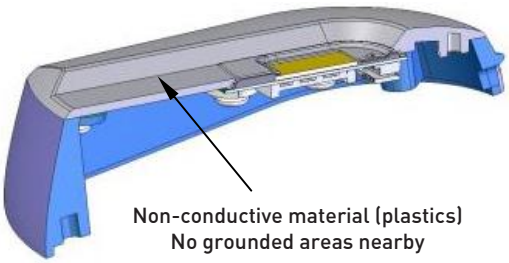
9.1 Sensor integration

Avoid galvanic contact

Thanks to the conductive frame, containing micro-ergonomics, a smooth transition to exterior mechanics can easily be obtained (example below).

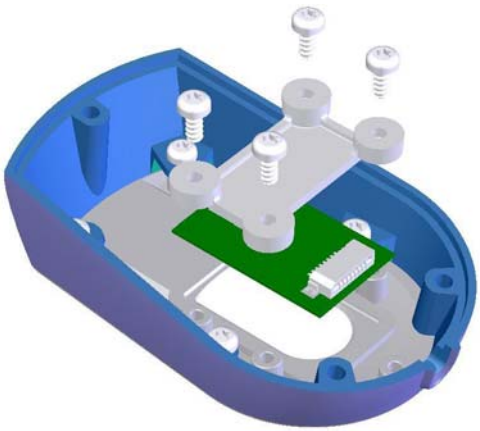


Note that the sensor and its drive electrode (frame) must be mounted in such way that electrical insulation to adjacent conductive surfaces is achieved. It is also recommended to avoid grounded surfaces nearby the drive electrode, since this might interfere with sensor operation.

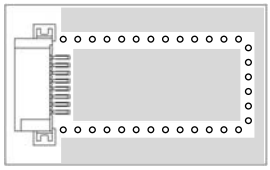


Proper mechanical support

The best way to ensure a solid sensor mount is to apply a stable, non-conductive, support to the backside of the sensor component.



On the FPC1011F1 package this non-conductive support can preferably be attached to the entire backside area, except for the connector.



Depending on application, the FPC1011F2 package may require a suitable “under fill, if sufficient external support is not offered. Mechanical force outside the maximum rating may permanently destroy the sensor product.

9.2 Sensor shut down mode

In software controlled authentication systems, where all capture image tasks are initiated by software it is recommended to disconnect the power supply when sensor is not in use. This procedure will improve life time and overall reliability. All communication signals should also be set to low (GND) to avoid feeding the CMOS circuitry through the I/Os. This especially applies to active low signals.

Stand by procedure for FPC1011F1:

1. Disconnect sensor power supply VDD.
   Indicated as switch S10 in the reference layout.
2. Set SPI communication pins low.
   (SPI_DO, SPI_DI, SPI_CK)
3. Set SPI_CS_N and RST_N low.

Stand by procedure for FPC1011F2:

1. Disconnect sensor power supply VDD and AVDD.
   Indicated as switch S10 in the reference layout.
2. Set SPI communication pins low.
   (SPI_DO, SPI_DI, SPI_CK)
3. Set PIF communication pins low.
   (PIF_DATA0-7, PIF_RD_N, PIF_WR_N)
4. Set general signal pins low.
   (CK, MODE, PWRDN)
5. Set chip select and reset low.
   (SPI_CS_N, PIF_CS_N and RST_N

The start-up procedure is the reverse.

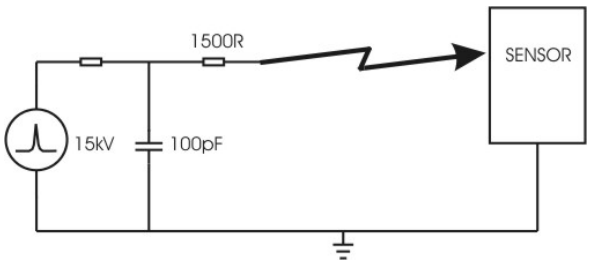
9.3 ESD protection

The importance of ESD protection
To generate an image, capacitive fingerprint sensors require a finger to be in contact with the sensor surface. This will expose all capacitive sensors to severe ESD discharges, as they usually are the "first point of contact". ESD discharge voltages are often under-estimated and the actual voltage levels may be surprisingly high. Discharges in the 1 to 2 kV range will typically not even be noticed, i.e. felt in the finger.

All sensors from Fingerprint Cards incorporate extensive internal ESD protection for all accessible front surfaces. The protection level is well in excess of 15kV using a standard Human Body Model discharge.

Human Body Model
The Human Body Model consists of a 100 pF capacitor, which simulates the capacitance between body and ground. This capacitor is charged to a test voltage. The resistance of the finger and skin is approximated by a 1500 ohm series resistor. The discharge will have a time constant of, 100pF x 1500 ohm = 150 nS. For a 15 kV discharge the peak current would be 15kV/1500 = 10A.

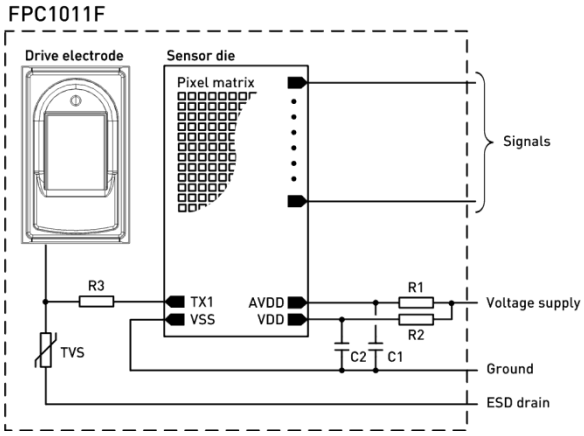
Although the ESD-specification is given as a voltage level it is important to realize that an ESD test is more of a current discharge test.



Human Body Model

Internal sensor protection
ESD discharge issues are best illustrated by considering the simplified internal schematic in the figure below.

Sensors from FPC have a robust sensor surface coating, which will deflect discharges to the sensor drive electrode (frame). From the electrode, the discharge current will be conducted via the Transient Voltage Suppressor (TVS) to the local ESD drain node. The voltage at the drive electrode is thereby limited. The 100 ohm resistor will limit the current towards the sensor chip to very safe levels.



Sensor internal schematic

Voltages induced by the ESD current
In a simplified model, two currents occur during an ESD event - the main ESD current flowing through the TVS to the sensor ESD drain, and the much smaller current flowing through the 100 ohm resistor back into sensor chip input protection.

The current flow through the 100 ohm resistor will depend on the clamping voltage over the TVS. A 15kV discharge will generate a 200 mA current pulse into the chip protection diodes, well within the chip ESD rating. The duration of the pulse will be in the order of 600nS. After this time the current will decay exponentially. The charge through the protection diode can be estimated to 0.15 nC.

Sensor cable extensions
When using longer sensor cable lengths, the electromagnetic coupling between the current in the ESD drain connection and other signal and supply connections need to be considered.

This coupling is rather complicated and will depend on the cable geometry. With the standard, short connection between the sensor and the receiving electronics, these effects are not significant and can be ignored.

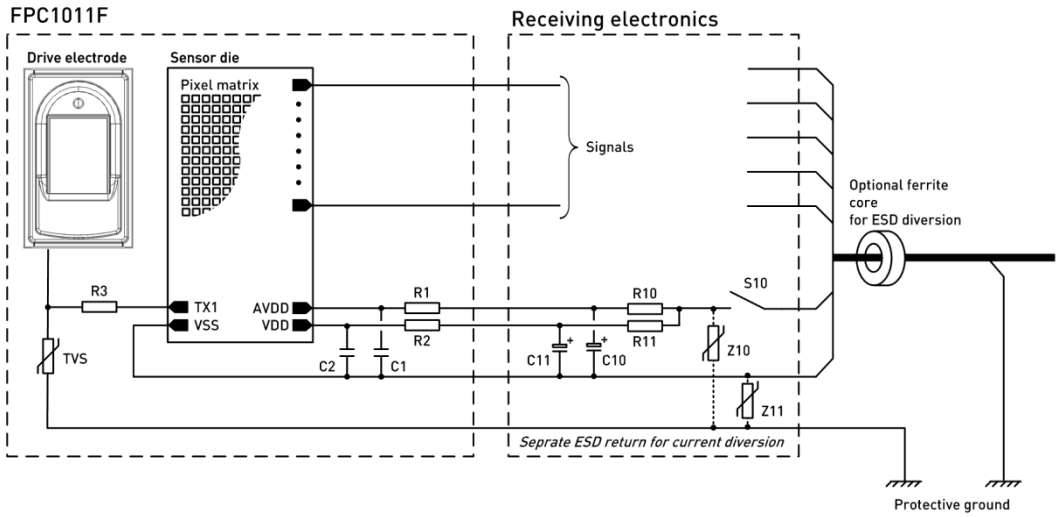
Longer cable lengths between sensor and the receiving electronics can in some cases be acceptable. Exact guidelines are not possible since the ESD effects will depend on the actual installation but up to 0.2 meter would in general not cause any problems.

Extensions will also affect signal fidelity and the digital waveforms need to be checked for adverse reflections. Problems with ringing become more evident as the length increases. At 1 m the ringing will cause waveforms that are questionable.

Minimizing effects on downstream electronics
The ESD pulse will continue past the sensor connection and spread into the receiving electronics ground plane and most likely further on to a "protective earth" ground via a connecting cable. This connection will often have considerable length and hence potential ESD problems.

To help alleviate the risk of electromagnetic coupling a separate ESD return to divert the ESD current to some "suitable" point is recommended. One way to prevent problems with stray currents due to the dual ground path, is to front the separate ESD return with a TVS in order to break this current path at low voltages while allowing the ESD pulse to pass freely.

Even higher ESD diversion can be achieved by also increasing the inductance of the signal cable connection from the receiving electronics. The common mode inductance forms a "barrier" to help steer the ESD current over to the separate ESD return. One of the easiest means is to mount an EMI ferrite core on the cable near the electronics.



Recommended ESD precaution in application / External TVS (e.g. Transguard VC060309A200, www.avx.com)

9.4 FPC1011F1 - reference layout

The FPC1011F1 sensor component is internally preset for serial communication. Number of signals is reduced in order to obtain a narrow 8 pin flex connector interface.

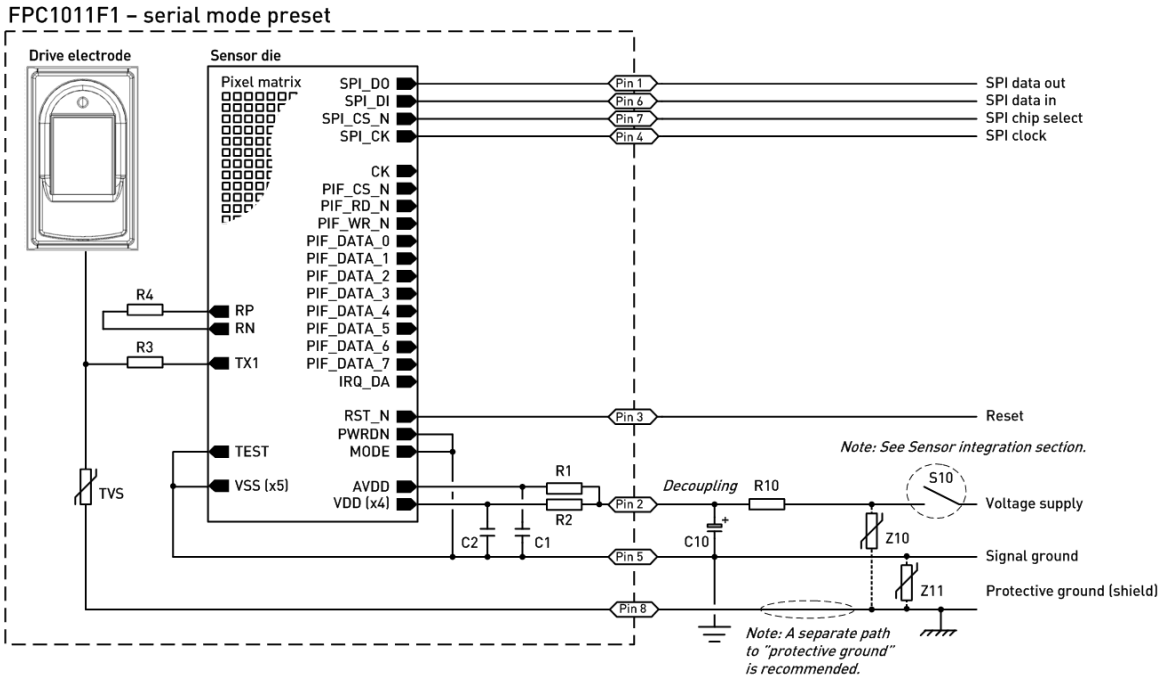
The SPI communication has already been covered in the *Serial mode* section of this document and the detailed pin configuration is available in the *FPC1011F1-Pin configuration* section.

Depending on the overall quality of the connected power supply, i.e. noise, different filter/decoupling circuitries may be necessary.

In normal cases a standard buffer capacitor of 5-10µF is enough. In case of a noisy environment, other types of filtering may be required to obtain optimal performance.

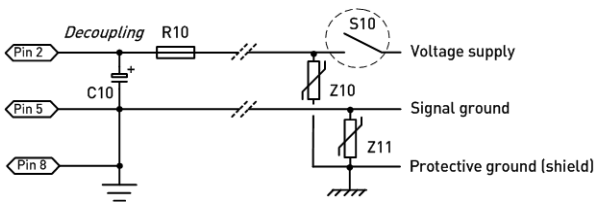
Although the sensor is specified for a voltage supply range between 2.5 - 3.3 volts, different protection and decoupling circuitries may be necessary to reach full SPI communication speed.

Please note that the reference layout is only an example and is not guaranteed to be the best implementation for all applications. It is also recommended to carefully read the *Sensor integration* section.

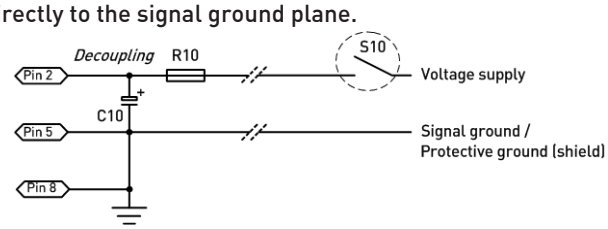


FPC1011F1 reference schematics - serial communication

It is always recommended to connect the separate ESD discharge path (pin 8 or G1) directly to a protective ground/shield node. If a separate ESD return is not possible, voltage suppressors can be added at the ground plane connection to divert high discharge currents from sensitive electronics.
The very last and "worst" alternative, without any ESD current diversion, is to connect the ESD return directly to the signal ground plane.



Discharge path is connected using current diversion



Discharge path is connected directly to signal ground

9.5 FPC1011F2 - reference layout

FPC1011F2, serial mode

The FPC1011F2 sensor component offers both a serial SPI interface and parallel asynchronous interface. Communication interface is easily selected by means of a separate mode pin.

In order to activate parallel mode, connect the MODE pin to GND.

The SPI communication has already been covered in the *Serial mode* section of this document and the detailed pin configuration is available in the *FPC1011F2-Pin configuration* section.

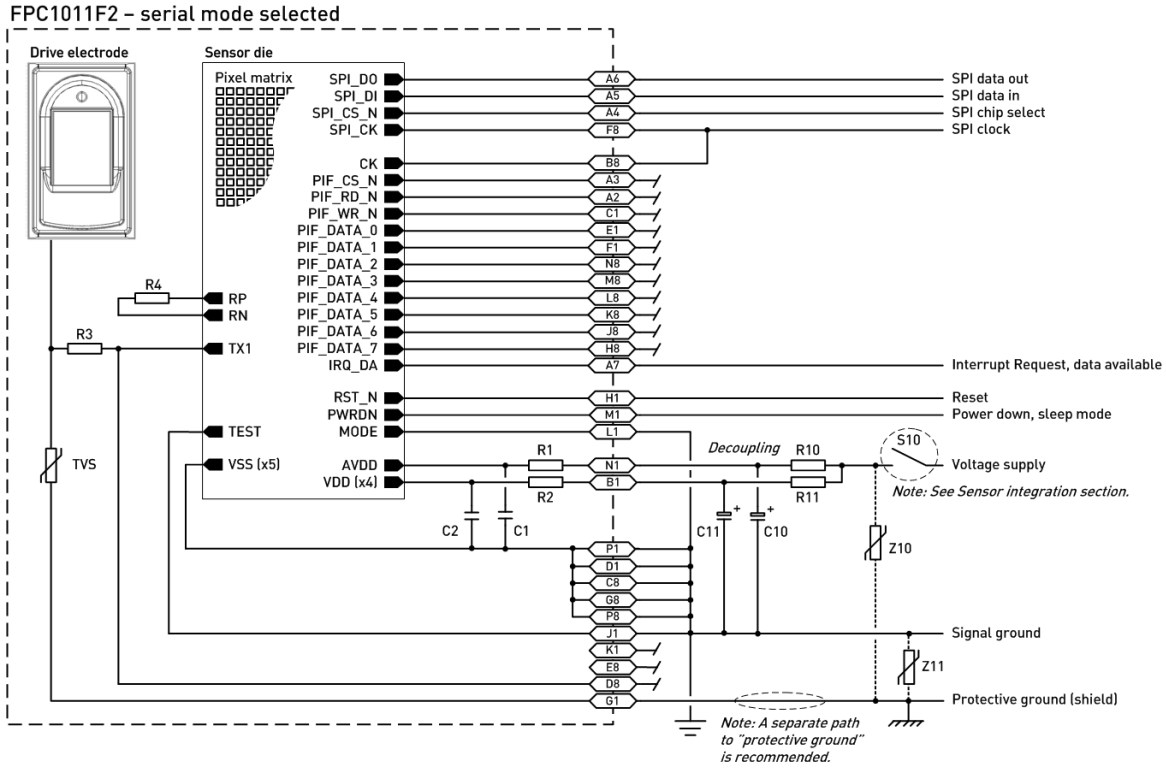
Depending on the overall quality of the connected power supply, i.e. noise, different filter/decoupling circuitries may be necessary. In normal cases a standard buffer capacitor of 5-10µF is enough.

In case of a noisy environment, other types of filtering may be required to obtain optimal performance.

Although the sensor is specified for a voltage supply range between 2.5 - 3.3 volts, different protection and decoupling circuitries may be necessary to reach full SPI communication speed.

Regarding the separate ESD discharge path, please see the *FPC1011F1 - reference layout* for details.

Please note that the reference layout is only an example and is not guaranteed to be the best implementation for all applications. It is also recommended to carefully read the *Sensor integration* section.



FPC1011F2 reference schematics - serial communication

FPC1011F2, parallel mode

The FPC1011F2 sensor component offers both a serial SPI interface and parallel asynchronous interface. Communication interface is easily selected by means of a separate mode pin.

In order to activate parallel mode, connect the MODE pin to VDD.

The parallel communication has already been covered in the *Parallel mode* section of this document and the detailed pin configuration is available in the *FPC1011F2-Pin configuration* section.

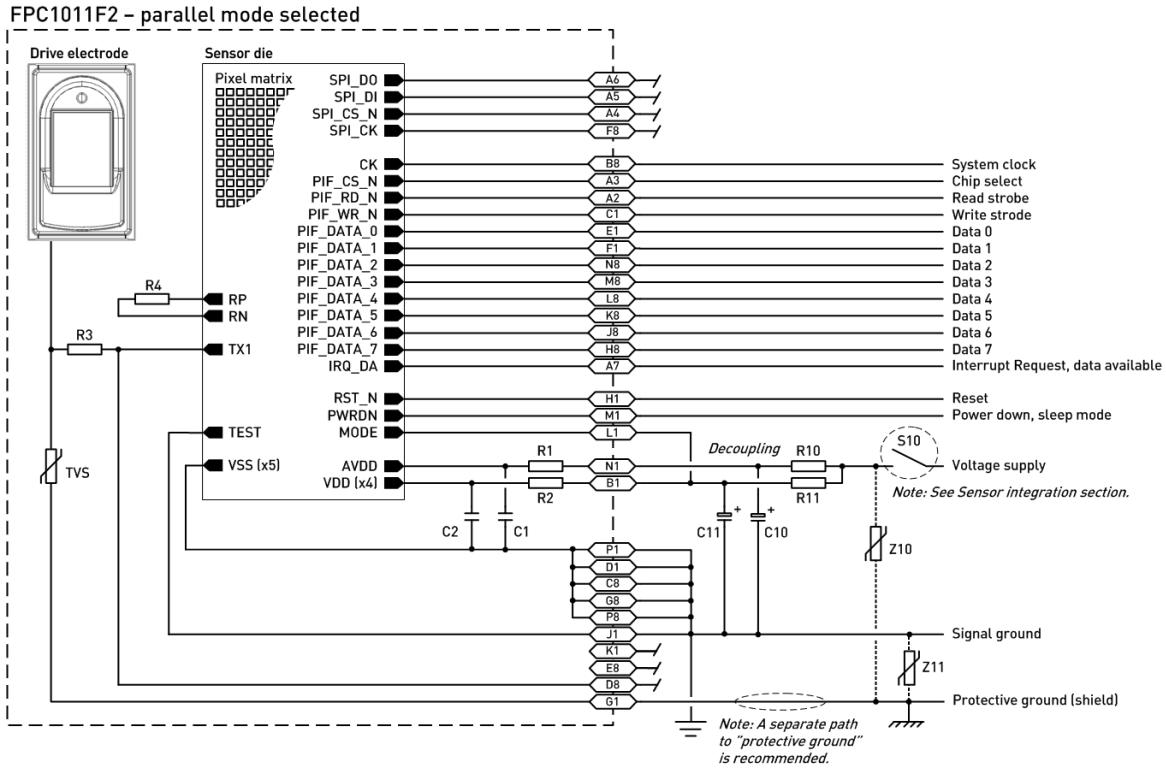
Depending on the overall quality of the connected power supply, i.e. noise, different filter/decoupling circuitries may be necessary. In normal cases a standard buffer capacitor of 5-10µF is enough.

In case of a noisy environment, other types of filtering may be required to obtain optimal performance.

Although the sensor is specified for a voltage supply range between 2.5 - 3.3 volts, different protection and decoupling circuitries may be necessary to reach full SPI communication speed.

Regarding the separate ESD discharge path, please see the *FPC1011F1 - reference layout* for details.

Please note that the reference layout is only an example and is not guaranteed to be the best implementation for all applications. It is also recommended to carefully read the *Sensor integration* section.



FPC1011F2 reference schematics - parallel communication

9.6 FPC1011F1 - mating flex strip

FPC1011F1 is prepared for a standard 8-pin flex cable and thus provided with a standard low insertion force type of connector (0528520870).

There are several flex cable brands available and many of them will probably perform well. It is also possible to manufacture a custom design flex. Normally this type of flex is much easier to bend and is also possible to shape to fit the application entirely.

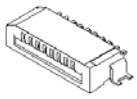
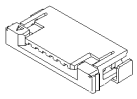
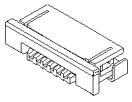
Below four different connector configurations, a standard type of flex and a custom design type of flex are presented.

The custom design flex cable is available from Fingerprint Cards in low volumes (samples). Volume orders can be placed directly with the supplier in Taiwan.

Mating connector data (examples):

Supplier: Molex (www.molex.com)

Part number:

	Non-ZIF	ZIF
Top side connector	*0527930870* 	*0522070860* 
Bottom side connector	*0528520870* 	*0522710869* 

Top or bottom side configuration is selected to fit a particular application.

Description: 1.00mm (.039") Pitch
FFC/FPC Connector,
SMT, Right Angle,
8 Circuits, Lead-free

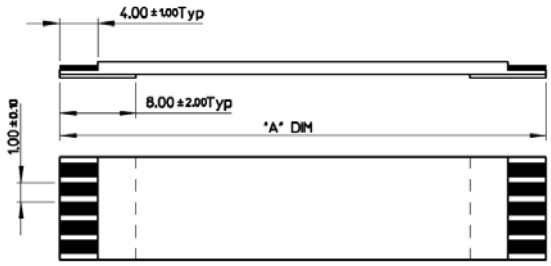
Standard type of flex cable (example):

Supplier: Molex (www.molex.com)

Part number: 0210390227 (Standard type)
0982670227 (High temperature)

Description: 1.00mm (.039") Pitch
Premo-Flex™ FFC Jumper,
Same Side Contacts (Type A),
8 Circuits,
76.00mm (3.000") Length

Additional: Other lengths are available

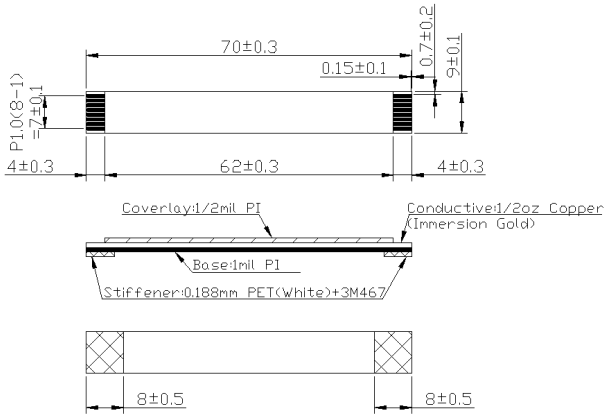


Custom design type of flex cable, typical data:

Part number: FPC5207

Description: Soft flex, 1.00mm Pitch
Same Side Contacts, 8 Circuits
70 mm Length, 0.2 mm Thickness

Additional: Minimum bend radius
- Static application 0.3 mm
- Dynamic application 1.5 mm



PRELIMINARY

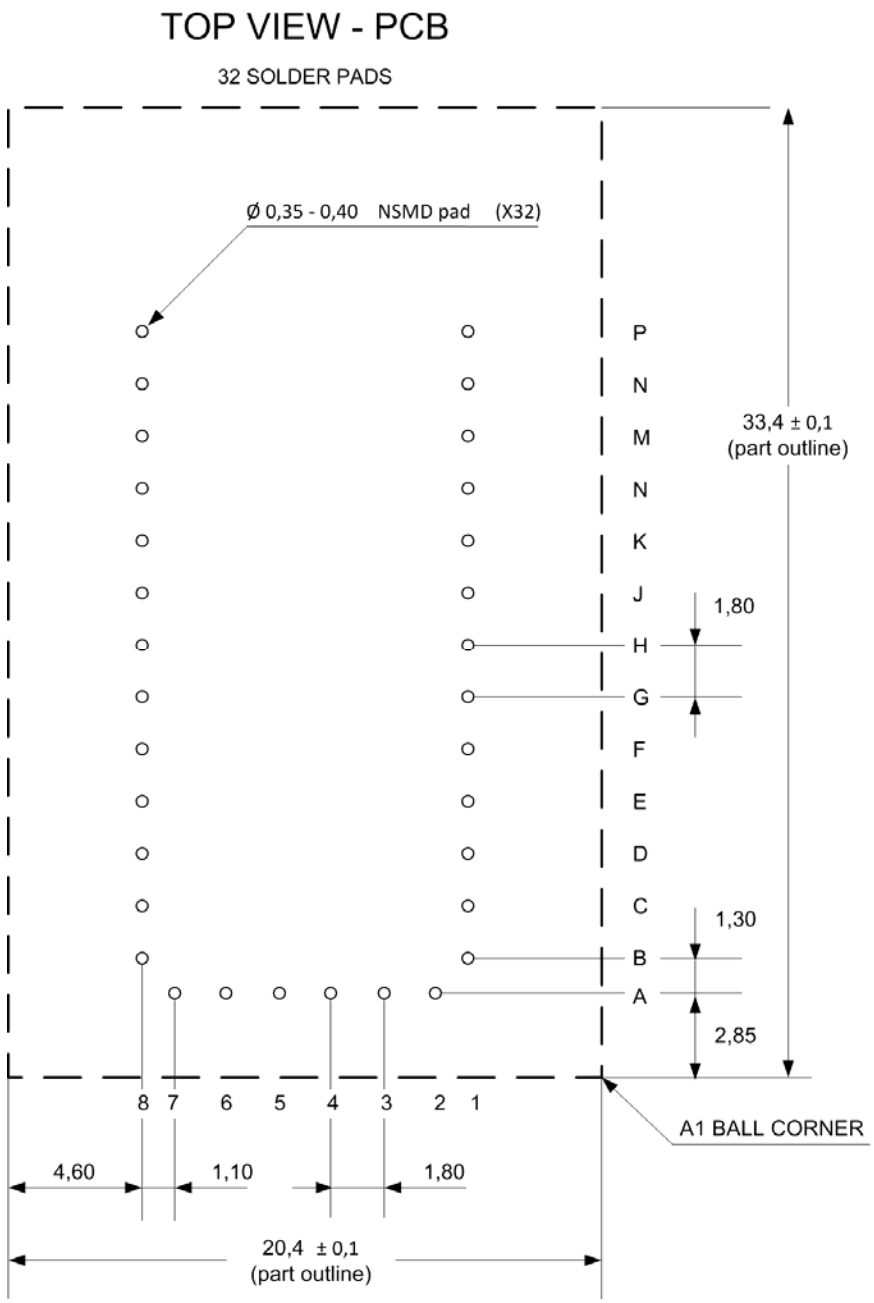
9.7 FPC1011F2 - PCB layout pattern

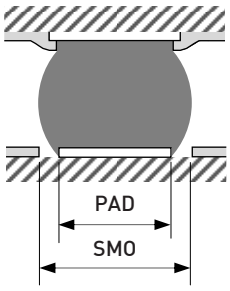
The FPC1011F2 sensor is provided with 32 solder balls, allowing access to both the serial interface (SPI) and the asynchronous parallel interface (PIF). Besides the communication interfaces, a number of setup signals are also available. For details refer to the *FPC1011F2-pin configuration* section.

Solder pads should be NSMD (non-solder-mask-defined) and the vertical and horizontal pitch is 1,80 mm.

Recommended PCB design parameters:

- Pad layout:	NSMD
- Pad size (PAD):	0,35 - 0,40 mm
- Solder mask opening (SMO):	0,45 - 0,50 mm
- Ball size before soldering:	0,46 mm
- Ball size after soldering:	0,36 mm

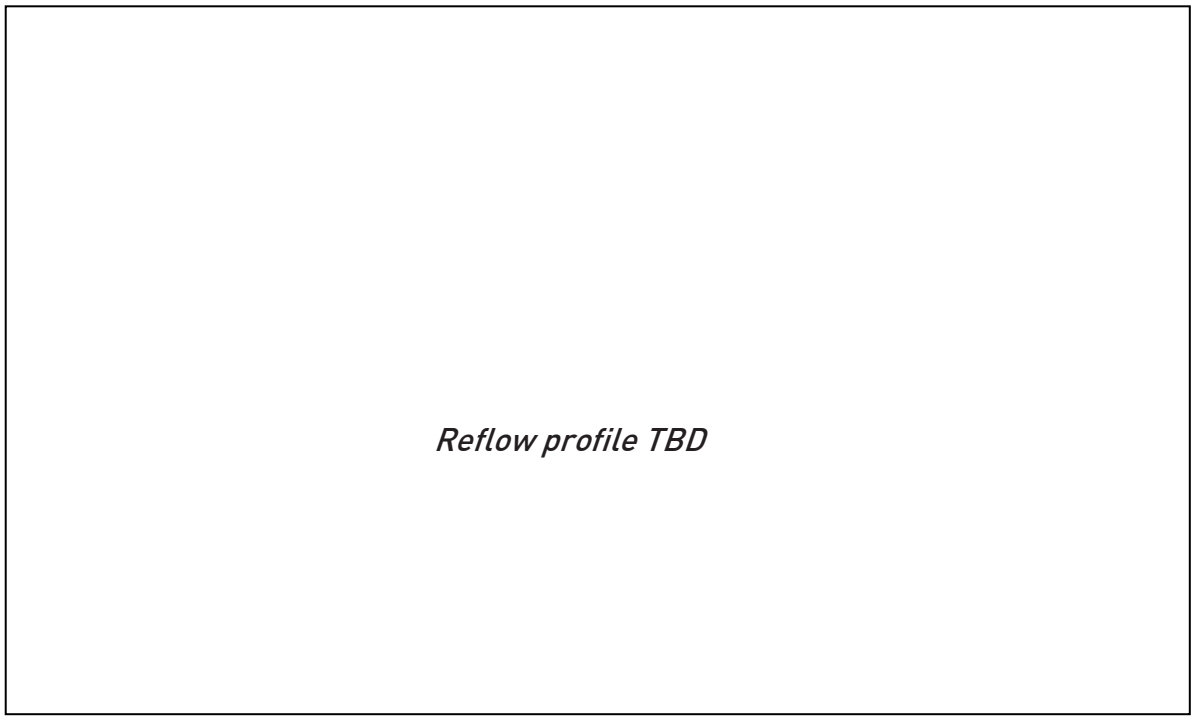




PRELIMINARY

9.8 FPC1011F2 - reflow soldering profile

The BGA version of the FPC1011F sensor is adapted for a standard SMT reflow process.



FPC1011F2 - Recommended reflow soldering profile

10 Order information

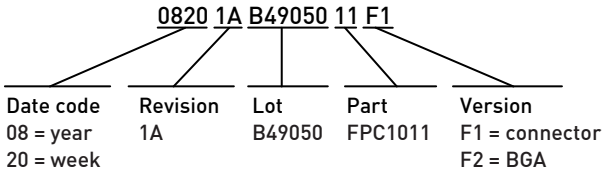
10.1 Part numbers

Part number:	FPC1011F1
Description:	Area sensor with FLEX connector type of package
Minimum Order Quantity (MOQ):	200

Part number:	FPC1011F2
Description:	Area sensor with BGA type of package
Minimum Order Quantity (MOQ):	200

10.2 Production codes

All parts are laser marked on the backside with a unique production code (1.5 x 8 mm). This code comprises information about production date, revision, production lot, part number and version.



10.3 Package information

Products are supplied in ESD safe, standard JEDEC trays, 40 sensor units per tray.

Five trays and one lid are stacked, wrapped and packed in an ESD safe bag.

Exterior cardboard box is marked, text and barcode (code 39), with necessary product information; part number, lot number, date code (yyww) and quantity.

10.4 ESD sensitivity

Electrostatically sensitive device. Ensure proper handling during device assembly.

11 Document revision history

REVISION	DATE	CHANGE	AUTHOR	APPROVED
A	2008-03-03	First preliminary release	MSL	PSV
B	2008-06-26	Second preliminary release	MSL	PSV
C	2008-09-04	Final release	MSL	PSV
D	2008-11-06	FPC1011F2 info added, general updates	MSL	PSV

12 Contact information

Main office
Fingerprint Cards AB
P.O. Box 2412
SE-403 16 Göteborg
Sweden

Visiting address
Västra Hamngatan 8

Telephone
+46 (0)31 60 78 20

Fax
+46 (0)31 13 73 85

Web site
www.fingerprints.com

E-mail
sales@fingerprints.com
tech@fingerprints.com