

FPD87392BXB

+3.3V TFT-LCD Timing Controller with Dual LVDS Inputs/Dual RSDS™ Outputs for TFT-LCD Monitor and Notebook (SXGA/SXGA+/UXGA)

General Description

The FPD87392BXB Panel Timing Controller is an integrated FPD-Link + RSDS™ + TFT-LCD Timing Controller. The logic architecture is implemented using standard and default timing controller functionality based on an Embedded Gate Array. The device is reconfigurable to the needs of a specific application by providing user-defined specifications or customer supplied VHDL/Verilog code.

The FPD87392BXB is a timing controller that combines an LVDS dual pixel input interface with National's Reduced Swing Differential Signaling (RSDS™) output column driver interface for SXGA, SXGA+ and UXGA resolutions. It resides on the TFT-LCD panel and provides the data buffering and control signal generation. The RSDS™ data path to the column driver contributes toward lowering radiated EMI and reduced system dynamic power consumption. The RSDS™ dual 12 pair differential bus conveys up to 24-bit color data for SXGA/SXGA+/UXGA panels when using VESA 60Hz standard timing.

Features

- Input frequency range from 25 MHz to 85 MHz
- Support display resolutions SXGA (1280x1024), SXGA+ (1400x1050) and UXGA (1600x1200)
- Embedded gate array for custom panel timing
- RSDS™ (Reduced Swing Differential Signaling) Column Driver bus for low power and reduced EMI
- Drives RSDS™ column driver up to 170 Mb/s with an 85 MHz clock
- 6 or 8 bit LVDS dual pixel input interface (FPD-Link)
- Virtual 8-bit color depth in FRC mode
- Flexible RSDS™ data output mapping for Bottom or Top mount
- Supports 1 and 2 line inversion mode for RVS output
- Supports Graphics Controllers with spread spectrum interface for lower EMI
- Free Run Mode Function
- Fail-safe function in DE mode (Bonding Option)
- Supports DE mode and SYNC only mode (Bonding Option)
- Power-On-Reset Support
- CMOS circuitry operates from a 3.0V to 3.6V supply
- 128 TQFP package with body size 14mm x 14mm x 1.0mm, 0.4mm Pitch

System Diagram

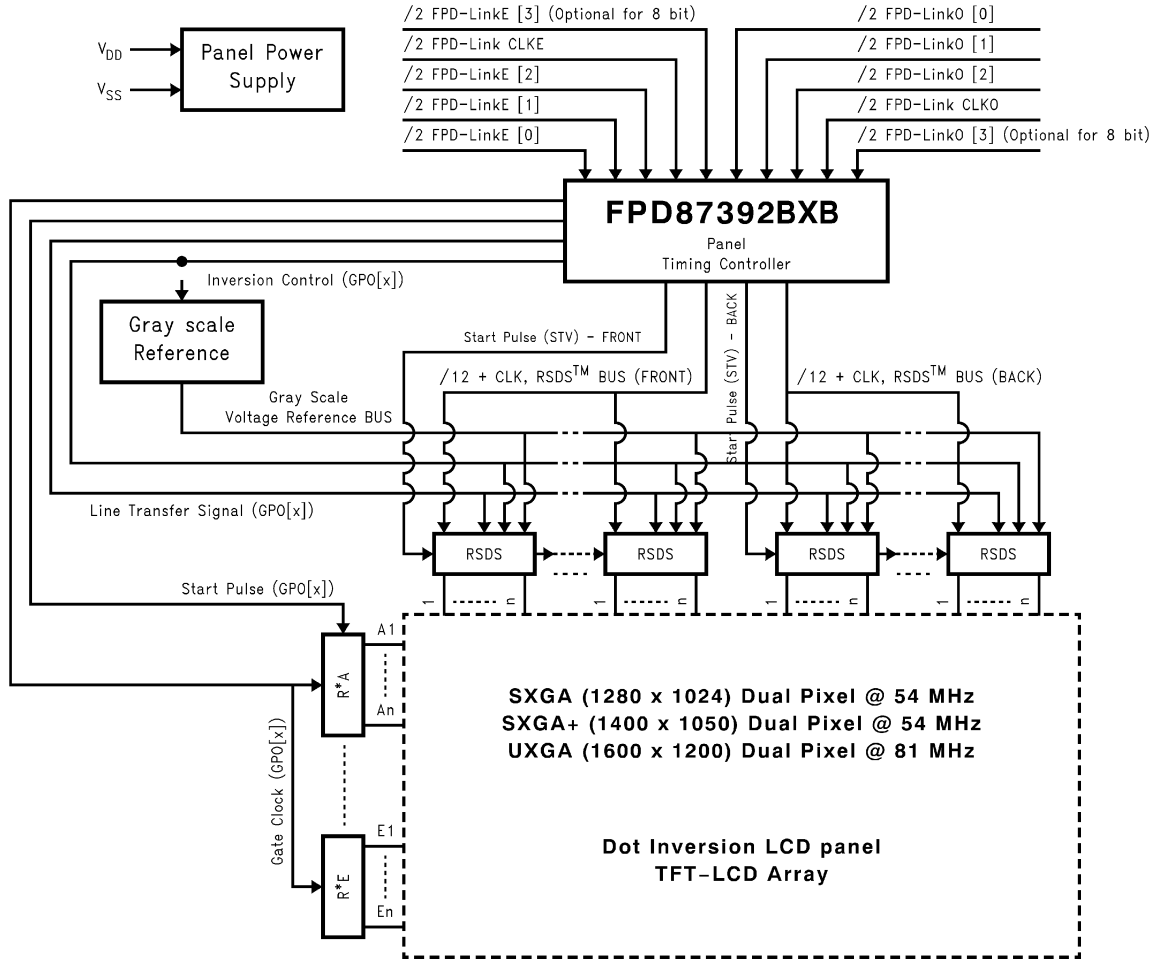
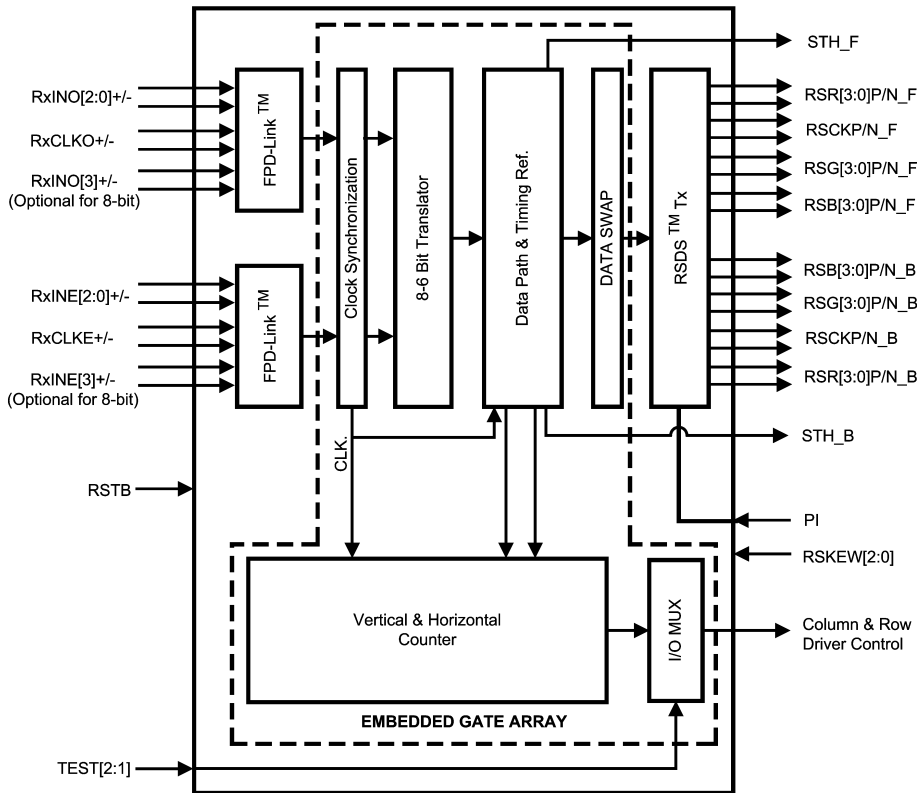


FIGURE 1. Block Diagram of the LCD Module

Block Diagram



20104328

FIGURE 2. Block Diagram

Functional Description

DUAL FPD-LINK RECEIVERS

The LVDS based FPD-Link Receivers inputs video data and control timing through 8 pairs of LVDS channels plus 2 pairs of LVDS clocks to provide 24-bit color or use only 6 pairs of LVDS channels plus 2 LVDS clocks to provide 18-bit color. The video data is converted to a parallel data stream and routed to the 8-6 bit translator.

SPREAD SPECTRUM SUPPORT

The FPD-Link receiver supports graphics controllers with Spread Spectrum interfaces for reducing EMI. The Spread Spectrum methods supported are Center and Down Spread. A maximum of 2% total is supported at a frequency modulation of 100kHz maximum.

8-6 BIT TRANSLATOR

8-bit data is reduced to a 6-bit data path via a time multiplexed dithering technique or simple truncation of the LSBs. This function is enabled via the input control pins.

DATAPATH BLOCK AND RSDS TRANSMITTER

6(8)-bit video data (RGB) is input to the Datapath Block supports up to an 85 MHz dual pixel rate. The data is delayed to align the Column Driver Start Pulse (STH) with the Column Driver data. The dual data bus (RSR[3:0]P/N, RSG[3:0]P/N, RSB[3:0]P/N) outputs at a 170 MHz rate on 24 differential output channels. The clock is output on the

(Front, Back) RSCKP/N differential pairs. The RSDS Column Drivers latch data on both positive and negative edges of the clock. The swap function provides flexible RSDS data output mappings for either Top or Bottom mount. The RSDS output setup/hold timings are also adjustable through the RSKEW[2:0] input pins.

TIMING CONTROL FUNCTION

The Timing Control function generates control to Column Drivers, Row Drivers, and power supply. The GPOs (General Purpose Outputs) provide for CD latch pulse, REV, and Row Driver control generation. The General Purpose Outputs allow the user to generate control anywhere within the frame data. Standard Row Driver interface or Custom Row Driver interfaces can be implemented with the GPOs (General Purpose Outputs).

RSDS OUTPUT VOLTAGE CONTROL

The RSDS output voltage swing is controlled through an external load resistor connected to the RPI pin. The RSDS output signal levels can be adjusted to suit the particular application. This is dependent on overall LCD module design characteristics such as trace impedance, termination, etc. The RSDS output voltage is inversely related to the RPI value. Lower RPI values will increase the RSDS output voltage swing and consequently overall power consumption will also increase.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Rating:

($C_{ZAP} = 120 \text{ pF}$,
 $R_{ZAP} = 1500\Omega$)

MM = 200V,
 HBM = 2000V

| | |
|--|------------------------------|
| Supply Voltage (V_{DD}) | -0.3V to +4.0V |
| DC TTL Input Voltage (V_{IN}) | -0.3V to ($V_{DD} + 0.3V$) |
| DC LVDS Input Voltage (V_{IN}) | -0.3V to ($V_{DD} + 0.3V$) |
| DC Output Voltage (V_{OUT}) | -0.3V to ($V_{DD} + 0.3V$) |
| Junction Temperature | +150°C |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Lead Temperature (T_L) (Soldering 10 sec.) | 260°C |

Operating Conditions

| | Min | Max | Units |
|---------------------------------|-----|-----|------------------|
| Supply Voltage (V_{DD}) | 3.0 | 3.6 | V |
| Operating Temp. Range (T_A) | 0 | 70 | °C |
| Supply Noise Voltage | | 100 | mV _{PP} |

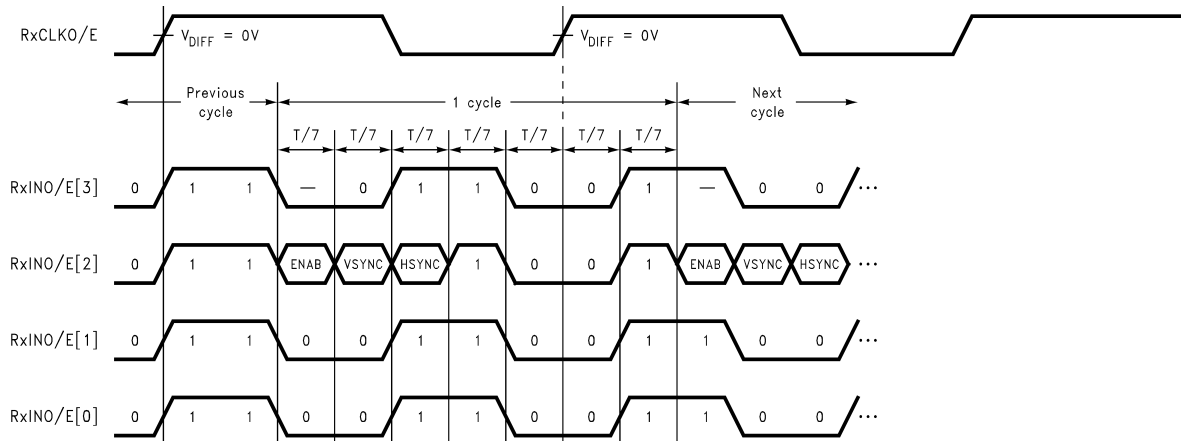
DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.0V$ to $3.6V$, $I_{PI} = 100 \mu\text{A}$ (Unless otherwise specified)

TTL DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------|----------------------------|--|----------------|---|---|---------------|
| V_{DD} | Core Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| V_{IH} | Minimum Input High Voltage | | 2.0 | | | V |
| V_{IL} | Maximum Input Low Voltage | | | | 0.8 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -8\text{mA}$ | $V_{DD} - 0.6$ | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 8 \text{ mA}$ | | | 0.4 | V |
| I_{IN} | Input Current | $V_{IN} = V_{DD}, \text{GND}$ | | | ± 10 | μA |
| I_{PU} | Pull-Up Current | $V_{DD} = 3.3V, V_{IN} = V_{DD}$ | | | -50 | μA |
| I_{PD} | Pull-Down Current | $V_{DD} = 3.3V, V_{IN} = \text{GND}$ | | | +50 | μA |
| I_{DD} | Average Supply Current | $C_{L(TTL)} = 15 \text{ pF}$, $R_{L(RSDS)} = 100\Omega$ and $C_{L(RSDS)} = 5 \text{ pF}$ (jig & test fixture capacitance), $I_{PI} = 100 \mu\text{A}$ (Typically PI pin connected to 13 k Ω to ground), See Figure 3 for input conditions | | 170 (CLK = 65 MHz, $V_{DD} = 3.3V$) | 250 (CLK = 85 MHz, $V_{DD} = 3.6V$) | mA |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.



20104302

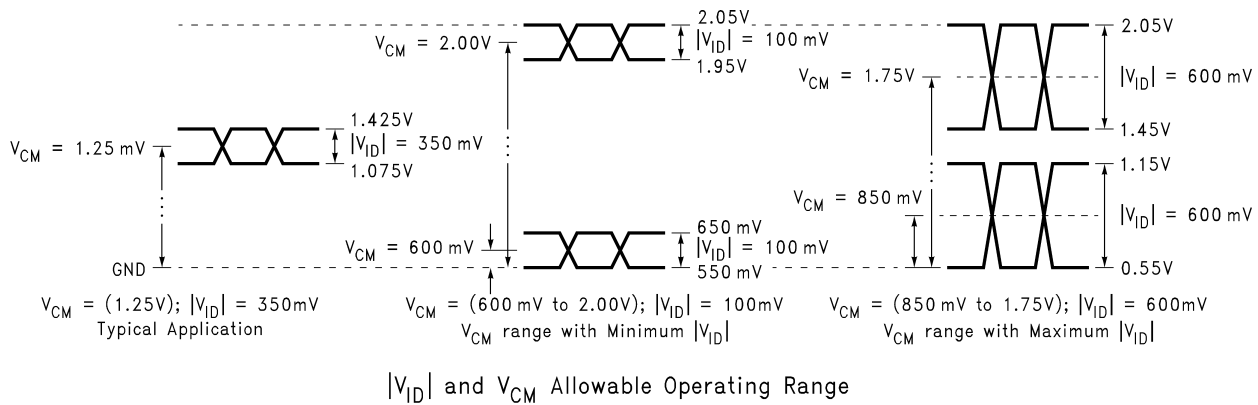
FIGURE 3. FPD-Link Receiver Input Pattern Used to Measure I_{DD}

DC Electrical Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)

FPD-Link (LVDS) Receiver Input Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|--|---------------------|-----|---------------------|---------------|
| LVDS RECEIVER DC SPECIFICATIONS | | | | | | |
| Note: LVDS Receiver DC parameters are measured under static and steady state conditions which may not reflect the actual performance in the end application. | | | | | | |
| V_{THLVDS} | Differential Input High Threshold Voltage | $V_{CM} = 1.2\text{V}$ | | | +100 | mV |
| V_{TLVDS} | Differential Input Low Threshold Voltage | | -100 | | | mV |
| I_{IN} | Input Current | $V_{IN} = 2.05\text{V}$, $V_{DD} = 3.6\text{V}$ | | | ± 10 | μA |
| | | $V_{IN} = 0.55\text{V}$, $V_{DD} = 3.6\text{V}$ | | | ± 10 | μA |
| V_{IN} | Input Voltage Range (Single-ended) | $V_{DD} = 3.0 - 3.6\text{V}$ | 0.55 | | 2.00 | V |
| $ V_{ID} $ | Differential Input Voltage | | 0.100 | | 0.600 | V |
| V_{CM} | Common Mode Voltage Offset | $V_{DD} = 3.0 - 3.6\text{V}$ | $0.55 + V_{ID} /2$ | | $2.05 - V_{ID} /2$ | V |



20104303

FIGURE 4. FPD-Link Receiver V_{ID} and V_{CM} Definitions

DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)

RSDS Output

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------|-----------------------------|---------------------|-----|-----------|-----|-------|
| $V_{OD_{RSDS}}$ | Differential Output Voltage | $R_L = 100\ \Omega$ | | ± 200 | | mV |
| $V_{OS_{RSDS}}$ | Offset Voltage | | 1.1 | 1.3 | 1.5 | V |

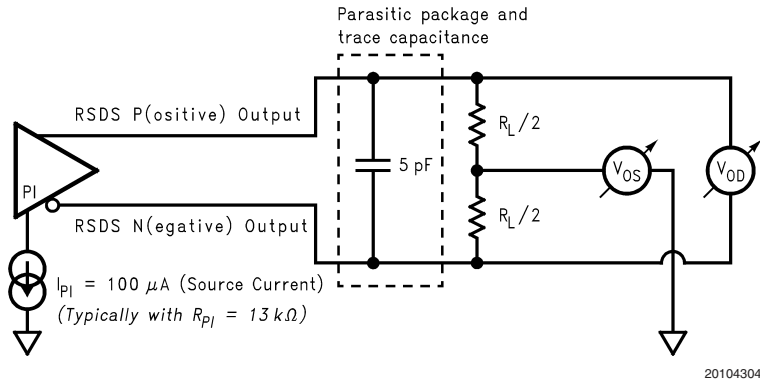


FIGURE 5. RSDS V_{OD} and V_{OS} Test Circuit

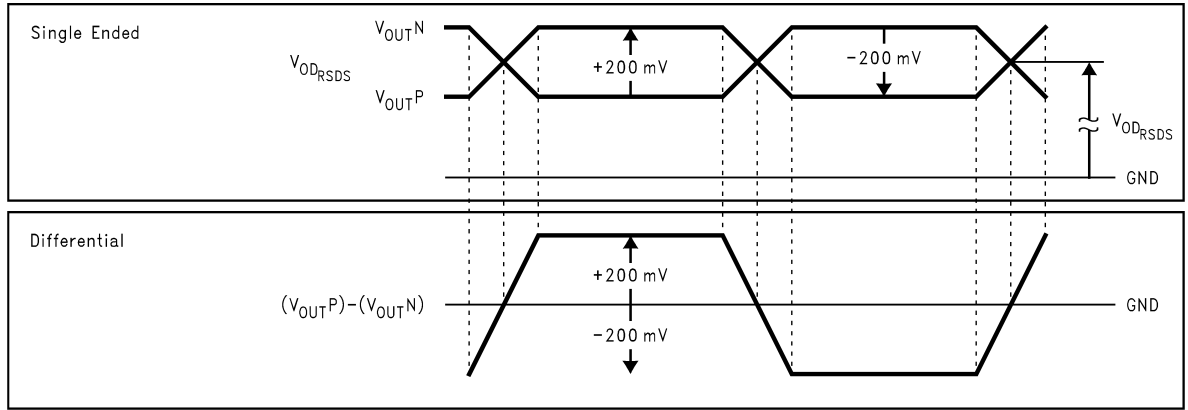


FIGURE 6. RSDS Output Waveforms: Single Ended vs Differential

AC Electrical Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified)

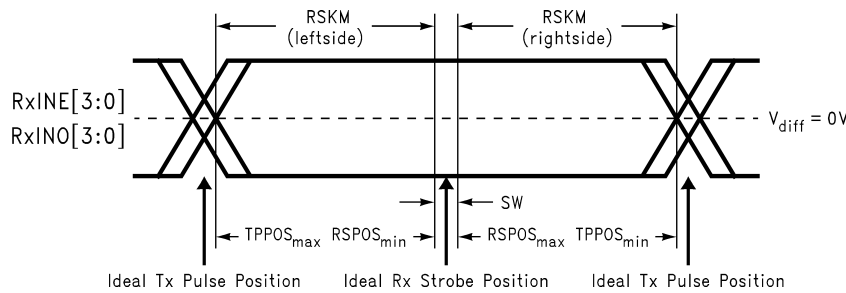
LVDS Data Input

| Symbol | Parameter | Conditions | Min | Max | Units |
|--------|--|---|-----|-----|-------|
| RPLLS | FPD-Link Receiver Phase Lock Loop Wake-up Time | | | 10 | ms |
| RSKM | RxIN Skew Margin (Note 2) and (Figure 7) | $V_{DD} = 3.3\text{V}$, $\text{CLK} = 85\ \text{MHz}$ | 240 | | ps |

Note 2: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window: RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type and length of cable), and source clock (FPD-Link Transmitter TxCLK IN) jitter. The specified RSKM minimum assumes a TPPOS max of 200 ps.

RSKM = cable skew (type, length) + source clock jitter (cycle to cycle) + remaining margin for data sampling (≥ 0)

This parameter is guaranteed by design. The limits are based on statistical analysis of the device performance over PVT (Process, Voltage, Temperature) range.



20104306

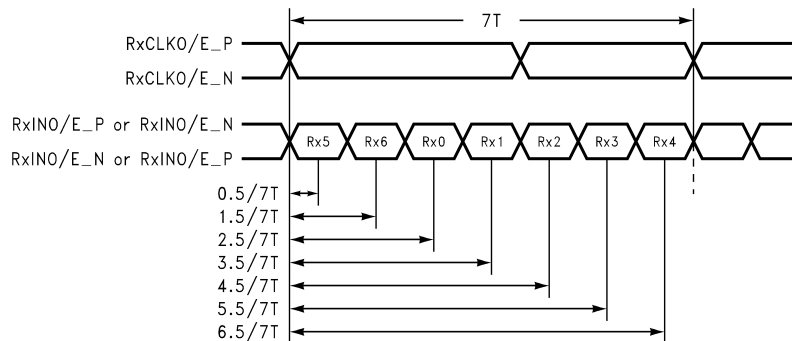
Acronyms:

- RSKM Receiver Skew Margin
- TPPOS Transmitter Pulse Position
- RSPOS Receiver Strobe Position
- SW Strobe Width

Definitions:

- SW: Setup and Hold Time (Internal data sampling window)
- RSKM: Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) + Remaining margin for data sampling (≥ 0)
- Cable Skew: Typically 10 ps – 40 ps per foot.

FIGURE 7. FPD-Link Receiver Input Skew Margin

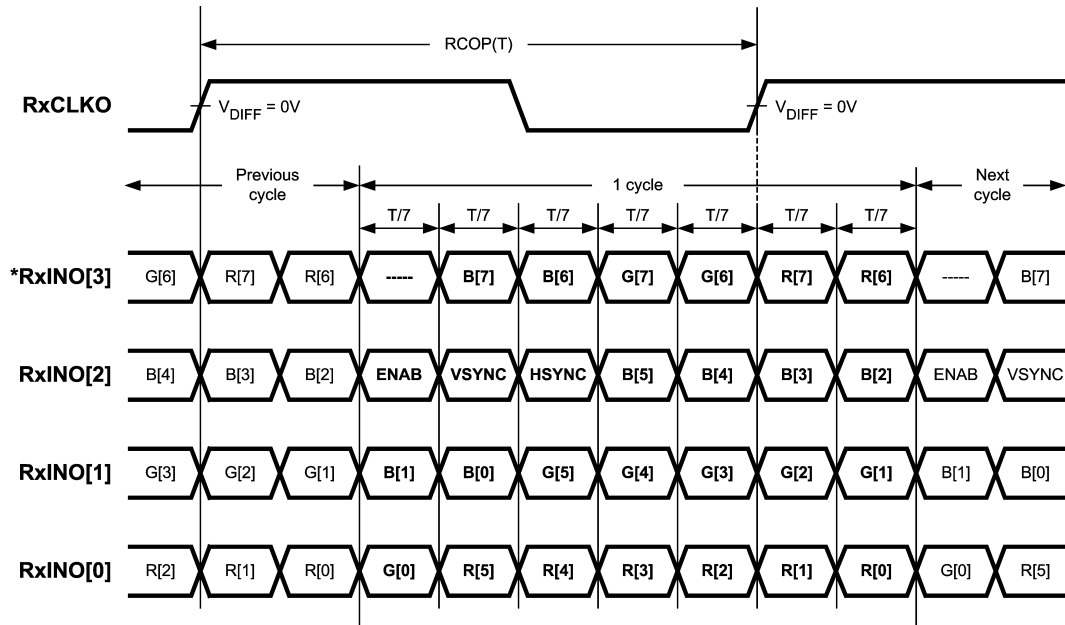


20104307

FIGURE 8. Ideal Strobe Position for LVDS Input

AC Electrical Characteristics

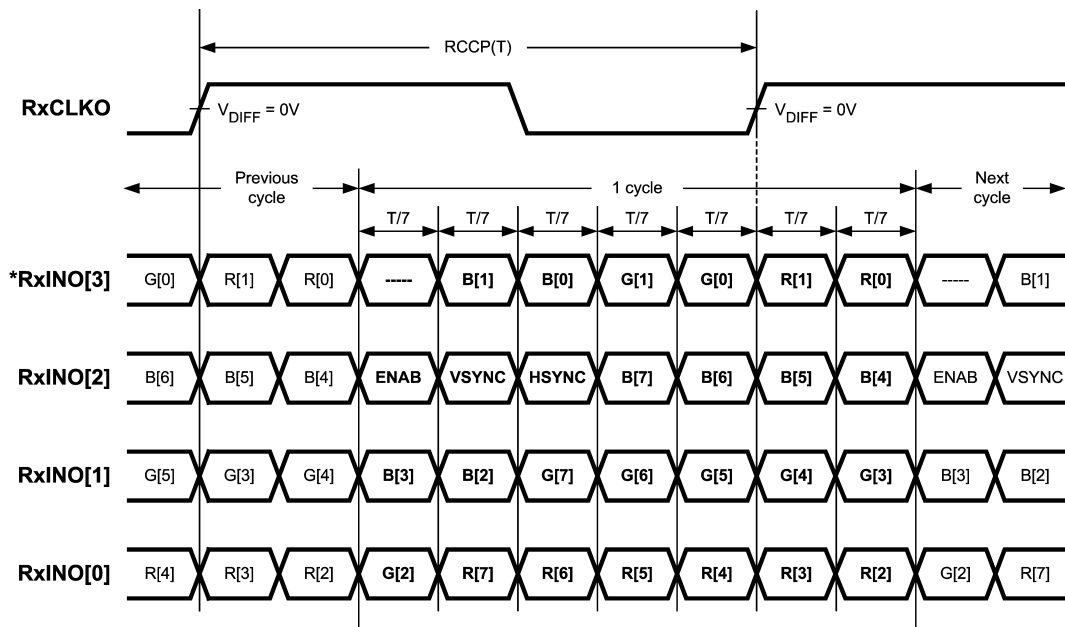
$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)



Note: *6-Bit Input Mode, LVDS Input Pair RxINx[3] will be Ignored

20104326

FIGURE 9. FPD-Link ReceiverSS Input Data Mappings (Default)



Note: *6-Bit Input Mode, LVDS Input Pair RxINx[3] will be Ignored

20104308

FIGURE 10. FPD-Link Receiver NS Input Data Mappings

AC Electrical Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)

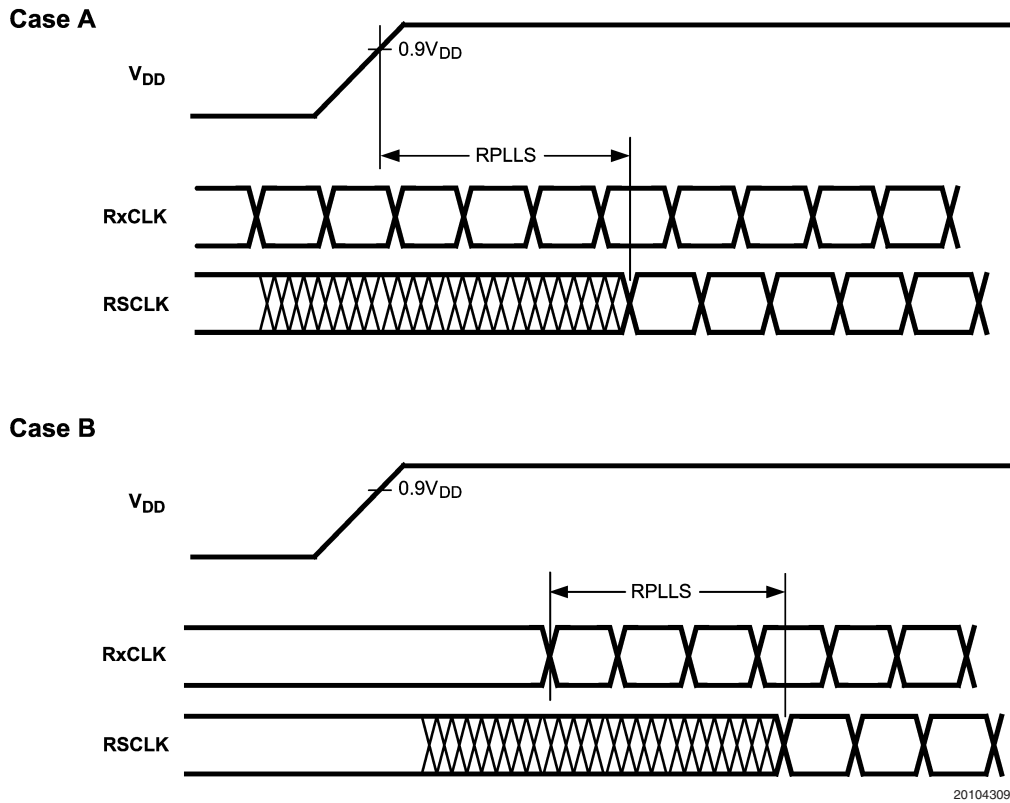


FIGURE 11. FPD-Link Receiver Phase Lock Loop Wake-up Time

AC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)

Output Timing

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|--|--|-----|------|-----|-------|
| RCHP | RS DS Clock (RSCK) High Period | $R_T = 100\ \Omega$, $I_{PI} = 100\ \mu\text{A}$, CLK = 85 MHz | | 5.7 | | ns |
| RCLP | RS DS Clock (RSCK) Low Period | $R_T = 100\ \Omega$, $I_{PI} = 100\ \mu\text{A}$, CLK = 85 MHz | | 5.8 | | ns |
| SPSTU | STH Rising to RSCK Falling | $R_T = 100\ \Omega$, $I_{PI} = 100\ \mu\text{A}$, CLK = 85 MHz | 3.0 | | | ns |
| SPHLD | STH Falling to RSCK Falling | $R_T = 100\ \Omega$, $I_{PI} = 100\ \mu\text{A}$, CLK = 85 MHz | 3.0 | | | ns |
| RSTU | RS(R, G, B) Setup to Falling or Rising Edge of RSCK | $R_T = 100\ \Omega$, $C_{L(RS DS)} = 5\ \text{pF}$, $I_{PI} = 100\ \mu\text{A}$, CLK = 85 MHz, RS DS[2:0] = "100" | | 3.28 | | ns |
| RHLD | RS(R, G, B) Hold from Falling or Rising Edge of RSCK | $R_T = 100\ \Omega$, $C_{L(RS DS)} = 5\ \text{pF}$, $I_{PI} = 100\ \mu\text{A}$, CLK = 85 MHz, RS DS[2:0] = "100" | | 1.87 | | ns |

RS DS Setup and Hold Time with Data Skew Control Values - Reference Only

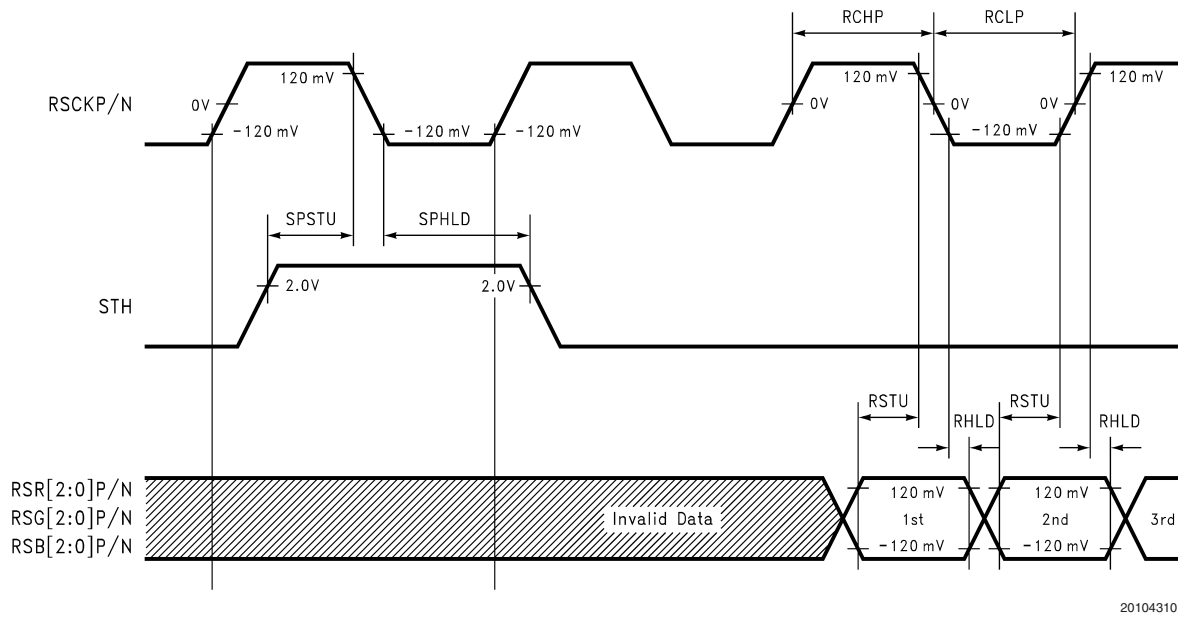
(RxCLKP/N = 85 MHz; $V_{DD} = 3.0$ to 3.6V , $R_T = 100\ \Omega$; $I_{PI} = 100\ \mu\text{A}$; Duty Clock = 50%/50%, $\pm 5\%$; 25°C)

Note: Typical values on this table are measured under Static and Steady state conditions which may not be reflective of its performance in the end application.

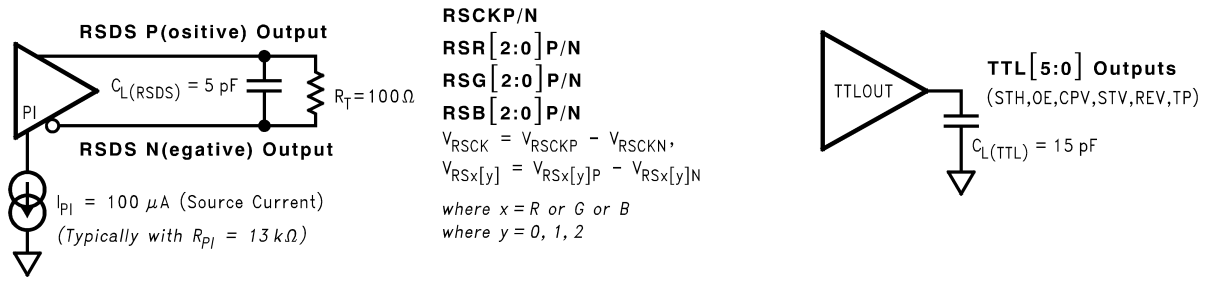
| RS DS[2:0] | Setup Time (RSTU) | | | Hold Time (RHLD) | | | Units |
|------------|-------------------|------|-----|------------------|------|-----|-------|
| | Min | Typ | Max | Min | Typ | Max | |
| 000 | | 1.26 | | | 3.91 | | ns |
| 001 | | 1.75 | | | 3.41 | | |
| 010 | | 2.30 | | | 2.90 | | |
| 011 | | 2.77 | | | 2.41 | | |
| 100 | | 3.28 | | | 1.87 | | |
| 101 | | 3.79 | | | 1.37 | | |
| 110 | | 4.27 | | | 0.89 | | |
| 111 | | 4.77 | | | 0.76 | | |

AC Electrical Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)



20104310

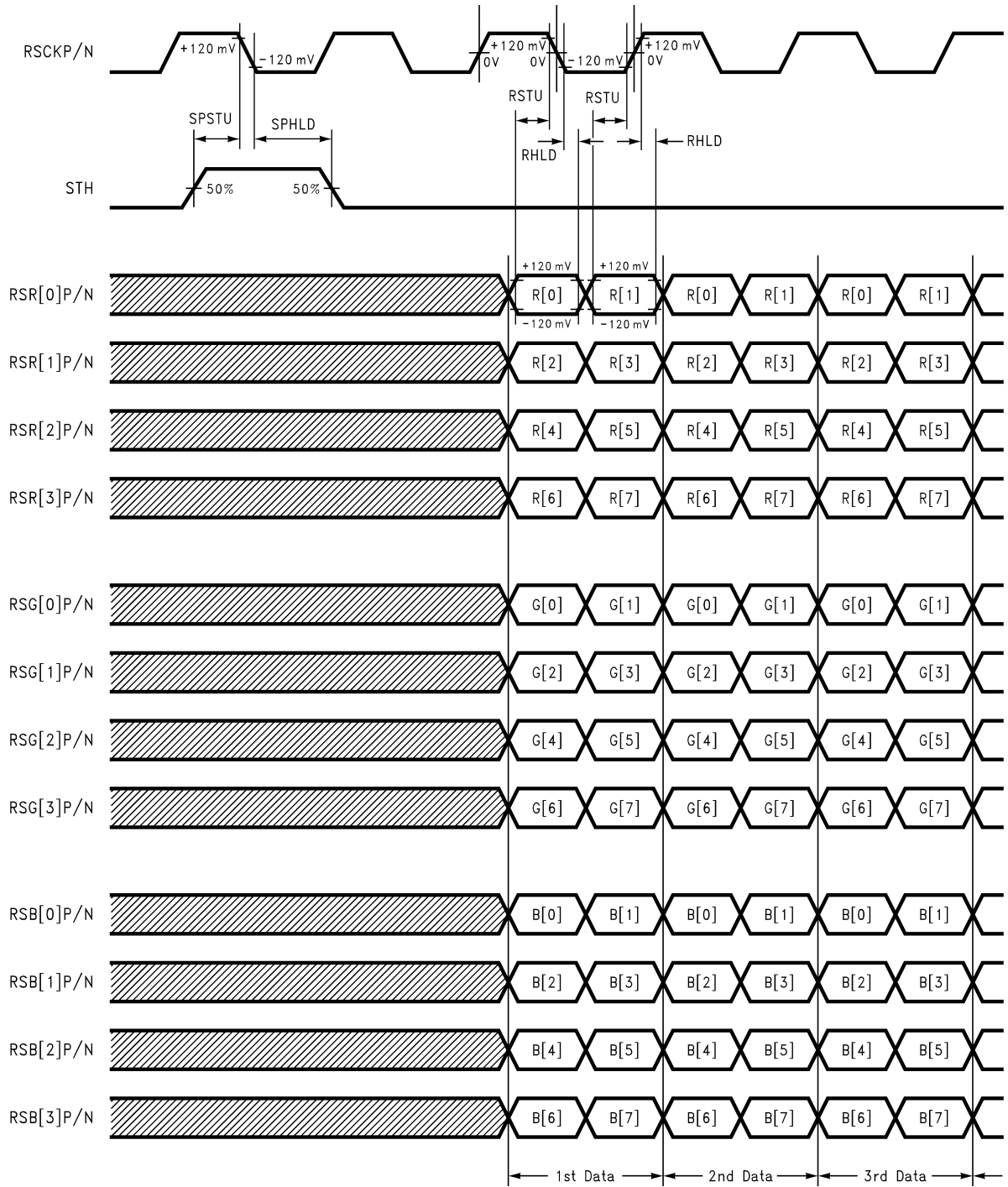


20104311

FIGURE 12. RSDS and TTL (CMOS) Output Timing Diagram

AC Electrical Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)



20104312

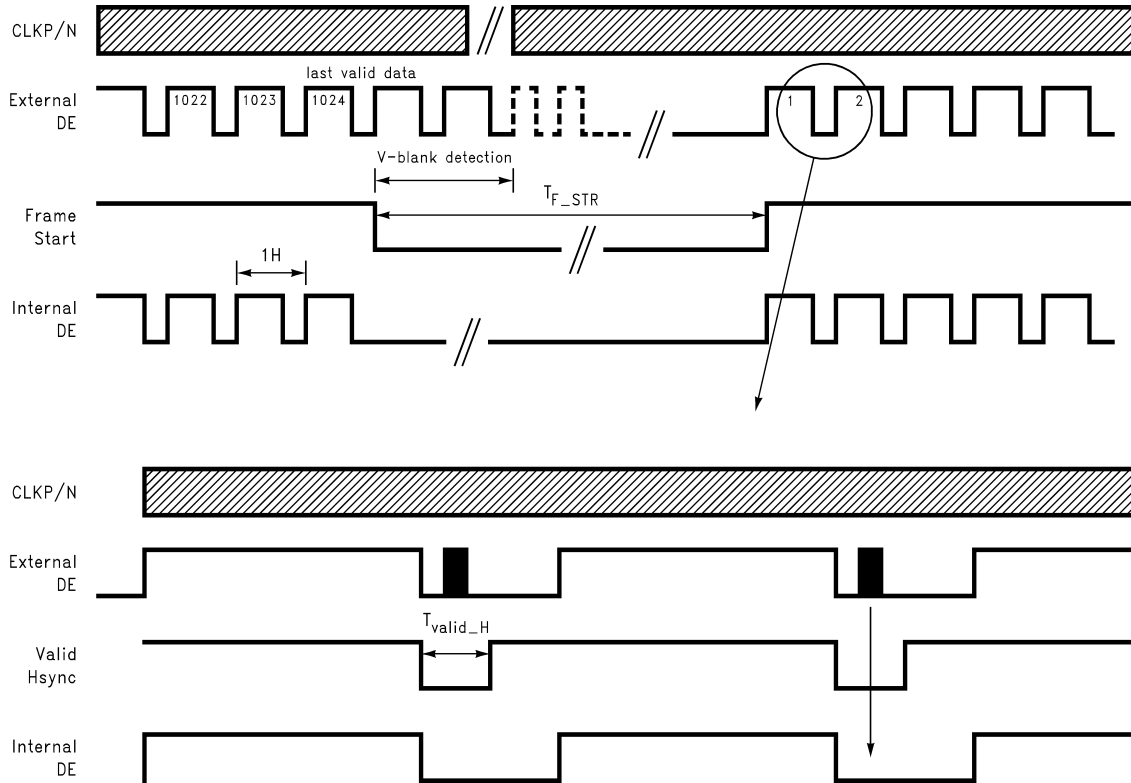
FIGURE 13. RS DS Output Data Mapping

AC Electrical Characteristics

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 3.0\text{V}$ to 3.6V , $I_{PI} = 100\ \mu\text{A}$ (Unless otherwise specified) (Continued)

Failure Detect (B/O pin "FDE" = High)

This function is valid in DE mode and FDE pin set to "High". Invalid external DE pulse does not affect the internal operation during failure zone.



20104313

| Graphic Mode | T_{F_STR} (Lines) | T_{valid_H} (Clocks) |
|--------------|----------------------|-------------------------|
| SXGA | 12 | 74 |
| SXGA+ | 12 | 74 |
| UXGA | 12 | 101 |

Note: T_{F_STR} (Frame Start Time) and T_{valid_H} (Valid H Time) is estimated numbers. These values may not work properly for the specific application and needs optimization procedure on the actual system.

Output Timing—TTL

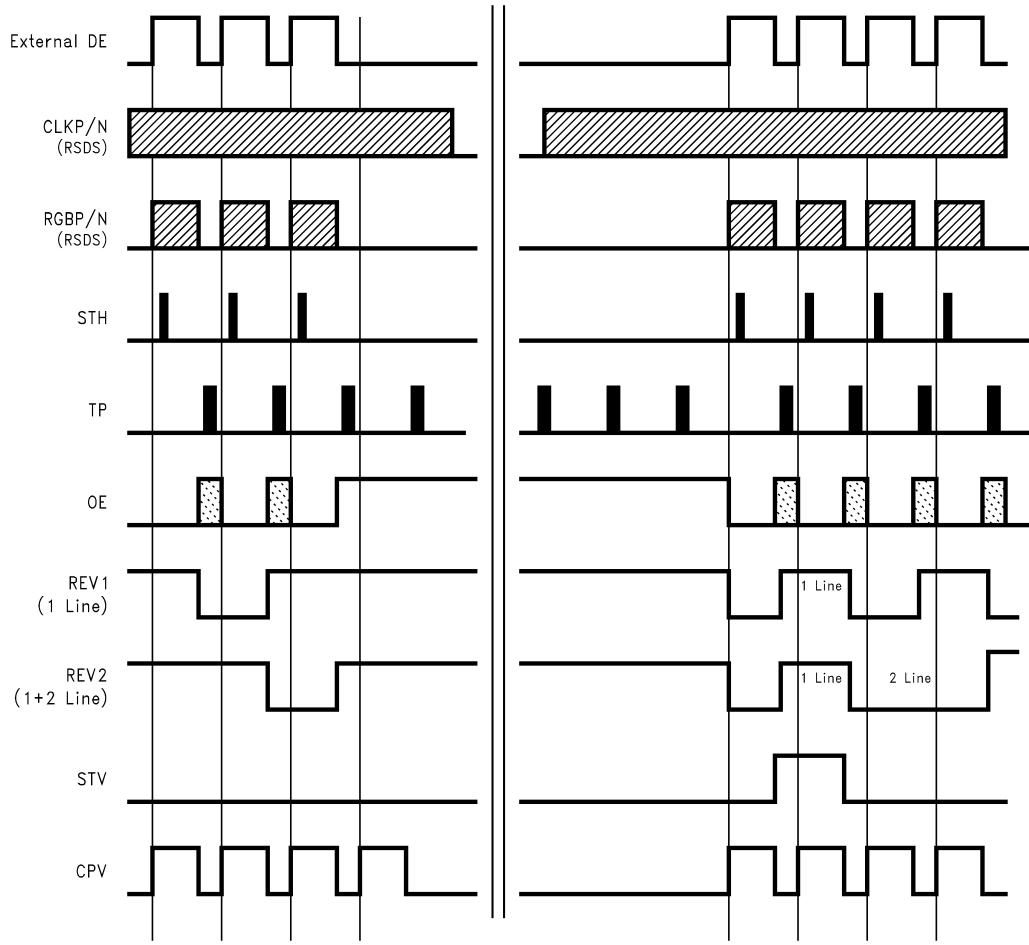
| Parameter | Comments (TPW, OE2, OE1 : 3'b000) | SXGA @ 54 MHz | SXGA+ @ 54 MHz | UXGA @ 81 MHz | Remarks/ Unit |
|-----------|--|------------------------------------|------------------------------------|-------------------------------------|------------------|
| t1 | STH Rising to Active Data | 2 | 2 | 2 | CLKP/N |
| t2 | High Duration of STH | 1 | 1 | 1 | CLKP/N |
| t3 | STH Rising to TP Rising | 660 | 720 | 820 | CLKP/N |
| t4 | High Duration of TP | 54 | 54 | 81 | CLKP/N |
| t5 | STH Rising to OE Falling | 687 | 747 | 861 | CLKP/N |
| t6 | High Duration of OE | 189 | 189 | 284 | CLKP/N |
| t7 | STH Rising to CPV | 660 | 720 | 820 | CLKP/N |
| t8 | High Duration of CPV | 422 | 422 | 540 | CLKP/N |
| t9 | STH Rising to STV | 238 | 298 | 280 | CLKP/N |
| t10 | High Duration of STV | 1 (844) | 1 (844) | 1 (1080) | Line (CLKP/N) |
| t11 | STH Rising to REV (1 LINE) | 645 | 705 | 805 | CLKP/N |
| t12 | High/Low Duration of REV (1 LINE) | 1 (844) | 1 (844) | 1 (1080) | Line (CLKP/N) |
| t13 | STH Rising to REV2 (1 + 2 LINE) | 645 | 705 | 805 | CLKP/N |
| t14 | High/Low Duration of REV2 (1 + 2 LINE) | 1 (the first line)/2 (844/1688) | 1 (the first line)/2 (844/1688) | 1 (the first line)/2 (1080/2160) | Line (CLKP/N) |

Line = Hsync Cycle

TP/OE Duty Control Configuration

| Resolution | TPW | OE2 | OE1 | TP | OE (μ s) | @ 54 MHz (CLK) | @ 81 MHz (CLK) |
|-------------------------|-----|-----|-----|---|------------------|-------------------|-------------------|
| SXGA, SXGA+ @ 54 MHz | 0 | 0 | 0 | 1.0 μ s 54 CLK @ 54 MHz 27 CLK @ 81 MHz | 3.5 | 189 | 284 |
| | 0 | 0 | 1 | | 3.0 | 162 | 243 |
| | 0 | 1 | 0 | | 2.5 | 135 | 203 |
| | 0 | 1 | 1 | | 2.0 | 108 | 162 |
| UXGA @ 81 MHz | 1 | 0 | 0 | 0.5 μ s 27 CLK @ 54 MHz 41 CLK @ 81 MHz | 3.5 | 189 | 284 |
| | 1 | 0 | 1 | | 3.0 | 162 | 243 |
| | 1 | 1 | 0 | | 2.5 | 135 | 203 |
| | 1 | 1 | 1 | | 2.0 | 108 | 162 |

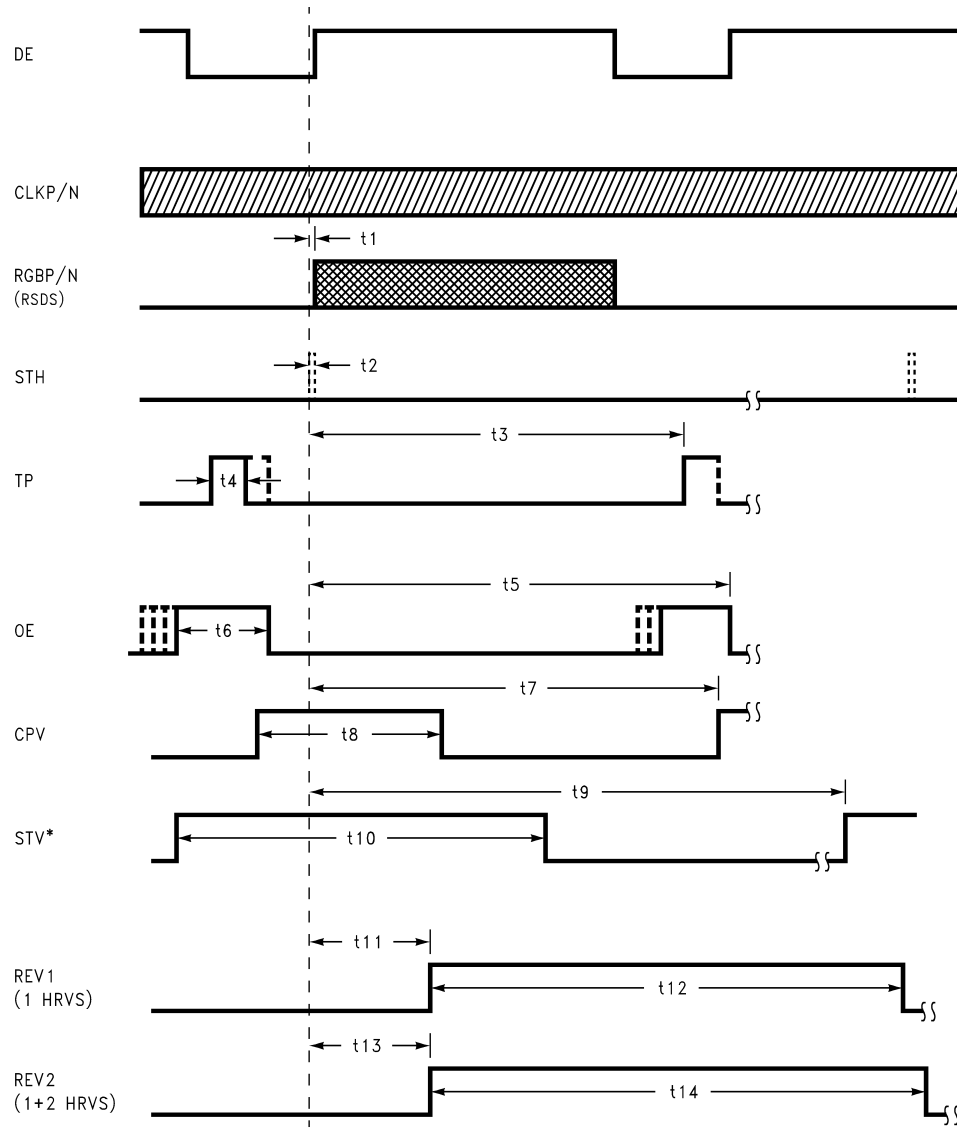
Output Timing—TTL (Continued)



20104314

FIGURE 14. TTL Output Timing Diagram

Output Timing—TTL (Continued)



* Timing based on first occurrence of STH signal to the left of the measured output.

20104315

FIGURE 15. Typical TTL Output Timing Diagram (continued)

Output Timing—TTL (Continued)

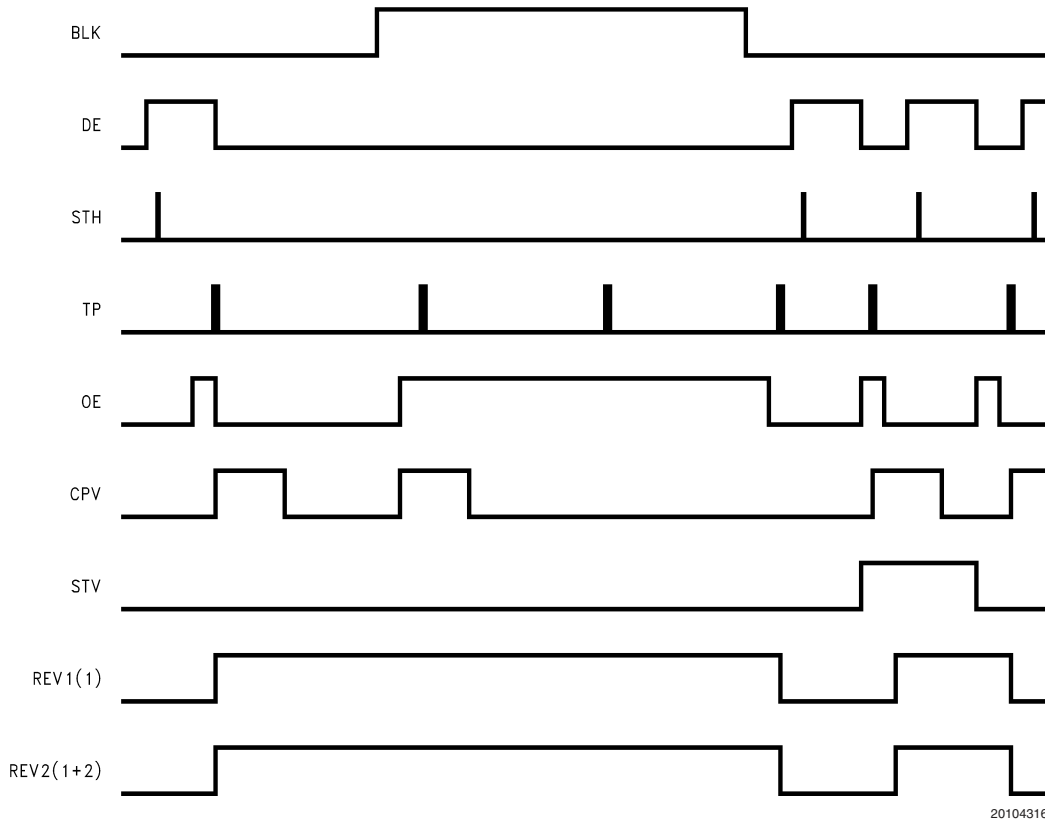


FIGURE 16. TTL Output Timing with Blanking

Output Timing—TTL (Continued)

8-BIT RSDS Output Data Mapping

| Pin No. | DMAP2, DMAP1 | | | | Pin No. | DMAP2, DMAP1 | | | |
|---------|--------------|-------|--------------|-------|---------|--------------|-------|--------------|-------|
| | 00 | 01 | 10 | 11 | | 00 | 01 | 10 | 11 |
| | Top Mount | | Bottom Mount | | | Top Mount | | Bottom Mount | |
| 47 | R3P_F | R0N_F | B0N_B | B3P_B | 78 | R3P_B | R0N_B | B0N_F | B3P_F |
| 48 | R3N_F | R0P_F | B0P_B | B3N_B | 79 | R3N_B | R0P_B | B0P_F | B3N_F |
| 49 | R2P_F | R1N_F | B1N_B | B2P_B | 80 | R2P_B | R1N_B | B1N_F | B2P_F |
| 50 | R2N_F | R1P_F | B1P_B | B2N_B | 81 | R2N_B | R1P_B | B1P_F | B2N_F |
| 51 | R1P_F | R2N_F | B2N_B | B1P_B | 82 | R1P_B | R2N_B | B2N_F | B1P_F |
| 52 | R1N_F | R2P_F | B2P_B | B1N_B | 83 | R1N_B | R2P_B | B2P_F | B1N_F |
| 53 | R0P_F | R3N_F | B3N_B | B0P_B | 84 | R0P_B | R3N_B | B3N_F | B0P_F |
| 54 | R0N_F | R3P_F | B3P_B | B0N_B | 85 | R0N_B | R3P_B | B3P_F | B0N_F |
| 56 | G3P_F | G0N_F | G0N_B | G3P_B | 87 | G3P_B | G0N_B | G0N_F | G3P_F |
| 57 | G3N_F | G0P_F | G0P_B | G3N_B | 88 | G3N_B | G0P_B | G0P_F | G3N_F |
| 58 | G2P_F | G1N_F | G1N_B | G2P_B | 89 | G2P_B | G1N_B | G1N_F | G2P_F |
| 59 | G2N_F | G1P_F | G1P_B | G2N_B | 90 | G2N_B | G1P_B | G1P_F | G2N_F |
| 60 | G1P_F | G2N_F | G2N_B | G1P_B | 91 | G1P_B | G2N_B | G2N_F | G1P_F |
| 61 | G1N_F | G2P_F | G2P_B | G1N_B | 92 | G1N_B | G2P_B | G2P_F | G1N_F |
| 62 | G0P_F | G3N_F | G3N_B | G0P_B | 93 | G0P_B | G3N_B | G3N_F | G0P_F |
| 63 | G0N_F | G3P_F | G3P_B | G0N_B | 94 | G0N_B | G3P_B | G3P_F | G0N_F |
| 65 | CLKP_F | | CLKP_B | | 95 | CLKP_B | | CLKP_F | |
| 66 | CLKN_F | | CLKN_B | | 96 | CLKN_B | | CLKN_F | |
| 67 | B3P_F | B0N_F | R0N_B | R3P_B | 98 | B3P_B | B0N_B | R0N_F | R3P_F |
| 68 | B3N_F | B0P_F | R0P_B | R3N_B | 99 | B3N_B | B0P_B | R0P_F | R3N_F |
| 69 | B2P_F | B1N_F | R1N_B | R2P_B | 100 | B2P_B | B1N_B | R1N_F | R2P_F |
| 70 | B2N_F | B1P_F | R1P_B | R2N_B | 101 | B2N_B | B1P_B | R1P_F | R2N_F |
| 71 | B1P_F | B2N_F | R2N_B | R1P_B | 102 | B1P_B | B2N_B | R2N_F | R1P_F |
| 72 | B1N_F | B2P_F | R2P_B | R1N_B | 103 | B1N_B | B2P_B | R2P_F | R1N_F |
| 73 | B0P_F | B3N_F | R3N_B | R0P_B | 104 | B0P_B | B3N_B | R3N_F | R0P_F |
| 74 | B0N_F | B3P_F | R3P_B | R0N_B | 105 | B0N_B | B3P_B | R3P_F | R0N_F |
| 107 | STH_F | | STH_B | | 108 | STH_B | | STH_F | |

Output Timing—TTL (Continued)

6-BIT RSDS Output Data Mapping

| Pin No. | DMAP2, DMAP1 | | | | Pin No. | DMAP2, DMAP1 | | | |
|---------|--------------|-------|--------------|-------|---------|--------------|-------|--------------|-------|
| | 00 | 01 | 10 | 11 | | 00 | 01 | 10 | 11 |
| | Top Mount | | Bottom Mount | | | Top Mount | | Bottom Mount | |
| 47 | HI-Z | R0N_F | B0N_B | HI-Z | 78 | HI-Z | R0N_B | B0N_F | HI-Z |
| 48 | HI-Z | R0P_F | B0P_B | HI-Z | 79 | HI-Z | R0P_B | B0P_F | HI-Z |
| 49 | R2P_F | R1N_F | B1N_B | B2P_B | 80 | R2P_B | R1N_B | B1N_F | B2P_F |
| 50 | R2N_F | R1P_F | B1P_B | B2N_B | 81 | R2N_B | R1P_B | B1P_F | B2N_F |
| 51 | R1P_F | R2N_F | B2N_B | B1P_B | 82 | R1P_B | R2N_B | B2N_F | B1P_F |
| 52 | R1N_F | R2P_F | B2P_B | B1N_B | 83 | R1N_B | R2P_B | B2P_F | B1N_F |
| 53 | R0P_F | HI-Z | HI-Z | B0P_B | 84 | R0P_B | HI-Z | HI-Z | B0P_F |
| 54 | R0N_F | HI-Z | HI-Z | B0N_B | 85 | R0N_B | HI-Z | HI-Z | B0N_F |
| 56 | HI-Z | G0N_F | G0N_B | HI-Z | 87 | HI-Z | G0N_B | G0N_F | HI-Z |
| 57 | HI-Z | G0P_F | G0P_B | HI-Z | 88 | HI-Z | G0P_B | G0P_F | HI-Z |
| 58 | G2P_F | G1N_F | G1N_B | G2P_B | 89 | G2P_B | G1N_B | G1N_F | G2P_F |
| 59 | G2N_F | G1P_F | G1P_B | G2N_B | 90 | G2N_B | G1P_B | G1P_F | G2N_F |
| 60 | G1P_F | G2N_F | G2N_B | G1P_B | 91 | G1P_B | G2N_B | G2N_F | G1P_F |
| 61 | G1N_F | G2P_F | G2P_B | G1N_B | 92 | G1N_B | G2P_B | G2P_F | G1N_F |
| 62 | G0P_F | HI-Z | HI-Z | G0P_B | 93 | G0P_B | HI-Z | HI-Z | G0P_F |
| 63 | G0N_F | HI-Z | HI-Z | G0N_B | 94 | G0N_B | HI-Z | HI-Z | G0N_F |
| 65 | CLKP_F | | CLKP_B | | 95 | CLKP_B | | CLKP_F | |
| 66 | CLKN_F | | CLKN_B | | 96 | CLKN_B | | CLKN_F | |
| 67 | HI-Z | B0N_F | R0N_B | HI-Z | 98 | HI-Z | B0N_B | R0N_F | HI-Z |
| 68 | HI-Z | B0P_F | R0P_B | HI-Z | 99 | HI-Z | B0P_B | R0P_F | HI-Z |
| 69 | B2P_F | B1N_F | R1N_B | R2P_B | 100 | B2P_B | B1N_B | R1N_F | R2P_F |
| 70 | B2N_F | B1P_F | R1P_B | R2N_B | 101 | B2N_B | B1P_B | R1P_F | R2N_F |
| 71 | B1P_F | B2N_F | R2N_B | R1P_B | 102 | B1P_B | B2N_B | R2N_F | R1P_F |
| 72 | B1N_F | B2P_F | R2P_B | R1N_B | 103 | B1N_B | B2P_B | R2P_F | R1N_F |
| 73 | B0P_F | HI-Z | HI-Z | R0P_B | 104 | B0P_B | HI-Z | HI-Z | R0P_F |
| 74 | B0N_F | HI-Z | HI-Z | R0N_B | 105 | B0N_B | HI-Z | HI-Z | R0N_F |
| 107 | STH_F | | STH_B | | 108 | STH_B | | STH_F | |

Note: Note: For 6-bit output mode, RSDS pair 3P/Ns will be in HI-Z mode.

LVDS Input and RSDS Output Data

| RxMap | BIT_CFG2 | BIT_CFG1 | Input Data | Output Data | Functional Description |
|-------|----------|----------|------------|-------------|-----------------------------------|
| 0 | 0 | 0 | 8-bit | 8-bit | Data is unchanged (NS mapping) |
| 0 | 0 | 1 | 8-bit | 6-bit | 2 MSBs are HI-Z, FRC Enabled (NS) |
| 0 | 1 | 0 | 6-bit | 8-bit | 2 LSBs are zero (NS) |
| 0 | 1 | 1 | 6-bit | 6-bit | 2 MSBs are HI-Z (NS) |
| 1 | 0 | 0 | 8-bit | 8-bit | Data is unchanged (SS mapping) |
| 1 | 0 | 1 | 8-bit | 6-bit | 2 MSBs are HI-Z, FRC Enabled (SS) |
| 1 | 1 | 0 | 6-bit | 8-bit | 2 LSBs are zero (SS) |
| 1 | 1 | 1 | 6-bit | 6-bit | 2 MSBs are HI-Z (SS) |

Input Signal Timing

Sync only mode, no DE inputted, is supported when the SYNC pin (Bonding Option pin) is enable high. Whenever DE signal is inputted, it works as DE mode. In the DE mode, H-blank min is considered with Failure detection mode enabled. In the defaults mode, T_{valid_H} should be subtracted in the table below.

| Graphic Mode | Sync Mode (Bonding Option) | | | | | | DE Mode | | Number of Total Horizontal Lines in a Frame | Number of Total Pixel Clocks in a Horizontal Line |
|--------------|----------------------------|----------------|------|-------------------|----------------|------|-------------------|-------------------|---|---|
| | H-Timing (clocks) | | | V-Timing (lines) | | | H-Timing (clocks) | V-Timing (lines) | | |
| | From Sync to Data | Total H-Timing | | From Sync to Data | Total V-Timing | | H-Blank | H-Blank Detection | | |
| | Typ | Min | Max | Typ | Min | Max | Min | Min | | |
| SXGA | 248 | 1430 | 2047 | 38 | 1066 | 2047 | 150 | 2 | 1066 | 1688 |
| SXGA+ | 128 | 1550 | 2047 | 12 | 1066 | 2047 | 150 | 2 | 1066 | 1688 |
| UXGA | 304 | 1804 | 4095 | 46 | 1250 | 2047 | 204 | 2 | 1250 | 2160 |

Note: H = Lines

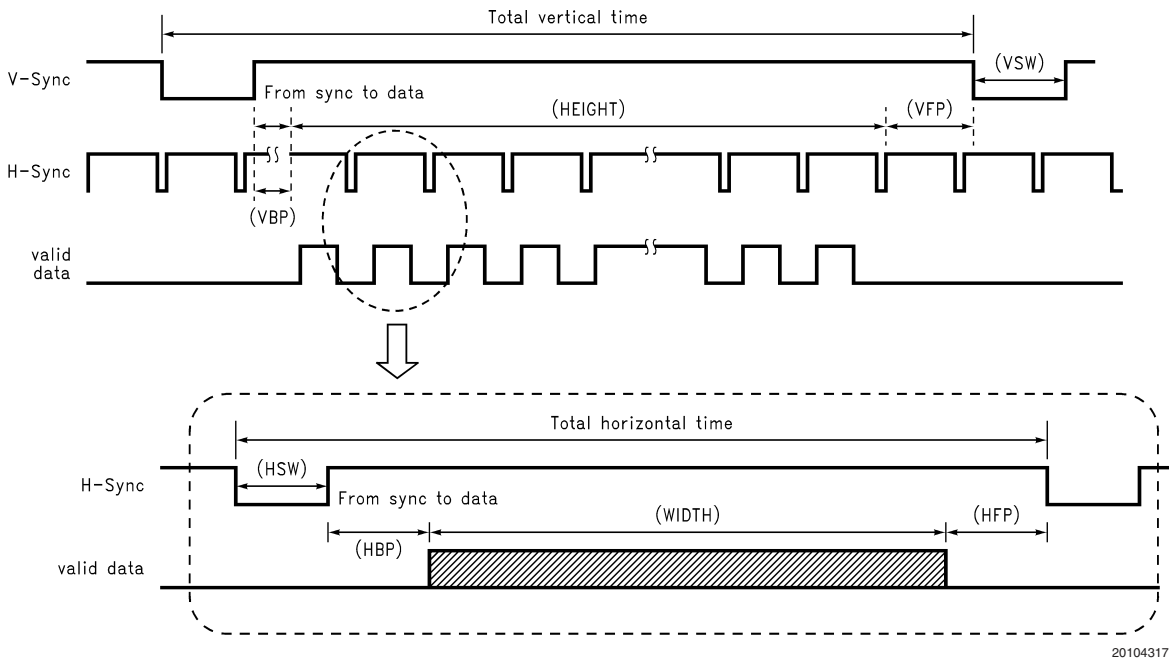


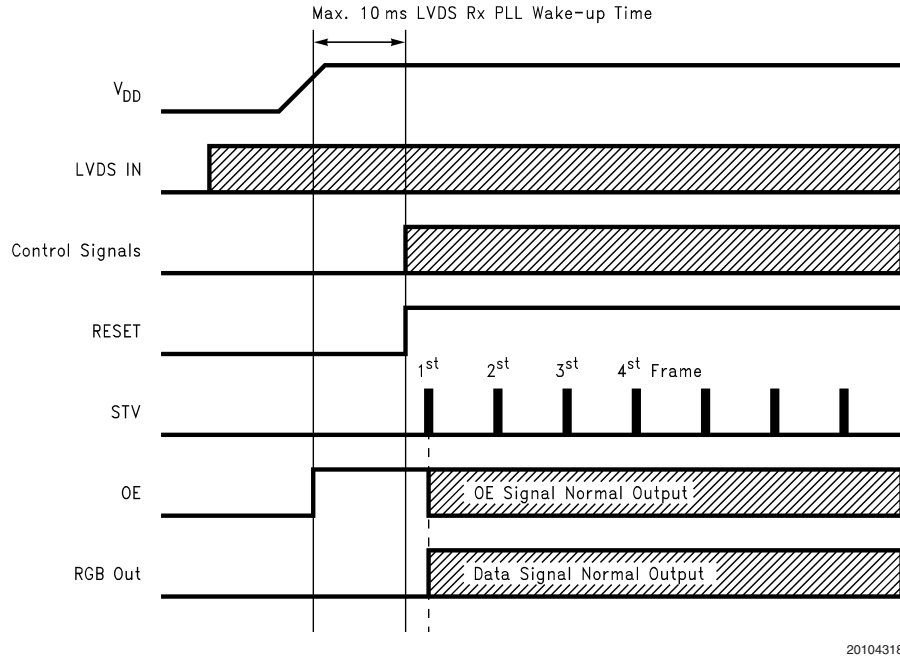
FIGURE 17. Video Signal Format

Supports VESA Standard in SYNC Mode (B/O SYNC Pin = High)

| | | SXGA | SXGA+ | UXGA | Unit |
|------------|--------|------|-------|------|-------|
| Horizontal | WIDTH | 1280 | 1400 | 1600 | clock |
| | HFP | 48 | 48 | 64 | clock |
| | HSW | 112 | 112 | 192 | clock |
| | HBP | 248 | 128 | 304 | clock |
| Vertical | HEIGHT | 1024 | 1050 | 1200 | Line |
| | VFP | 1 | 1 | 1 | Line |
| | VSW | 3 | 3 | 3 | Line |
| | VBP | 38 | 12 | 46 | Line |

Power Up Sequence (Defaults)

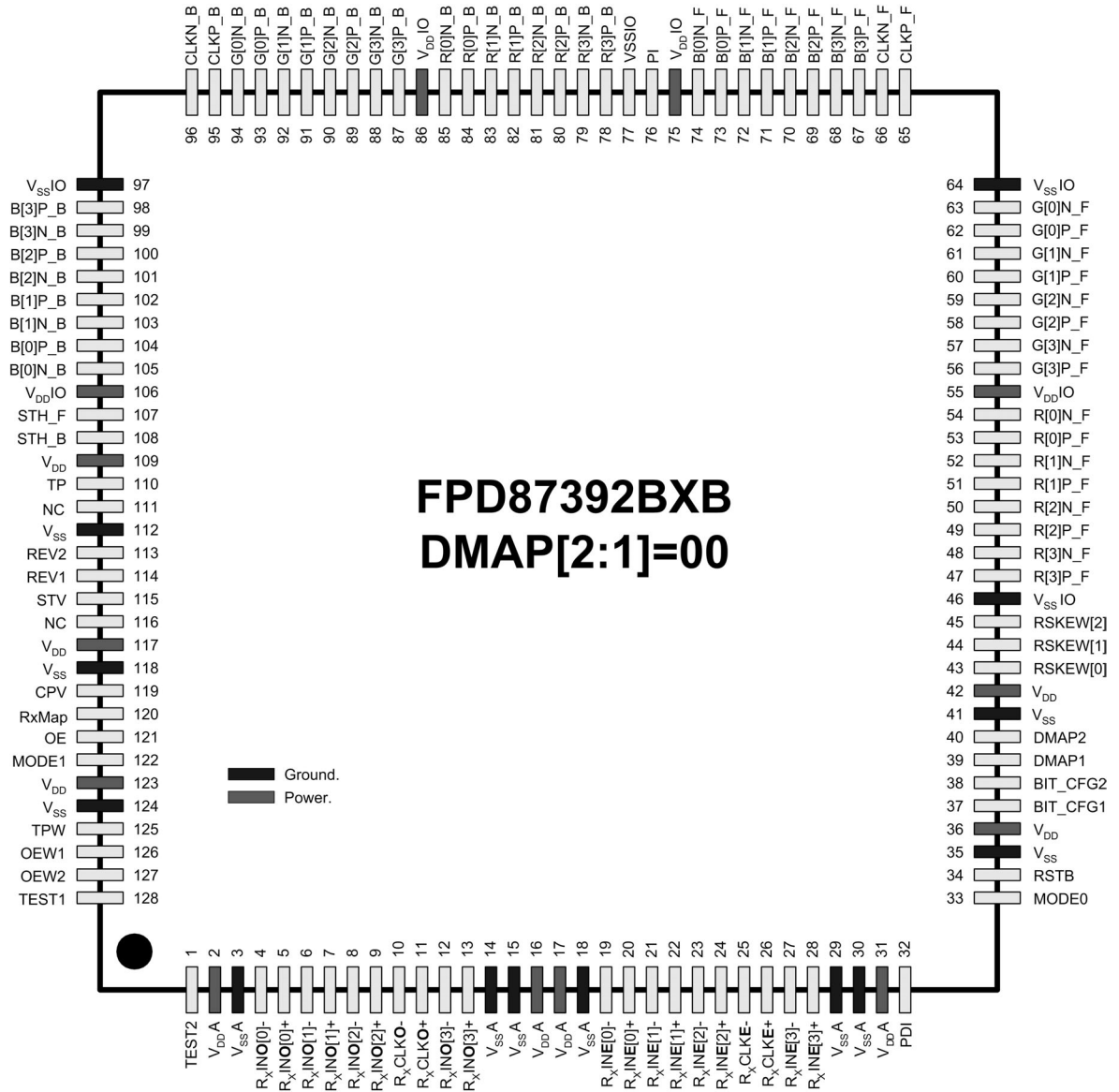
When Power is ON, the TCON start to operate and generate the control signals by inputted LVDS signals. LVDS Receiver will take maximum 10 ms for the PLL wake-up time. Whether LVDS signals exist before the power-on doesn't effect. When the Reset is reach to 2.0V, the R, G, B data and control signals are outputted sequentially and the sequence is just as following figure.



20104318

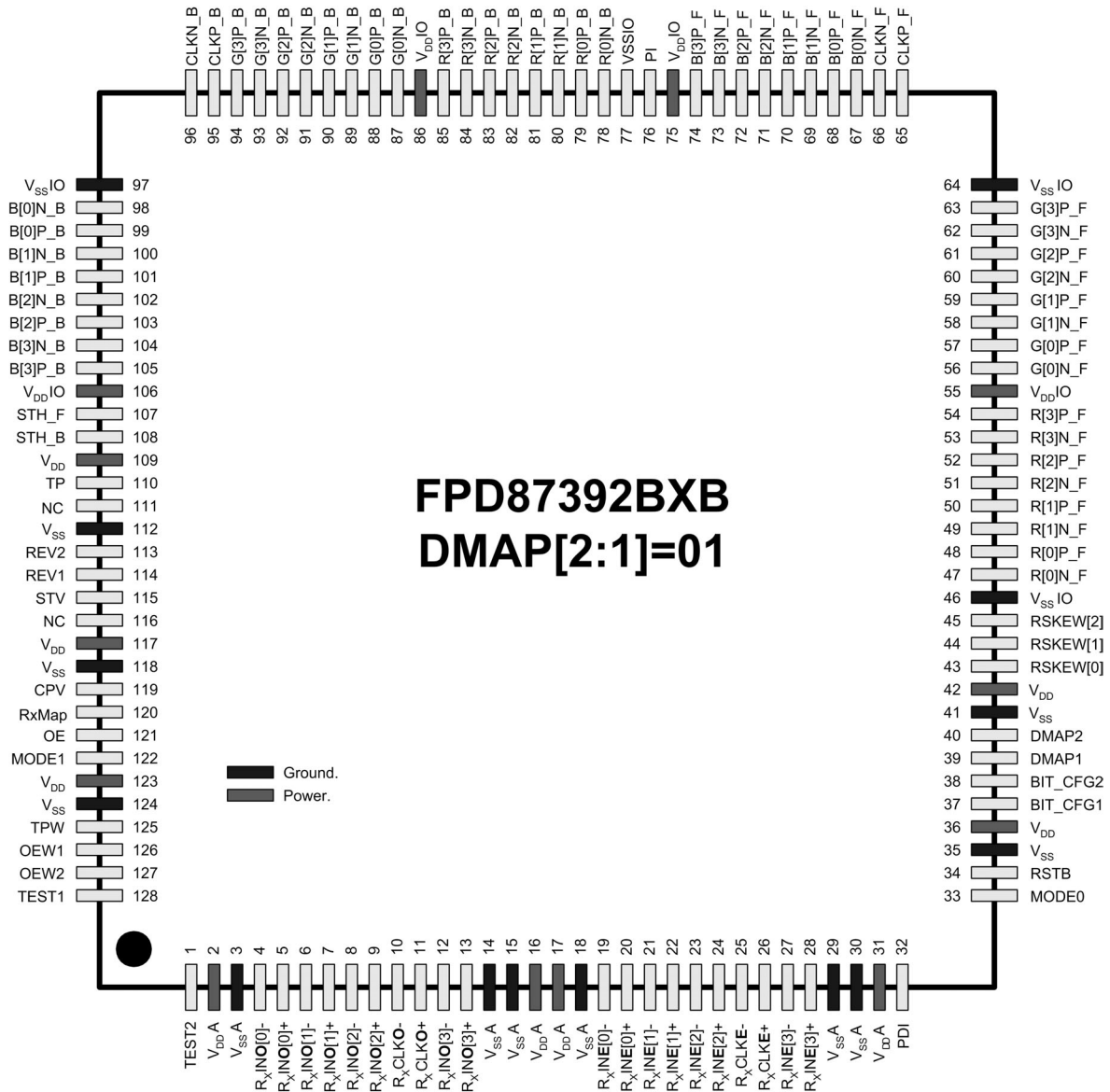
FIGURE 18. Power Up Sequence

Pin Connection



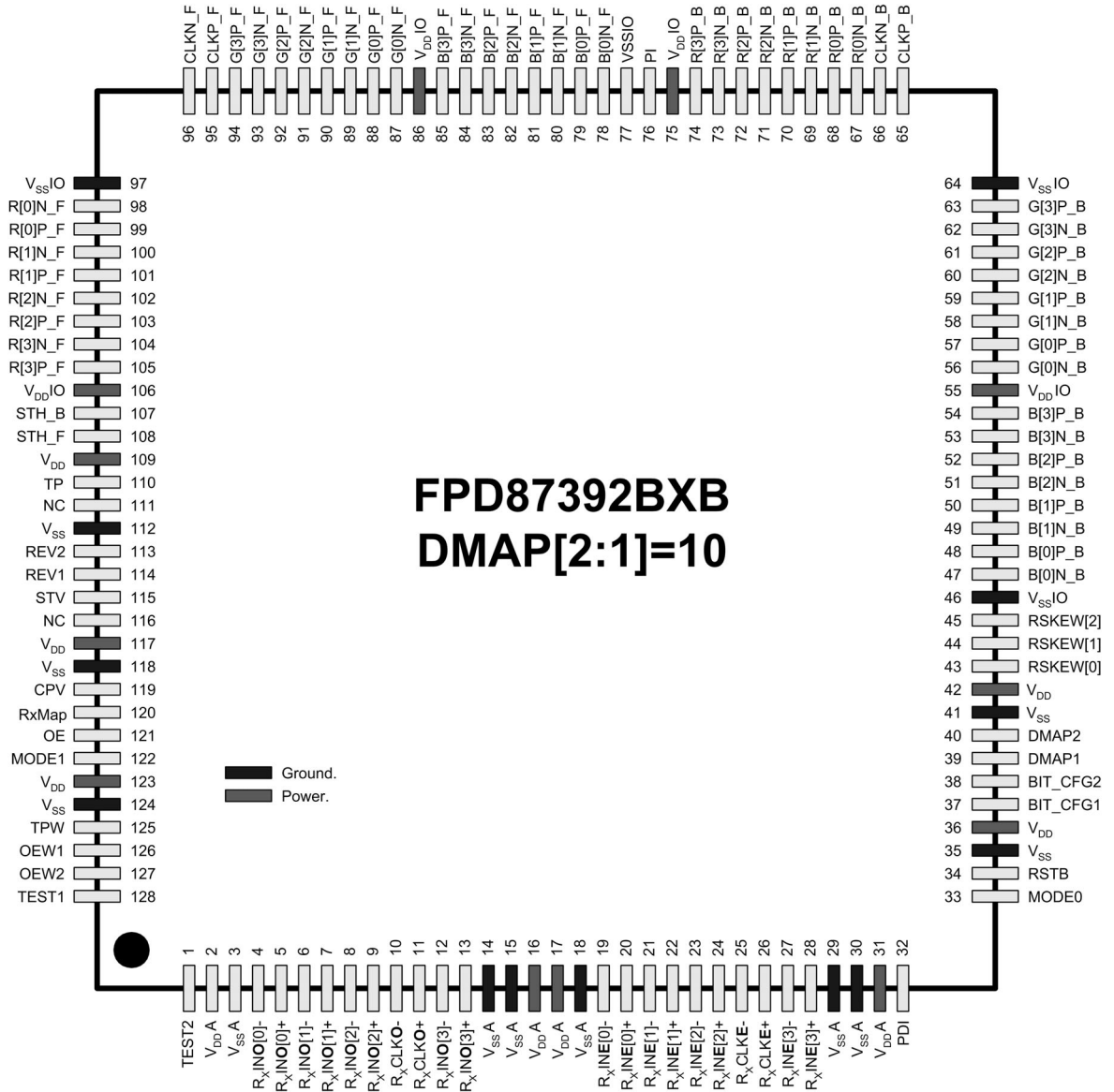
20104319

Pin Connection (Continued)



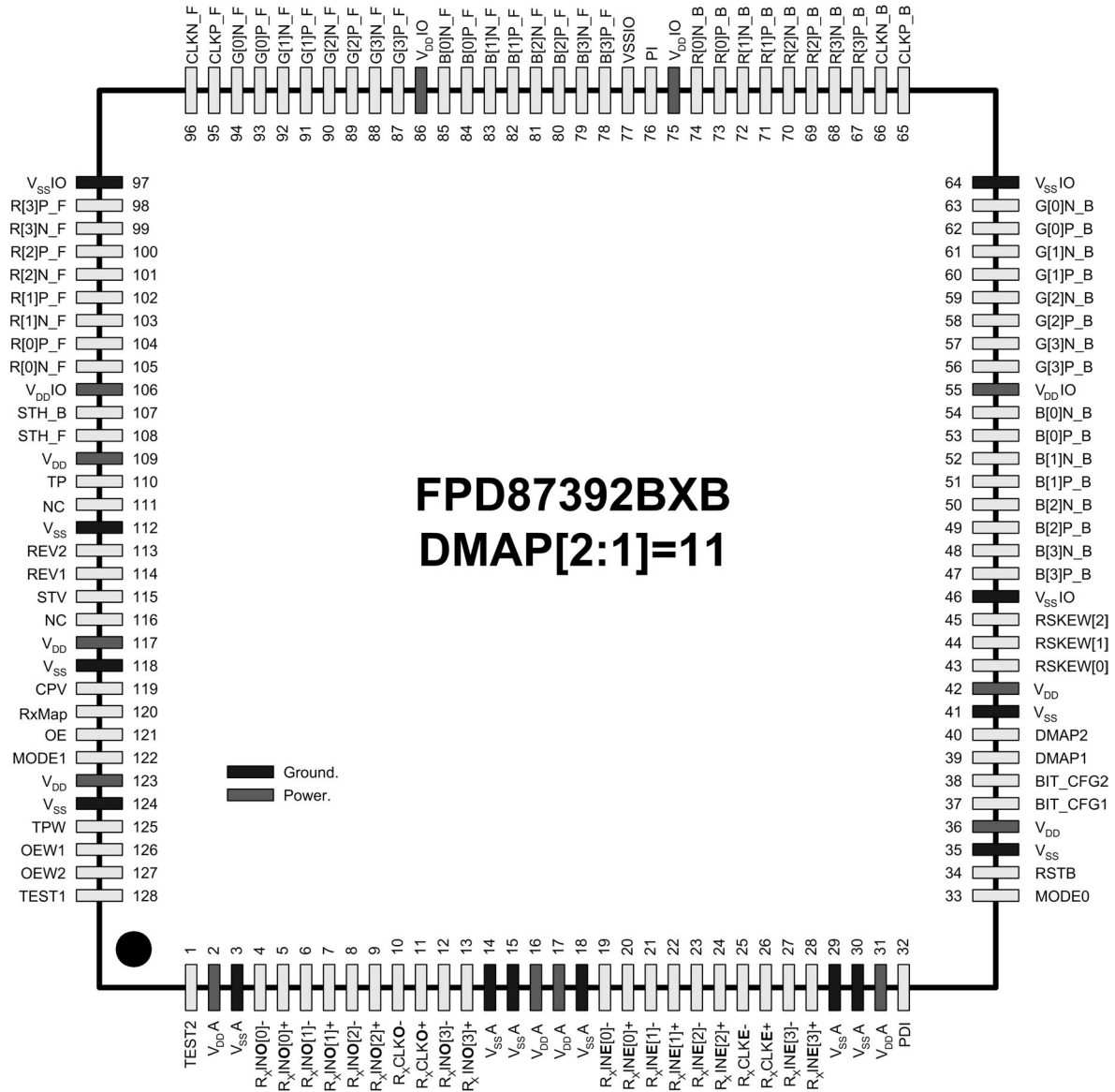
20104320

Pin Connection (Continued)



20104321

Pin Connection (Continued)



20104322

Pin Description System Interface

| Symbol | Pin No. | Type | Function |
|--------------------------------|------------------|-------|---|
| RxINO[0]P/N and RxINE[0]P/N | 4, 5 19, 20 | LVDSI | FPD-Link Data Differential Pair 0 Input |
| RxINO[1]P/N and RxINE[1]P/N | 6, 7 21, 22 | LVDSI | FPD-Link Data Differential Pair 1 Input |
| RxINO[2]P/N and RxINE[2]P/N | 8, 9 23, 24 | LVDSI | FPD-Link Data Differential Pair 2 Input |
| RxINO[3]P/N and RxINE[3]P/N | 12, 13 25, 26 | LVDSI | FPD-Link Data Differential Pair 3 Input |
| RxCLKOP/N and RxCLKEP/N | 10, 11 27, 28 | LVDSI | FPD-Link Clock Differential Pair Input |

RSDS Interface

| Symbol | Pin No. | Type | Function |
|-------------|------------|------|--|
| B[3:0]P/N_B | 47–54 | RSO | Blue Reduced Swing Differential Outputs to Back Column Drivers |
| G[3:0]P/N_B | 56–63 | RSO | Green Reduced Swing Differential Outputs to Back Column Drivers |
| R[3:0]P/N_B | 67–74 | RSO | Red Reduced Swing Differential Outputs to Back Column Drivers |
| CLKP/N_B | 65, 66 | RSO | Clock Reduced Swing Differential Outputs to Back Column Drivers |
| B[3:0]P/N_F | 78–85 | RSO | Blue Reduced Swing Differential Outputs to Front Column Drivers |
| G[3:0]P/N_F | 87–94 | RSO | Green Reduced Swing Differential Outputs to Front Column Drivers |
| R[3:0]P/N_F | 98–105 | RSO | Red Reduced Swing Differential Outputs to Front Column Drivers |
| CLKP/N_F | 95, 96 | RSO | Clock Reduced Swing Differential Outputs to Front Column Drivers |
| PI | 76 | I | External Resistor Input for RSDS Output (V_{OD}) Level Control |
| RSKEW[2:0] | 43, 44, 45 | I | Output RSDS Data Skew Control (Default 3'b000) |

Column/Row Driver Control

| Symbol | Pin No. | Type | Function |
|--------|---------|------|--|
| TP | 110 | TO | Line Latch Signal Output to Column Drivers |
| STH_B | 107 | TO | Horizontal Start Signal Output to Back Column Drivers |
| STH_F | 108 | TO | Horizontal Start Signal Output to Front Column Drivers |
| REV1 | 114 | TO | Data Inversion Output to Column Driver (1 Line) |
| REV2 | 113 | TO | Data Inversion Output to Column Driver (1 + 2 Line) |
| STV | 115 | TO | Row Driver Start Pulse |
| CPV | 119 | TO | Row Driver Shift Clock |
| OE | 121 | TO | Control TFT Gate Pulse Width to Row Drivers |

Pin Description (Continued)**Control Input**

| Symbol | Pin No. | Type | Function |
|------------|----------|------|---|
| BIT_CFG1/2 | 37, 38 | I | LVDS Input and RSDS Output Bit Selection |
| MODE[1:0] | 122, 33 | I | Graphic Mode Selection “00”: SXGA, “01”: SXGA+, “10”: UXGA, “11”: Don't Care |
| DMAP1/2 | 39, 40 | I | RSDS Output Data Mapping |
| TPW | 125 | I | TP Duty Control (Default Low) |
| OEW1/2 | 126, 127 | I | OE Duty Control (Default 2'b00) |
| TEST1/2 | 128, 1 | I | Test Mode Low: Normal Operation, High: Test Mode |
| PDI | 32 | I | LVDS Power Down (Active Low) |
| RSTB | 34 | I | System Reset (Active Low) |
| RxMap | 120 | I | RxMap=1(SS Mapping); RxMap=0, NS Mapping |
| NC | 111, 116 | | No Connect |

Power Supply

| Symbol | Pin No. | Type | Function |
|-------------------|--------------------------|------|---|
| V _{DD} | 36, 42, 109, 117, 123 | P | Digital Power for Logic Core and LVDS Deserializer |
| V _{SS} | 35, 41, 112, 118, 124 | G | Digital Ground for Logic Core and LVDS Deserializer |
| V _{DDA} | 2, 16, 17, 31 | P | Power for LVDS PLL and Analog Bandgap |
| V _{SSA} | 3, 14, 15, 18, 29, 30 | G | Ground for LVDS PLL and Analog Bandgap |
| V _{DDIO} | 55, 75, 86, 106 | P | Digital I/O Power and RSDS Outputs |
| V _{SSIO} | 46, 64, 77, 97 | G | Digital I/O Ground and RSDS Outputs |

Bonding Option (B/O)

| Symbol | Pin No. | Type | Function |
|--------|---------|------|---|
| SYNC | B/O | PU | SYNC Mode High: Enable, Low: Disable |
| FRM | B/O | PU | Free Run Mode High: Enable, Low: Disable |
| FDE | B/O | PU | Failure Detection High: Enable, Low: Disable |
| POR | B/O | PU | Power-On-Reset High: Enable, Low: Disable |

Pin Types

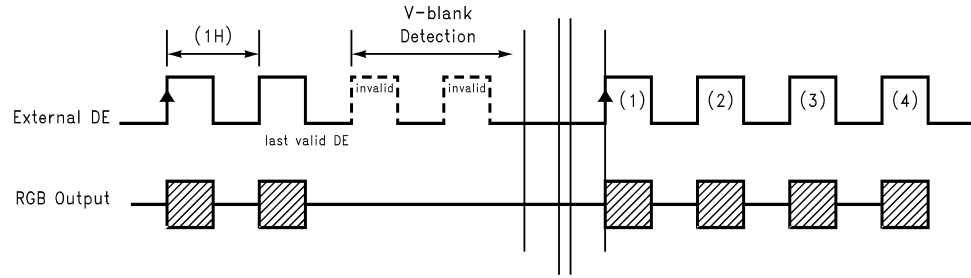
| | | | |
|-------|--|----|------------|
| I | -Input (3.3V TTL-Compatible) | G | -Ground |
| TO | -TTL Output (3.3V TTL-Compatible) | PU | -Pull-Up |
| LVDSI | -Low Voltage Differential Signal Input | PD | -Pull-Down |
| RSO | -Reduced Swing Differential Output | | |
| P | -Power | | |

Appendix 1. DE Mode Timing Details

DE Mode (Disabled SYNC Pin)

Always true whenever DE is exist as inputted signal. If V_{SYNC} , H_{SYNC} and DE are available, DE mode is superior and generate the control timing. "V-blank Detection" period is two cycles of the previous DE signals. After the V-blank detection period, "Counter" start to count whenever DE signal available followed on the rising edge.

Case 1: Disabled Failure Detection Mode



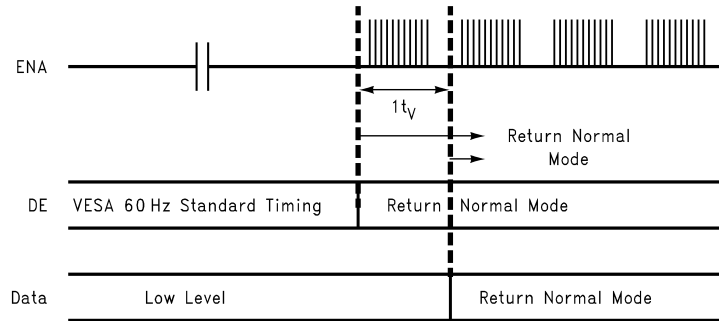
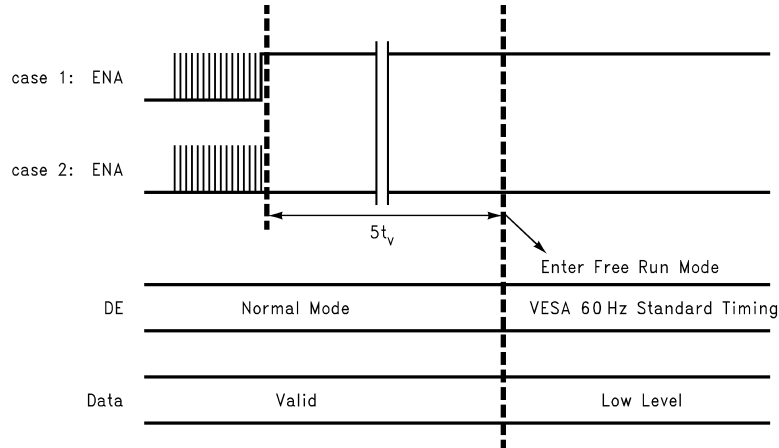
20104323

Case 2: Enabled Failure Detection Mode (SXGA). Please refer to the "Failure Detect" on page 10.

Appendix 2. Free Run Mode Function (B/O Pin FRM "Low" to Disable)

Either input DE signal, ENA, on the DE mode or V_{SYNC} on the SYNC mode are lost more than 5 frames (here, "lost" means ENA or V_{SYNC} signal more than 5 frames without change), then the TCON will enter the Free Run Mode. In the Free Run Mode, the vertical and horizontal period will follow VESA 60 Hz standard and output data will be in the Low Level.

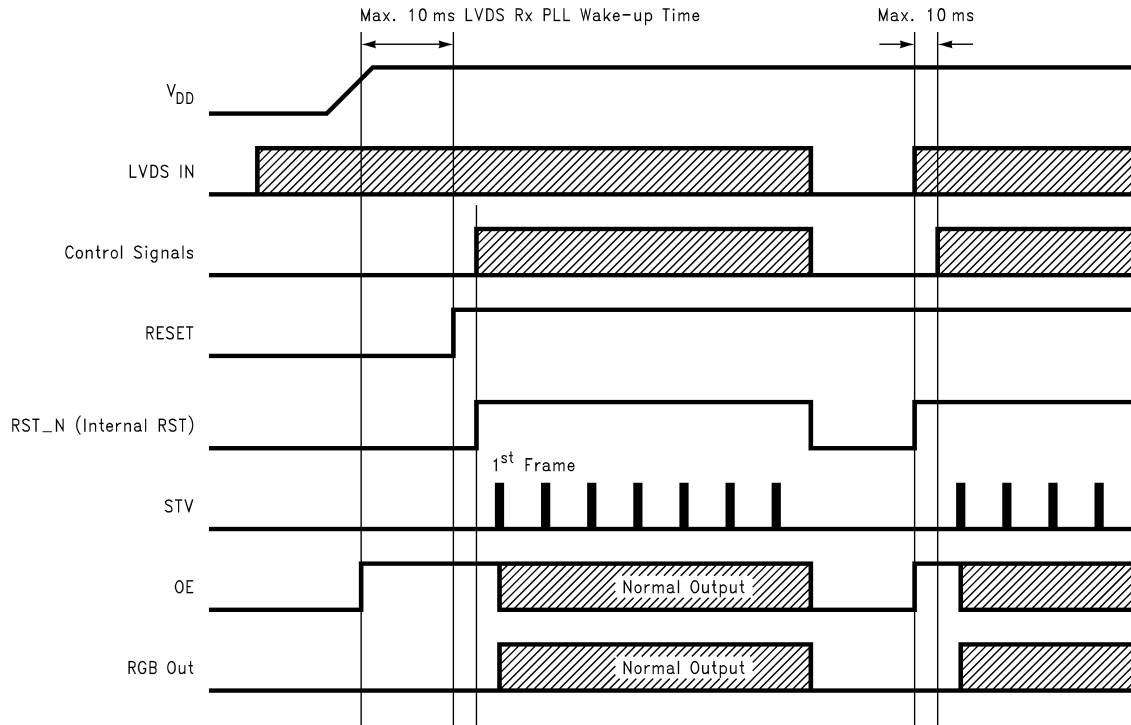
When TCON detects input signal back to normal ("normal" means ENA or V_{SYNC} signal has to change from Low Level to High Level), then output control signals will return to the Normal Mode. In the next frame, output data will also return to Normal Mode.



20104324

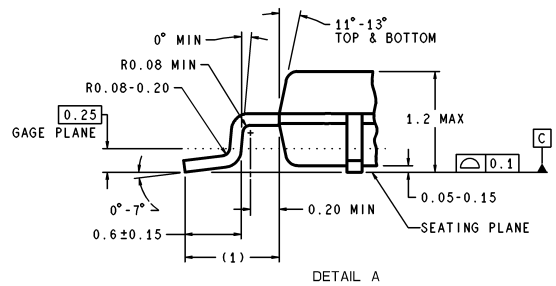
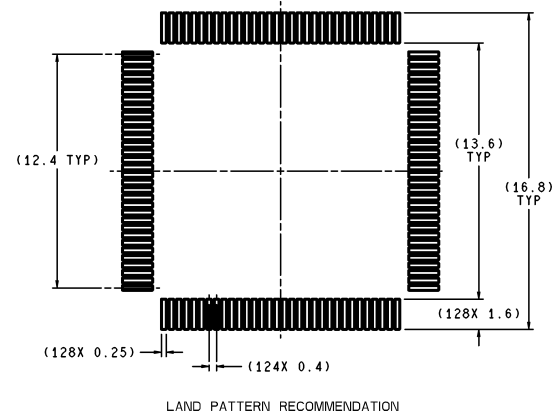
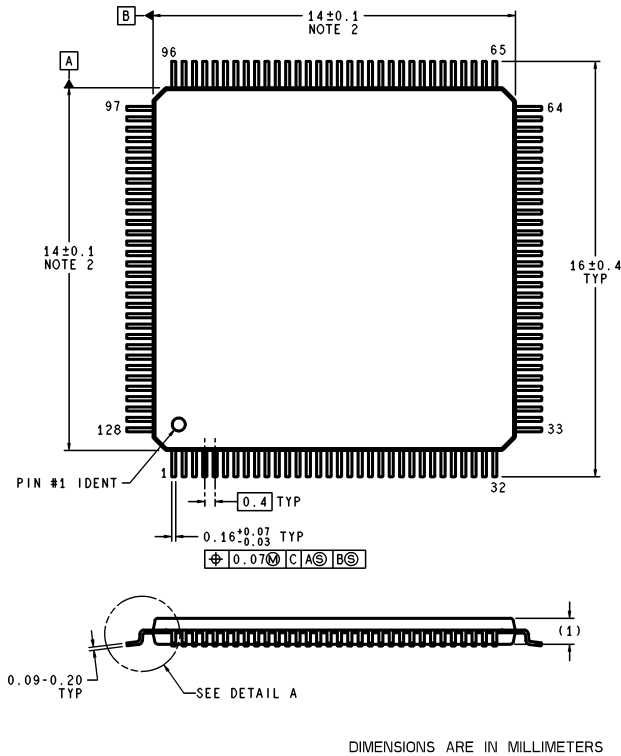
Appendix 3. Power-Up Sequence on “POR Enabled” Mode

When Bonding option pins, POR (Power-On-Reset), enable set to “High”, TCON start running as POR mode. If the input LVDS clocks lost with any reasons during the normal operation, POR output signal (RST_N) will be low until LVDS clock comeback again. The Reset counter start to count with LVDS clock resume then turn to normal operation mode before the 10 ms PLL Wake-Up time limits.



20104325

Physical Dimensions inches (millimeters) unless otherwise noted



VJX128A (Rev A)

128-lead Plastic Quad Flatpack, JEDEC
Dimensions in millimeters only
Order Number FPD87392BXBVQ
NS Package Number VJX128A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



National Semiconductor
Americas Customer
Support Center
 Email: new.feedback@nsc.com
 Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
 Fax: +49 (0) 180-530 85 86
 Email: europa.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +44 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
 Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
 Fax: 81-3-5639-7507
 Email: jpn.feedback@nsc.com
 Tel: 81-3-5639-7560

www.national.com