FPD6836P70

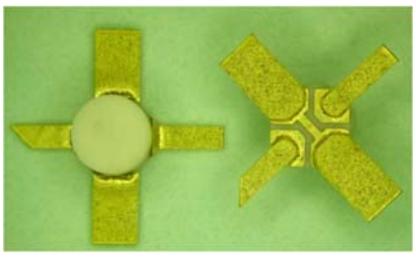
Low-Noise High-Frequency Packaged pHEMT

GENERAL DESCRIPTION

Package - P70

The FPD6836P70 is a low parasitic, surface mountable packaged depletion mode pseudomorphic High Electron Mobility Transistor (pHEMT) optimised for low-noise, high-frequency applications.

100% RoHS Compliant



Key Characteristics

- 22dBm Output Power (P_{1dB})
- 15dB Gain at 5.8GHz
- 0.8dB Noise Figure at 5.8GHz
- 32dB Output IP_3 at 5.8GHz
- 45% Power-Added Efficiency at 5.8GHz
- Usable Gain to 18GHz

Applications

- Gain blocks and medium power stages
- WiMax (2GHz to 11GHz)
- WLAN 802.11a (5.8GHz)
- Point-to-Point Radio (to 18GHz)

TYPICAL PERFORMANCE

		SPECIFICATION				
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
P_{1dB} at Gain Compression	P_{1dB}		22		dBm	V_{DS}=5V, I_{DS}=55mA
Power-Added Efficiency	PAE		45		%	V_{DS}=5V, I_{DS}=55mA, P_{OUT}=P_{1dB}
Maximum Stable Gain (|S21/S12|)	MSG		15			V_{DS}=5V, I_{DS}=55mA, f=12GHz
			12			V_{DS}=5V, I_{DS}=55mA, f=18GHz
Small-Signal Gain	SSG	14	16		dB	V_{DS}=5V, I_{DS}=55mA
Output Third-Order Intercept Point	OIP_3		32		dBm	V_{DS}=5V, I_{DS}=55mA, P_{OUT}=10dBm SCL
Saturated Drain-Source Current	I_{DSS}	90	105	135	mA	V_{DS}=1.3V, V_{GS}=0V
Maximum Drain-Source Current	I_{MAX}		215		mA	V_{DS}=1.3V, V_{GS}=+1V
Transconductance	G_M		140		mS	V_{DS}=1.3V, V_{GS}=0V
Gate-Source Leakage Current	I_{GSO}		1		µA	V_{GS}=-5V
Pinch-Off Voltage	V_P	|0.7|	|1.0|	|1.3|	V	V_{DS}=1.3V, I_{DS}=0.2mA
Gate-Source Breakdown Voltage	BV_{GS}	|12.0|	|14.0|		V	I_{GS}=0.36mA
Gate-Drain Breakdown Voltage	BV_{GD}	|14.5|	|16.0|		V	I_{GD}=0.36mA
Thermal Resistivity	θ_{JC}		275		°C/W	
Noise Figure	NF		0.8			V_{DS}=5V, I_{DS}=55mA

Note: $T_{AMBIENT}$=22°C

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage (V_{DS})	-3V<V_{GS}<0V	8V
Gate-Source Voltage (V_{GS})	0V<V_{DS}<+8V	-3V
Drain-Source Current (I_{DS})		I_{DSS}
Gate Current (I_G)	Forward or reverse	10mA
RF Input Power[2] (P_{IN})	Under any acceptable bias state	16dBm
Channel Operating Temperature (T_{CH})	Under any acceptable bias state	175°C
Storage Temperature (T_{STOR})	Non-Operating Storage	-40C to 150°C
Total Power Dissipation (P_{TOT})	See De-Rating Note below	550mW
Simultaneous Combination of Limits[3,4]	2 or more max. limits	80%

Notes:
[1]$T_{AMBIENT}$=22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
[2]Max. RF input limit must be further limited if input VSWR>2.5:1.
[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously.
[4]Total Power Dissipation (P_{TOT}) defined as (P_{DC}+P_{IN})–P_{OUT}, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power. Total Power Dissipation to be de-rated as follows above 22°C: P_{TOT}=550mW-(1/RθJC)xT_{PACK}, where T_{PACK}=source tab lead temperature above 22°C. Example: For a 65°C carrier temperature: P_{TOT}=550mW-(3.6x(65-22))=395.2mW

Caution! ESD sensitive device

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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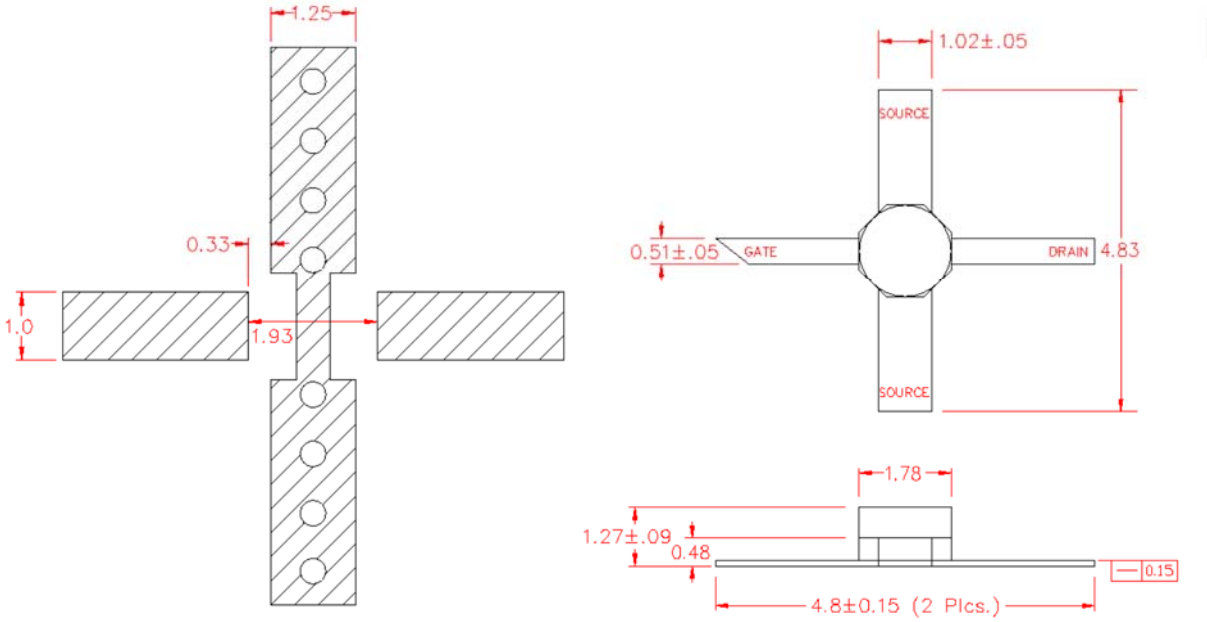
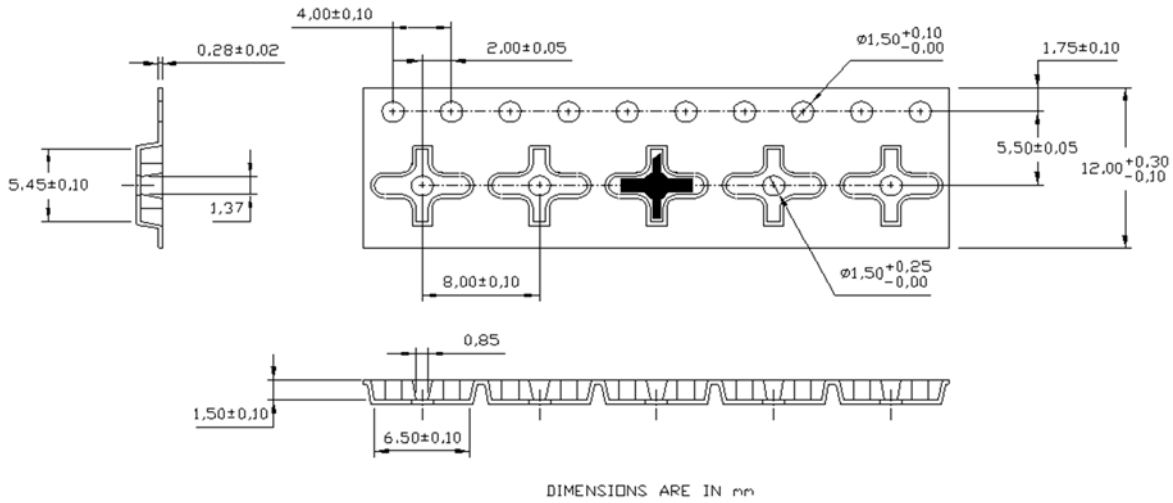
BIASING GUIDELINES

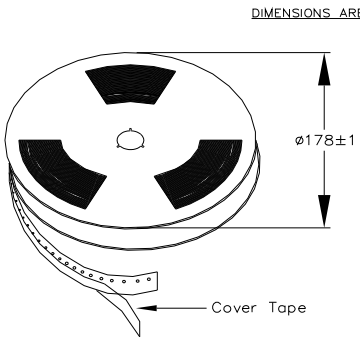
Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate.
Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD6836P70.
For standard Class A Operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are “quasi-E/D mode” devices, exhibit a Class AB trait when operated at 50% of IDSS. To achieve a larger separation between P1dB and IP3, an operating point in the 25% to 33% range is suggested. Such Class AB operation will not degrade the IP3 performance.

P70 PACKAGE OUTLINE AND RECOMMENDED PC BOARD LAYOUT



TAPE AND REEL DIMENSIONS AND PART ORIENTATION





Product Marking

The device is marked ABC where :-

A = Product type
B = Week code
C = Year code

- Terminal tape = 40mm(min.)
- Leader tape with empty Cavities = 350mm(min.)
- Trailer tape with empty Cavities = 160mm(min.)
- Devices per reel = 1000

PREFERRED ASSEMBLY INSTRUCTIONS

This package is compatible with both lead free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260°C. Package leads are gold plated.

HANDLING PRECAUTIONS

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD/MSL RATING

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. JS-001-2012.

The device has an MSL rating of Level 1. To determine this rating, preconditioning was performed to the device per the Pb-free solder profile defined within IPC/JEDEC J-STD-020, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices.

RELIABILITY

A MTTF in excess of 4 million hours at a channel temperature of 150°C is achieved for the process used to manufacture this device.

DISCLAIMERS

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION

DELIVERY QUANTITY	ORDERING CODE
Reel of 1000	FPD6836P70
Reel of 100	FPD6836P70 - 100
Bag of 3	FPD6836P70 - 003