National Semiconductor

PRELIMINARY
July 2003

FPD87392AXA
+3.3V TFT-LCD Timing Controller with Dual LVDS Inputs/Dual RSDS™ Outputs for TFT-LCD Monitor and Notebook (SXGA/SXGA+/UXGA)

General Description

The FPD87392AXA Panel Timing Controller is an integrated FPD-Link + RSDS™ + TFT-LCD Timing Controller. The logic architecture is implemented using standard and default timing controller functionality based on an Embedded Gate Array. The device is reconfigurable to the needs of a specific application by providing user-defined specifications or customer supplied VHDL/Verilog code.

The FPD87392AXA is a timing controller that combines an LVDS dual pixel input interface with National's Reduced Swing Differential Signaling (RSDS™) output column driver interface for SXGA, SXGA+ and UXGA resolutions. It resides on the TFT-LCD panel and provides the data buffering and control signal generation. The RSDS™ data path to the column driver contributes toward lowering radiated EMI and reduced system dynamic power consumption. The RSDS™ dual 12 pair differential bus conveys up to 24-bit color data for SXGA/SXGA+/UXGA panels when using VESA 60Hz standard timing.

Features

- Input frequency range from 30 MHz to 85 MHz
- Support display resolutions SXGA (1280x1024), SXGA+ (1400x1050) and UXGA (1600x1200)
- Embedded gate array for custom panel timing
- RSDS™ (Reduced Swing Differential Signaling) Column Driver bus for low power and reduced EMI
- Drives RSDS™ column driver up to 170 Mb/s with an 85 MHz clock
- 6 or 8 bit LVDS dual pixel input interface (FPD-Link)
- Virtual 8-bit color depth in FRC mode
- Flexible RSDS™ data output mapping for Bottom or Top mount
- Supports 1 and 2 line inversion mode for RVS output
- Supports Graphics Controllers with spread spectrum interface for lower EMI
- Free Run Mode Function
- Fail-safe function in DE mode (Bonding Option)
- Supports DE mode and SYNC only mode (Bonding Option)
- Power-On-Reset Support
- CMOS circuitry operates from a 2.7V to 3.6V supply
- Operation frequency: 54 MHz (max) @ V_{CC}: 2.7 ~ 3.0V
- Operation frequency: 85 MHz (max) @ V_{CC}: 3.0 ~ 3.6V
- 128 TQFP package with body size 14mm x 14mm x 1.0mm, 0.4mm Pitch

FPD87392AXA +3.3V TFT-LCD Timing Controller with Dual LVDS Inputs/Dual RSDS™ Outputs for TFT-LCD Monitor and Notebook (SXGA/SXGA+/UXGA)

System Diagram

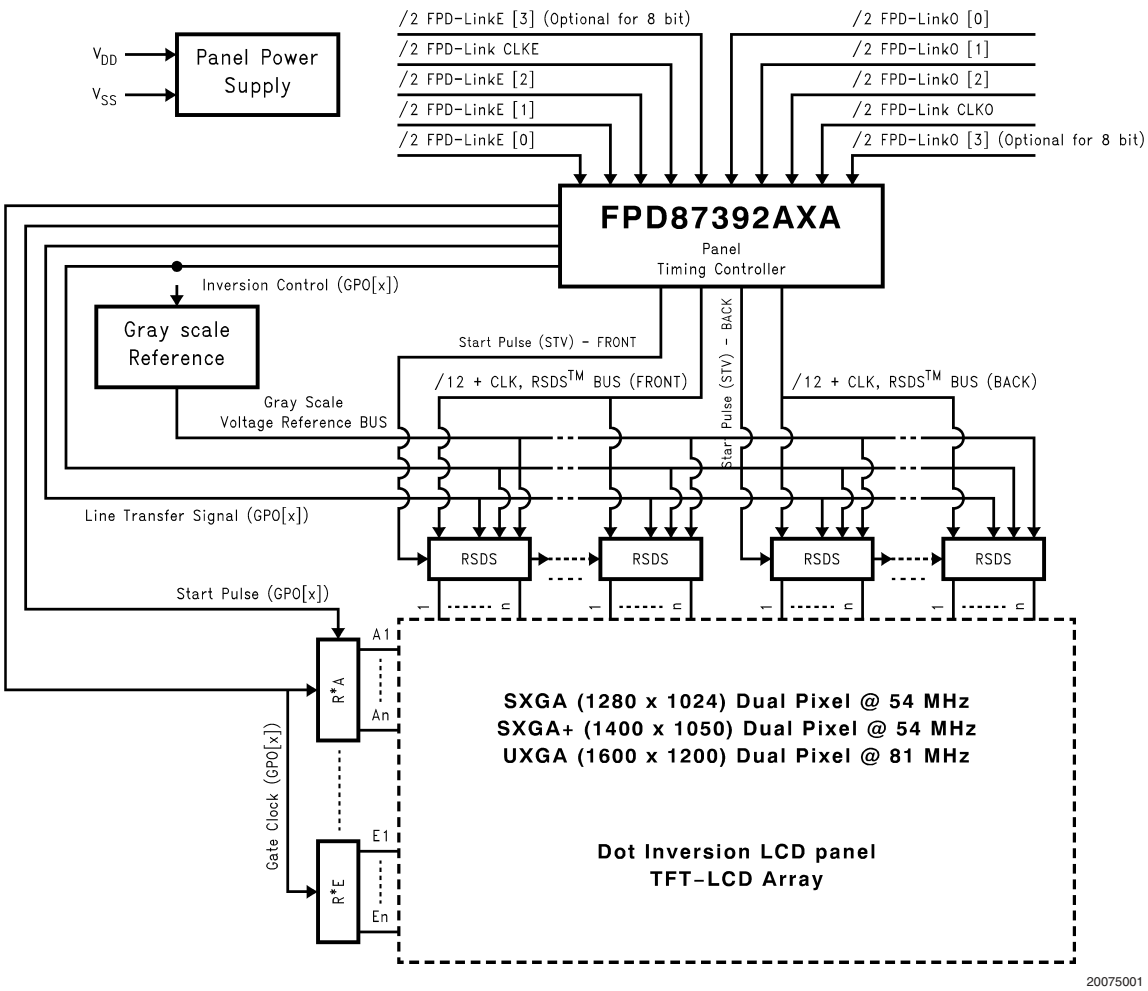


FIGURE 1. Block Diagram of the LCD Module

Block Diagram

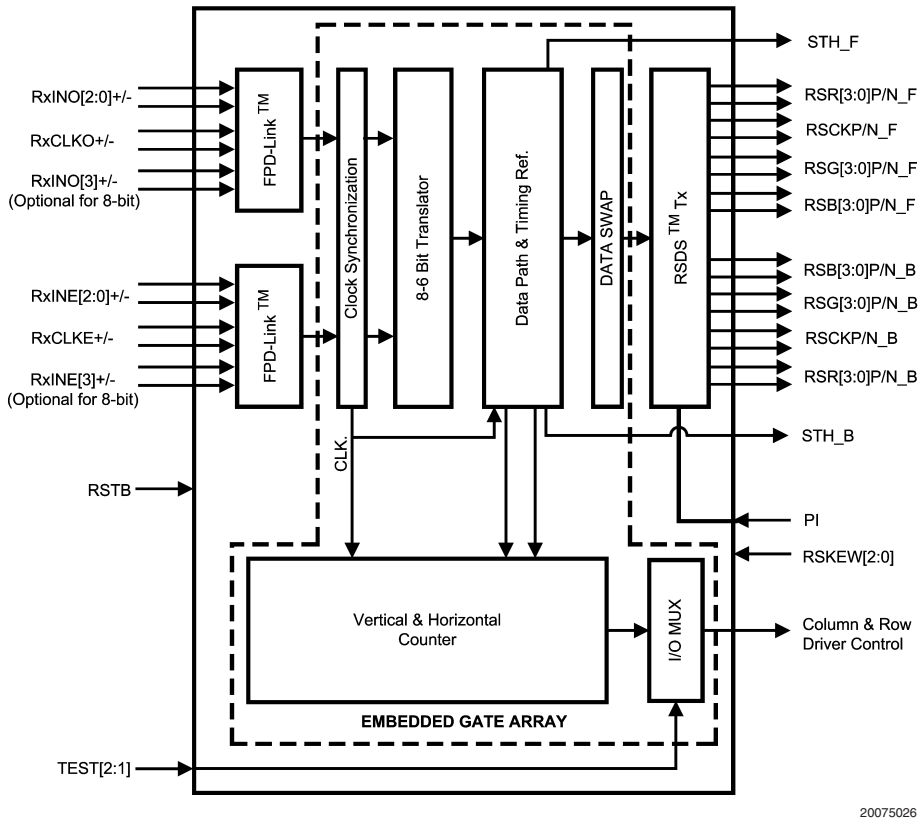


FIGURE 2. Block Diagram

Functional Description

DUAL FPD-LINK RECEIVERS

The LVDS based FPD-Link Receivers inputs video data and control timing through 8 pairs of LVDS channels plus 2 pairs of LVDS clocks to provide 24-bit color or use only 6 pairs of LVDS channels plus 2 LVDS clocks to provide 18-bit color. The video data is converted to a parallel data stream and routed to the 8-6 bit translator.

SPREAD SPECTRUM SUPPORT

The FPD-Link receiver supports graphics controllers with Spread Spectrum interfaces for reducing EMI. The Spread Spectrum methods supported are Center and Down Spread. A maximum of 2% total is supported at a frequency modulation of 100kHz maximum.

8-6 BIT TRANSLATOR

8-bit data is reduced to a 6-bit data path via a time multiplexed dithering technique or simple truncation of the LSBs. This function is enabled via the input control pins.

DATAPATH BLOCK AND RSDS TRANSMITTER

6(8)-bit video data (RGB) is input to the Datapath Block supports up to an 85 MHz dual pixel rate. The data is delayed to align the Column Driver Start Pulse (STH) with the Column Driver data. The dual data bus (RSR[3:0]P/N, RSG[3:0]P/N, RSB[3:0]P/N) outputs at a 170 MHz rate on 24 differential output channels. The clock is output on the (Front, Back) RSCKP/N differential pairs. The RSDS Column Drivers latch data on both positive and negative edges of the clock. The swap function provides flexible RSDS data output mappings for either Top or Bottom mount. The RSDS output setup/hold timings are also adjustable through the RSKEW[2:0] input pins.

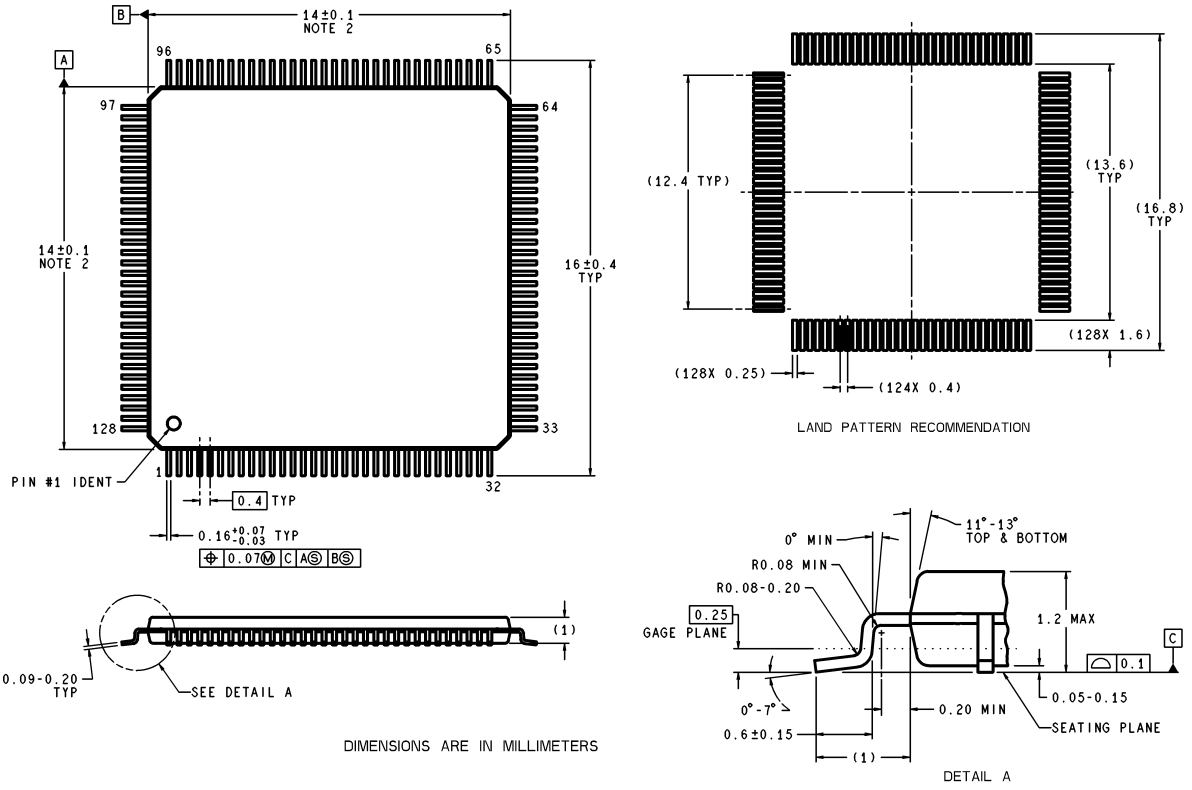
TIMING CONTROL FUNCTION

The Timing Control function generates control to Column Drivers, Row Drivers, and power supply. The GPOs (General Purpose Outputs) provide for CD latch pulse, REV, and Row Driver control generation. The General Purpose Outputs allow the user to generate control anywhere within the frame data. Standard Row Driver interface or Custom Row Driver interfaces can be implemented with the GPOs (General Purpose Outputs).

RSDS OUTPUT VOLTAGE CONTROL

The RSDS output voltage swing is controlled through an external load resistor connected to the RPI pin. The RSDS output signal levels can be adjusted to suit the particular application. This is dependent on overall LCD module design characteristics such as trace impedance, termination, etc. The RSDS output voltage is inversely related to the RPI value. Lower RPI values will increase the RSDS output voltage swing and consequently overall power consumption will also increase.

Physical Dimensions inches (millimeters) unless otherwise noted



Plastic Quad Flatpack, JEDEC
NS Package Number VJX128A

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