National Semiconductor

September 2007

FPD95320
320-Channel LTPS/CGS Driver with Partial Display Memory and MPL-1 Interface

General Description

The FPD95320 is a 320–channel LTPS/CGS driver with Partial Display Memory, a 18-bit RGB video interface and enhanced display quality. It provides 320 output source drivers with a 1:3 glass multiplex ratio. It includes a 230,400-bit memory for partial display modes, a timing controller with glass interface level-shifters, AC and DC V_{COM} drive schemes and glass power supply circuits. The output format can be configured to drive arbitrary display resolutions up to 320 RGB x 480. Advanced processing features enable up-scaling of incoming video to accommodate legacy graphics. There is also an upscale function for the Partial Display window to enable larger window sizes.

The on-chip Partial Display Memory is configurable in window size, location and color depth. This memory can support partial display windows such as 240x320 in 3-bit mode and 320x480 in 1-bit color mode. The partial display memory can be used to self-refresh a region of the display in a reduced power state or as an overlay for OSD and alpha-blending features. The FPD95320 also includes independent RGB gamma curve adjustments as well as user-definable color palettes for 1-bit and 3-bit Partial Display modes.

A low-speed serial interface is provided to control display operating modes and provide access to the Partial Display Memory. This interface can support both 8-bit and 9-bit protocols. A standard command set is supported to set display modes and operating parameters. Customized register profiles associated with each command are loaded from an on-chip EEPROM. Registers can also be directly accessed by using the Register Access Mode.

Features

■ **Power Savings**
■ Self-refreshed Partial Display Mode
■ Provides timing signal for on-glass charge-sharing circuit
■ **Standard Command Set**
■ Registers initialized from on-chip EEPROM
■ Command-triggered profiles can change register settings for modes/gamma settings
■ Eliminates frequent host SW changes to update register settings
■ 8 user-defined display configurations
■ **Programmable Settings**
■ Display resolution and glass signal timing
■ Video interface timing auto-learning circuit
■ VID_XFR output reduces tearing in partial mode
■ Gamma curves and V_{COM} adjustment
■ Video 2x upscale with programmable border
■ **Partial Display**
■ Configurable Partial Mode Window size, location and color depth
■ Self-refreshed partial display mode supports 1-bit and 3-bit depths
■ OSD function with Partial RAM data in video mode
■ Alpha blending, including transparent mode
■ Partial Window 2x upscale with border color
■ **Interfaces**
■ Low-Speed Serial Interface for commands, register access and partial memory access
■ 18-bit RGB Video interface
■ MPL1 high-speed serial interface

System Diagrams
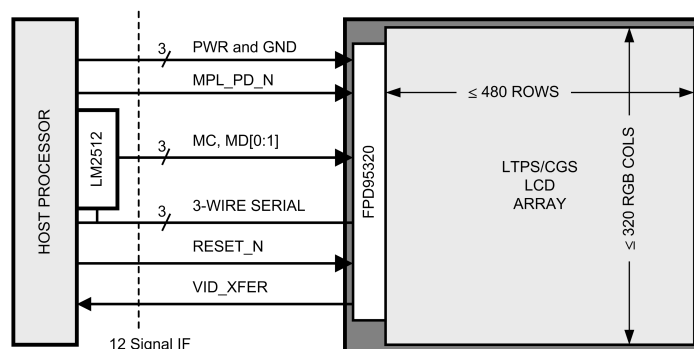
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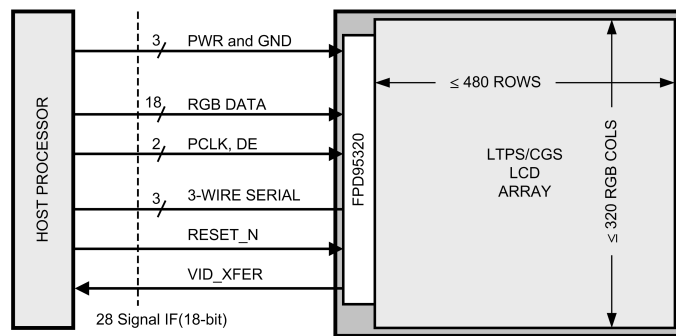
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