

Multi-standard desktop video modules

Rev.k — 14.06.2007

Product data sheet

1. General description

The FQ1216ME belongs to the new MK5 family of small size frontends, especially developed for LCD-TV application where a low noise figure and best-in-class performance is desired. The FQ1216ME combines the functions of an all-band TV tuner, and a multi-standard TV IF demodulation unit for both positive and negative modulated TV systems. The FQ1216ME is intended for CCIR L/L' (France), B/G, I and D/K systems.

The frontends have a built-in digital (I^2C) PLL tuning system. A DC-DC converter circuit is built-in in the FQ1216ME to synthesize the tuning voltage required, thus making the frontend a true 5 V device.

The FQ1216ME fulfills the requirement of IEC 60950-1 (2nd Edition) in respect of chapter 7 for Electric Strength Test and Impulse Test

For PIP/Double Window application, a second module address can be set for both the tuner and IF part. The footprint is identical to the Mk3, but the overall thickness is lower.

Table 1. Int	ermediate frequ	uencies			
System	L	Ľ'	B/G	D/K	I
Picture carrier	38.90 MHz	33.95 MHz	38.90 MHz	38.90 MHz	38.90 MHz
Color carrier	34.47 MHz	38.38 MHz	34.47 MHz	34.47 MHz	34.47 MHz
Sound 1	32.40 MHz	40.40 MHz	33.40 MHz	32.40 MHz	32.90 MHz
Sound 2	-	-	33.16 MHz	-	-
NICAM	33.05 MHz	39.80 MHz	33.05 MHz	33.05 MHz	32.348 MHz

Table 2. Cha	nnel coverage	
Band	Frequency range (MHz)	
Low band	48.25 to 158.00 ^[1]	
Mid band	160.00 to 442.00	
High band	442.00 to 863.25	

I] Can cover down to 45.75 MHz (Ch A for Ireland). Does not guarantee Ch FA (47.75 MHz) for L'



2. Features

- Multi-Standard TV Systems Broadcast reception
- Especially developed for LCD-TV / PDP application
- New input configuration (patent pending) results in Best-in-Class noise figure typically 5.5 dB in UHF
- True 5 V device (low power consumption compared to Mk3)
- Full frequency range from 48.25 MHz to 863.25 MHz
- PLL controlled tuning
- True-synchronous vision IF demodulator (PLL)
- Ultra linear FM PLL demodulator
- Demodulated video output, AF sound output, second IF sound output.
- I²C-bus control of tuning, address selection, AFC status information
- User-settable 2nd IF address for PIP application
- Complies with European regulations on radiation, signal handling and immunity (CENELEC 55020, 55013)
- Complies to CISPR13 (4th edition) including amendment 1 (1992) and amendment
- Fulfills the requirement of IEC 60950-1 (2nd edition) in respect of chapter 7 for Electric Strength Test and Impulse Test
- Low profile horizontally mounted metal 70 mm housing
- · Environmentally friendly lead-free process used
- Suitable for lead-free wave soldering

3. Applications

- STB
- LCD / Plasma TV
- PC-TV cards

4. Ordering information

Table 3. Ordering information

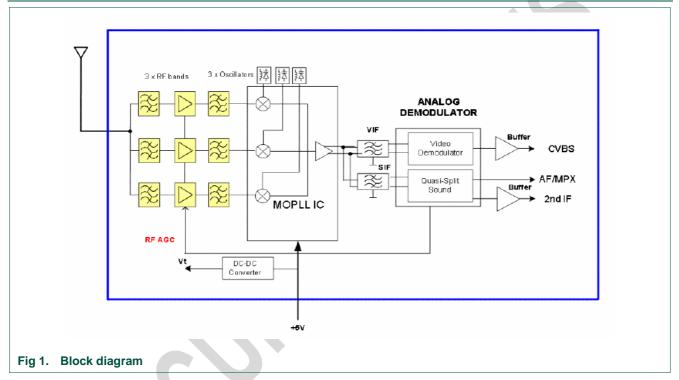
Type number	Package		
	Name	Description	Version
FQ1216ME/I H-5	3139 147 22641	IEC connector / Horizontal mounting	-
FQ1216ME/I V-5	3139 147 22981	IEC connector / Vertical mounting	-
FQ1216ME/P H-5	3139 147 22991	Phono connector / Horizontal mounting	-
FQ1216ME/P V-5	3139 147 23001	Phono connector / Vertical mounting	-
FQ1216ME/L H-5	3139 147 24061	Long IEC connector / Horizontal mounting	-

5. Marking

The following information is printed on a sticker that is on the top cover of the module

- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code

6. Block diagram



7. Pinning information

Pin namePinDescriptionN.C1(AGC monitor) do not connect [1]N.C2(Tuning voltage monitor) do not connect [1]+5 V3Supply voltage Vb, Tuner sectionSCL4I ² C-Bus Serial ClockSDA5I ² C-Bus Serial DataAS_TU6I ² C address Select Tuner Part	Table 4. Pin d	description	
N.C 2 (Tuning voltage monitor) do not connect ^[1] +5 V 3 Supply voltage Vb, Tuner section SCL 4 I ² C-Bus Serial Clock SDA 5 I ² C-Bus Serial Data	Pin name	Pin	Description
+5 V 3 Supply voltage Vb, Tuner section SCL 4 I ² C-Bus Serial Clock SDA 5 I ² C-Bus Serial Data	N.C	1	(AGC monitor) do not connect ^[1]
SCL 4 I ² C-Bus Serial Clock SDA 5 I ² C-Bus Serial Data	N.C	2	(Tuning voltage monitor) do not connect ^[1]
SDA 5 l ² C-Bus Serial Data	+5 V	3	Supply voltage Vb, Tuner section
	SCL	4	I ² C-Bus Serial Clock
AS THE 6 I^2C address Solect Typer Part	SDA	5	I ² C-Bus Serial Data
	AS_TU	6	I ² C-address Select - Tuner Part

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Pin name	Pin	Description
-	х	Not connected
-	х	Not connected
N.C	9	Not connected
AS_IF	10	I ² C-address Select – IF Part
2 nd _IF sound	11	Second IF sound output
CVBS	12	Composite video baseband signal
+5V IF	13	Supply voltage, IF section
AF_O/P	14	AF sound output
GND		Mounting Tags (TH1, TH2, TH3, TH4)

[1] For process use only

8. Limiting values

Table 5. Limiting values under operational conditions

The tuners are guaranteed to function properly under the following conditions.

Symbol	Parameter	Pin		Min	Тур	Max	Unit
V _{AGC}	AGC voltage monitor	1	[1]	10	-	-	MΩ
V _{cc}	Supply voltage	3		4.75	5	5.25	V
V _{ripple}	Ripple voltage susceptibility 20 Hz to 1 kHz		[2]	-	-	5	mV₽
	1 kHz to 200 kHz			-	-	10	mV _P
Icc	Supply current at 5 V			-	65	100	mA
V _{SCL}	Voltage on pin SCL	4		-0.3	-	5.25	V
V _{SDA}	Voltage on pin SDA	5					
	High level			3	-	5.5	V
	Low level			-0.3	-	1.5	V
I _{SDA}	current on pin SDA (open collector)			-1.0	-	5	mA
-	AS voltage	6	<u>[3]</u>	-	-	5.25	V
2 nd IF sou	ind output						
$Z_{\text{L(DC)}}$	load impedance DC	11		1.0	-	-	kΩ
	load impedance AC			1.0	_	_	kΩ

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Symbol	Parameter	Pin	Min	Тур	Max	Unit
$Z_{\text{L(DC)}}$	load impedance DC	12	75	-	-	Ω
$Z_{\text{L(AC)}}$	load impedance AC		75	-	-	Ω
$\tau_{\text{(load)}}$	load time constant		-	-	100	ns
IF section	I					
V _{CC}	Supply voltage	13	4.75	5	5.25	V
V _{ripple}	Ripple susceptibility	[2	1			
	20 Hz to 1 kHz		-		5	mV_{PP}
	1 kHz to 500 kHz		-	-	10	mV_{PP}
Icc	Supply current at 5 V		-	100	130	mA
AF Outpu	t					
$Z_{\text{L(DC)}}$	load impedance DC	14	100.0	-	-	kΩ
Z _{L(AC)}	load impedance AC		10.0	-	-	kΩ

[1] Minimum impedance required is 10 M_{Ω} , otherwise AGC voltage is loaded down. For process only

[2] Maximum allowable ripple voltage superimposed on the +5 V supply in the frequency range from 20 Hz to 500 kHz. Criteria: for TV: Δf < 2.12 kHz or AM < 0.28 %

[3] For detailed information about address coding, refer to Application Information

Table 6. Limiting values under environmental conditions

Symbol	Parameter	Conditions		Min	Max	Unit
Non-opera	tional Conditions					
T _{amb}	ambient temperature			-25	+85	°C
RH	relative humidity			-	100	%
gв	bump acceleration	25 g		-	245	m/s ²
gs	shock acceleration	50 g		-	490	m/s ²
	vibration amplitude	10 Hz to 55 Hz		-	0.35	mm
Operationa	al Conditions					
T _{amb}	ambient temperature		[1]	0	+70	°C
RH	relative humidity			-	95	%

[1] The typical MTBF is about 20,000 hours at this operational ambient temperature. For every 10 °C increase, the MTBF is reduced by half.

9. Static Characteristics

9.1 Overall performance

Unless otherwise specified, all electrical values for overall performance apply at the following conditions.

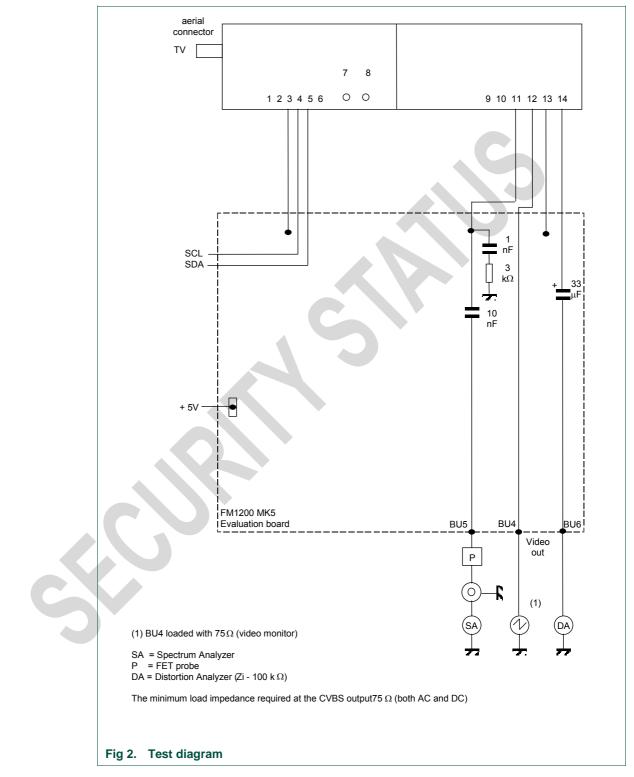
Table 7.	Static characteristics (con	ditional data)				
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb}	ambient temperature		-	25 ± 5	-	°C
RH	relative humidity		-	60 ± 15	-	%
Vcc	supply voltage	tuner and IF section	-	5 ± 0.125	-	V
Zs	source impedance	unbalanced	-	75	-	Ω
$Z_{O(2nd_IF)}$	second IF sound output load		-	0.5	-	kΩ
Z _{O(video)}	video output load		-	75	-	Ω
Z _{O(AF)}	AF1 sound output load		-	100	-	kΩ

Table 8. Static characteristics (Test equipment)

Equipment	Parameter	Min	Тур	Мах	Unit
DC voltmeter	input impedance	-	10	-	MΩ
Oscilloscope	input impedance resistance	-	1	-	MΩ
	input impedance capacitance	-	15	-	pF
Spectrum analyzer	input impedance	-	50	-	Ω
FET probe	input impedance resistance	-	10	-	MΩ
	input impedance capacitance	-	3.5	-	pF

9.2 Test diagram

The frontend characteristics are measured according to the test diagram.



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Test	sign	al	Frequency (MHz)	Amplitude	Modulatio	on		
A0	Un-ı carr	nodulated vision er	480.25	$60 \ dB\mu V$				
A1		stem signal with o modulation	480.25	60 dBμV (peak white)	100 % (sy pulse and indicated			
A2		/D/K/I–system signal video modulation	480.25	60 dBμV (top sync)	100 % (re and bar, ι			
A3		ystem signal with o modulation	55.75	60 dBμV (peak white)	100 % (sy and bar, ι			
B1	sour	modulated main nd carrier B/G/I/D/K em as chosen	A2 + 5.5/6.0/6.5 MHz	-13 dB respectively wrt A2		3		
B2		modulated sound er L system	486.75 MHz	-10 dB with respect to test signal A0 or A1	m = 0.54, kHz, unles			
В3	sour	modulated main nd carrier B/G/I/D/K em respectively	A2 + 5.5/6.0/6.5 MHz	-13 dB respectively wrt A2	frequency modulatio pre-emph indicated	n freque	ncy 1 kH	z, 50 µ
B4		modulated 2 nd sound er B/G system	A2 + 5.85 MHz	–20 dB respectively wrt A2				
B5		modulated main nd carrier L system	A1 + 6.5 MHz	–10 dB wrt test signal A1				
B6		modulated sound er L' system	A3 – 6.5 MHz	–10 dB with test signal A3	m = 0.54, kHz, unles			
Table	10.	Static characterist	ics (Aerial inp	out)				
Sym	bol	Parameter	Conditio	ns		Min	Max	Uni
VSW	′R		Referred carrier fre	to 75 Ω at RF p quency	icture	-	5	
Vant		antenna terminal disturbance voltage	Up to 1.7	5 GHz		-	46	dBµ

Table 9. Static characteristics (Definitions of test signals)

10. Dynamic Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Uni
f _b	Frequency range					
	low band		48.25	-	158.00	MH
	mid band		160.00	-	442.00	MH
	high band		442.00	-	863.25	MH
Δf_b	Margin					
	low band		1.5		•	MH
-	mid band		1.5	-	-	MH
	high band		1.5		-	MH
Gv	Voltage gain					
	low band		40	46	52	dB
	mid band		40	46	52	dB
	high band		40	46	50	dB
NF	Noise figure					
	low band		-	5.5	8.0	dB
	mid band		-	5.5	8.0	dB
	high band		-	5.5	8.0	dB
α_{image}	Image rejection	- wanted test signal F _{ant} at				
		- Un-wanted test signal at	(F _{ant} + 77.7	MHz)		
	low band		68	75	-	dB
	mid band		62	70	-	dB
	high band		52	62	-	dB
αIF	IF rejection All band	- wanted test signal F _{ant} - Un-wanted test signal A0 with frequency (F _{IF,PC} – 1 MHz)	60	75	-	dB
tıj	Oscillators lock-in time	Tuning speed (lock bit, CP = 1)	-	-	100	ms

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Symbol	Parameter	Conditions		Min	Т	ур	Max	Unit
V _{ESD}	ESD protection at the terminals	All terminals of frontend are pro against electros discharge up to products are cla in category B (N STD-883C).	otected static the assified	2	-		-	
	Maximum signal handling	F _{wanted}		100	1	10	-	dBµV
Table 12. Base on re	Dynamic characte					C		
Paramete	er	Test sign	al Test p	point I	Min	Тур	Max	Unit
CVBS ou	tput amplitude	A1	BU4	().7	1.0	1.3	V_{PP}
DC level	of sync pulse	A1	BU4			0.35	-	V
CVBS an	nplitude response at	1 MHz						
2 MHz		A1	BU4	-		0.0	-1.0	dB
3 MHz		A1	BU4	-		-0.5	-2.5	dB
4.43 MHz	2	A1	BU4	-		-0.5	-3.5	dB
specificat	arriers rejection, tion valid for B/G, I ar e wrt 1 MHz	A2 + B1 + B4 BU4						
5.5 / 6.0	MHz			2	45	50	-	dB
6.5 MHz				2	45	50	-	dB
noise rati	tion valid for L/L', B/C mode		or A3 BU4	2	11	46	-	dB
Noise lim dB, un-we	ited sensitivity (S/N 3 eighted)	30 A1 or A2 o	or A3 BU4	-		41	46	dΒμ
video sigi	ted sensitivity (–1 dB nal) vel of test signal	A2	BU4	-		23	33	dΒμ
Ondeau	d IF level (all system	$(a) \qquad A1 \text{ or } A2$	or A3 BU5	(90	103		dBµ

Parameter	Test signal	Test point	Min	Тур	Max	Unit
Audio output characteristics, specification valid for B/G, D/K and I modes	A2 + B3	BU6	400	480	600	mVrm
AF output level (C7 = 0), measured via LP 20 kHz filter, RMS detector 50 μ s de-emphasis for AF1 at 1 kHz (C5 = 1, C6 = 1)						
$(\dot{C}5 = 0)$ modulation = 54 %	A1 + B2 or A3 + B6	BU6	400	500	600	mVrm
AF output level (C7 = 0)						
Specification valid for B/G, D/K and I modes THD (total harmonic distortion)	A2 + B3	BU6		0.2	0.6	%
		- i				
Signal-to-noise ratio measured via LP 20 kHz filter, RMS detector 50 μ s de-emphasis for AF1 at 1 kHz (C5 = 1, C6 = 1)	A2 + B3	BU6	52	60	-	dB
Specification valid for L/L' mode THD (total harmonic distortion)	A1 + B2 or A3 + B6	BU6	-	0.8	1.5	%
Signal-to–noise ratio measured via LP 20 kHz filter, RMS detector for AF1 at 1 kHz	A1 + B2 or A3 + B6	BU6	42	50	-	dB
Specification valid for B/G, D/K and I modes (S/N = 40 dB) (C5 = 1, C6 = 1) Audio sensitivity	A2 + B3	BU6	-	23	40	dBμV
Specification valid for L/L' mode (S/N = 38 dB) Audio sensitivity	A1 + B2 or A3 + B6	BU6	-	35	45	dBμV

Table 13. Dynamic characteristics (Audio)

11. Application information

11.1 Demonstration kit

A demonstration kit is available for the FQ1216ME MK5 (software, application note and evaluation board).

Please contact your local sales engineer for details about the price and availability.

11.2 I²C programming

For information regarding general aspects of I²C-Bus control see "The I²C-Bus Specifications", published by NXP Semiconductors on the website <u>www.nxp.com</u>

The FQ1216ME MK5 contains two I^2C transceivers, one in the tuner part and one in the IF part. It is imperative to ensure that both I^2C devices are programmed correctly according to their addresses

If in doubt, please refer to the demonstration software

11.3 Tuner part programming

11.3.1 Write mode

Table 14.BIT allocation

Write mode, R/W = 0

Write data	Byte	MSB							LSB	АСК
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/W=0	А
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8	А
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0	А
Control byte	СВ	1	CP	T2	T1	Т0	RSA	RSB	WSB=0	А
Bandswitch byte	вв	Х	Х	Х	P4	P3	P2	P1	P0	А

Table 15. Address selection (byte ADB)

If the AS pin is left floating, the internal biasing will automatically set the tuner address to C2.

Voltage at terminal 6	Address	MA1	MA0
0 V to 0.5 V	CO	0	0
1.5 V to 2.0 V	C2	0	1
2.0 V to 3.0 V	C4	1	0
4.5 V to 5.0 V	C6	1	1

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Table 16. Programmable divider setting (bytes DB1 and DB2)

Divider ratio : $N = F_{OSC}/F_{ss}$

where $F_{OSC} = (F_{RF} + F_{IF}^{[1]})$ and F_{ss} is the step-size set by RSA and RSB as described below

N = 8192*N13 + 4096*N12 + 2048*N11 + 1024*N10 + 512*N9 + 256*N8 + 128*N7 + 64*N6 + 32*N5 + 16*N4 + 8*N3 + 4*N2 + 2*N1 + N0

[1] F = 38.9 MHz, except for L' mode. In this case F = 33.95 MHz

Table 17. Control byte (CB)

Charge pump setting

CP can be set to either 0 (low current) or 1 (high current)

- CP = 1, charge pump current = 280 µA results in fastest tuning (default mode)
- CP = 0, charge pump current = $60 \ \mu$ A results in moderate speed tuning with better residual oscillator

PLL Disabling

OS = 0, for normal operation

OS = 1, switches off the PLL tuning amplifier (PLL tuning is disabled)

Weak signal booster

WSB must be set to 0

otherwise tuner overload will occur

Table 18. Test mode setting

T2	T1	ТО	Test mode
0	0	0	Normal mode (read and write mode bytes allowed)
0	0	1	Normal mode (read and write mode bytes allowed) $^{\mbox{\scriptsize [1]}}$
0	1	0	Charge pump is off
0	1	1	Byte BB ignored
1	0	0	Charge pump sinks current
1	0	1	Charge pump sources current
1	1	0	1/2 f ref output from port P3
1	1	1	1/2 f ref output from port P3

[1] Default mode at power-on reset

Table 19. Reference divider ratio select bits

RSA	RSB	Reference frequency / Step size	Remarks
0	1	31.25 kHz	Slow picture search
1	1	62.5 kHz	Normal picture search

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Ports	P0	P1	P2	P3	P4
Low band	1	0	0	0	0
Mid band	0	1	0	0	0
High band	0	0	1	0	0

11.3.2 Read mode

Read mode, R/W Name	Byte	MSB							LSB	ACK
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	_
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/W=1	А
Status byte	SB	POR	FL	1	1	AGC	A2	A1	A0	А

The following data can be read from the device through the status byte.

• POR (power on reset)

. .

POR is internally set to 1 in case V_{cc} drops below 3 V. The POR bit is reset when an end of data is detected by the PLL-IC.

• FL (in lock flag) (FL = 1 when the phase lock loop is in lock)

The loop must be phase-locked during for at least 8 periods of the internal 7.8125 kHz reference frequency 1 msec before the FL flag is internally set to 1

11.4 IF part programming

The IF uses the new TDA9886 demodulation IC from NXP Semiconductors.

11.4.1 I²C bus control – format to write mode

S	Slave receives Slave address		W = 0	А	SAD	А	DATA	А	Р		
Descripti	on of Bit										
Bit		Function									
S		Start co	Start condition								
Standard	Slave address	100 0011X, where X is the value of R/W, see <u>Table 23</u>									
R/W = 0		Write mode									
A		Acknow	ledge, g	generate	d by slave						
Sub addr	ess (SAD)	See <u>Ta</u>	<u>ble 24</u>								
DATA		Bytes B, C and E (described below)									
Р		Stop condition									

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Table 23. Slave address

Value (hex)	A6	A5	A4	A3	A2	A1	A0	R/W
86 ^[1]	1	0	0	0	0	1	1	0
84 ^[2]	1	0	0	0	0	1	0	0

[1] Default address = 86 (hex) pin 10 open

[2] Alternate address = 84 (hex), 2nd tuner for PIP application, connect pin 10 with 2k2 resistor to ground

Table 24.Sub address byte (SAD)The first byte after slave address.

Data byte following SAD	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Switching (B data)	0	0	х	х	x	X	0	0
Adjust (C data)	0	0	0	0	0	0	0	1
Data (E data)	0	0	0	0	0	0	1	0

Table 25. Description of the bits of the various data bytes

B data B0 Switching video mode (sound trap)	
B1 Switching auto mute FM	
B2 Switching carrier mode	
B3 and B4 Switching TV standard positive/negative modulation (33 = 0)
B5 Switching forced mute audio	
B6 Switching not used	
B7 Switching L/L' Sound	
C data C0 to C4 Adjust TOP adjustment	
C5 and C6 Adjust de-emphasis	
C7 Adjust audio gain	
E data E0 and E1 Data standard sound carrier	
E2 to E4 Data standard video IF	
E5 Data VIF, SIF and tuner minimum gain	
E6 Data L standard PLL gating HIGH	
E7 Data VIF-AGC	

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		e over adjus			
C4	C3	C2	C1	CO	TOP adjustment (dB)
1	1	1	1	1	+15
1	1	1	1	0	+14
1	1	1	0	1	+13
1	1	1	0	0	+12
1	1	0	1	1	+11
1	1	0	1	0	+10
1	1	0	0	1	+9
1	1	0	0	0	+8
1	0	1	1	1	+7
1	0	1	1	0	+6
1	0	1	0	1	+5
1	0	1	0	0	+4
1	0	0	1	1	+3
1	0	0	1	0	+2
1	0	0	0	1	+1
1	0	0	0	0	+0
0	1	1	1	1	-1
0	1	1	1	0	-2
0	1	1	0	1	-3
0	1	1	0	0	-4
0	1	0	1	1	-5
0	1	0	1	0	-6
0	1	0	0	1	-7
0	1	0	0	0	-8
0	0	1	1	1	-9
0	0	1	1	0	-10
0	0	1	0	1	-11
0	0	1	0	0	-12
0	0	0	1	1	-13
0	0	0	1	0	-14

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C4	C3	C2	C1	C0	TOP adjustment (dB)
0	0	0	0	1	-15
0	0	0	0	0	-16

Table 27. Optimum setting

Optimum setting between overall picture quality and signal handling to fulfill CISPR20 / EN55020 requirements it is recommended to use these settings

Haussian augtomore	have the chains to	make their own setting
However clistomers	nave the choice to	make their own setting

Top setting	B/G/DK/I	L/L'
Low band	+0 dB	+0 dB
Mid band	-2 dB	-2 dB
High band	+0 dB	–2 dB

Table 28. Consolidated programming for TV systems

Description	Bits	TV sy	stem	s	Force audio mute		
		B/G	T	D/K	L	Ľ'	
Video trap bypass	B0	0	0	0	0	0	х
Auto mute FM	B1	1	1	1	1	1	Х
Carrier mode	B2	1	1	1	1	1	Х
FM mode	В3	0	0	0	0	0	Х
TV modulation	B4	1	1	1	0	0	Х
Forced mute audio	B5	0	0	0	0	0	1
Not used (OP1)	B6	1	1	1	1	1	Х
L/L' sound (OP2)	B7	0	0	0	0	1	Х
TOP adjustment	C0	0	0	0	0	0	Х
	C1	1	1	1	0	0	Х
	C2	0	0	0	0	0	Х
	C3	0	0	0	0	0	Х
	C4	1	1	1	1	1	Х
De-emphasis	C5	1	1	1	0	0	Х
De-emphasis time	C6	1	1	1	1	1	Х
Audio gain	C7	0	0	0	0	0	Х
Sound inter-carrier	E0	1	0	1	1	1	Х
	E1	0	1	1	1	1	Х
Video IF	E2	0	0	0	0	0	Х

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Description	Bits	TV sy	/stem	Force audio mute			
		B/G	I	D/K	L	Ľ'	
	E3	1	1	1	1	0	Х
	E4	0	0	0	0	1	Х
IF gain	E5	0	0	0	0	0	Х
L/L' PLL gating	E6	1	1	1	1	1	Х
VIF AGC output	E7	0	0	0	0	0	0

11.4.2 I²C bus control – format to read mode

Table 29. Slave tra	Insmits data	a									
S Slave	address	R/W = 1	А	DATA	AN	Р					
Description of Bits											
Bit	Fun	Function									
S	Star	t condition									
Standard slave add	ess 100	0011X, whe	ere X is the va	lue of R/W							
R/W = 1	Rea	id mode									
А	Ack	Acknowledge, generated by slave									
DATA	Byte	e D, see <u>Tab</u>	<u>le 30</u>								
AN	Ack	nowledge no	ot, generated	by the maste	r ^[1]						
Р	Stop	o condition,	generated by	the master ^[1]							

[1] The master generates an acknowledge, when it has received the data word "READ". The master next generates an acknowledge, then slave begins transmitting the data word "READ", and so on until the master generates no acknowledge and transmits a STOP condition

Table 30. Byte D

Transmitted byte after read condition – status register

Function	MSB							LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Read	AFCWIN	VIFL	FMIFL	AFC4	AFC3	AFC2	AFC1	PONR

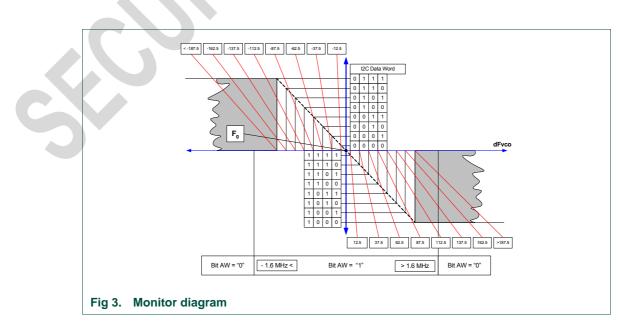
- PONR = 1, after power-on reset or after supply breakdown
- PONR = 0, after a successful reading of the status register
- FMIFL = Not used
- VIFL = 1, video IF level HIGH
- VIFL = 0, video IF level LOW
- AFCWIN = 1, F_{VIF} inside AFC window (within +/1.6 MHz)^[1]
- AFCWIN = 0, F_{VIF} outside AFC window (everywhere else)
- [1] Due to the Nyquist slope and the adjacent sound trap in the video SAW filter, the useable AFC window is typically from 500 kHz to + 1.6 MHz

Table 31. AFC status

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Function	Bits			
F _{VIF} vs F ₀ ^[1]	D4	D3	D2	D1
$F_{VIF} \leq F_0 - 187.5 \text{ kHz}$	0	1	1	1
$F_{VIF} = F_0 - 162.5 \text{ kHz}$	0	1	1	0
$F_{VIF} = F_0 - 137.5 \text{ kHz}$	0	1	0	1
$F_{VIF} = F_0 - 112.5 \text{ kHz}$	0	1	0	0
$F_{VIF} = F_0 - 87.5 \text{ kHz}$	0	0	1	1
$F_{VIF} = F_0 - 62.5 \text{ kHz}$	0	0	1	0
$F_{VIF} = F_0 - 37.5 \text{ kHz}$	0	0	0	1
$F_{VIF} = F_0 - 12.5 \text{ kHz}$	0	0	0	0
$F_{VIF} = F_0 + 12.5 \text{ kHz}$	1	1	1	1
$F_{VIF} = F_0 + 37.5 \text{ kHz}$	1	1	1	0
$F_{VIF} = F_0 + 62.5 \text{ kHz}$	1	1	0	1
$F_{VIF} = F_0 + 87.5 \text{ kHz}$	1	1	0	0
$F_{VIF} = F_0 + 112.5 \text{ kHz}$	1	0	1	1
$F_{VIF} = F_0 + 137.5 \text{ kHz}$	1	0	1	0
$F_{VIF} = F_0 + 162.5 \text{ kHz}$	1	0	0	1
$F_{VIF} \ge F_0 + 187.5 \text{ kHz}$	1	0	0	0



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11.4.3 Programming examples

11.4.3.1 Example 1: to tune to Ch E21 (471.25 MHz) in high band

- F_{osc} = 471.25 MHz + 38.9 MHz = 510.15 MHz
 - N = (510.15 MHz) / (62.5 kHz) = 1F E2 (Hexadecimal)
 - So DB1 = 1F H
 - and DB2 = E2 H
 - CB = 8E
 - BB = 44 H (because of high band selected)

11.4.3.2 Example 2: to tune to a PAL B/G program at 471.25 MHz

<u>R</u> Tu Addr	MSI	r <i>IIC</i> B BitG				Bit2	Bit1	LSB	-			HF IIC Data Bytes MSB Bit6 Bit5 Bit4 Bit3 Bit2 Bit1LSB Address
ADB	1	1	Û	đ	Û	<u>MA1</u>	MAO	<u>R/W</u>	=	C2		Slave $1 0 M1 0 1 M2 RMV = 86$
Write	,											Sub (SAD) 0 0 0 0 0 SAD1 SAD0 = 00
DB1	0	<u>N14</u>	<u>N13</u>	N12	N11	N10	N9	N8	=	1F		Write
DB2	N7	N6	N5	<u>N4</u>	<u>N3</u>	<u>N2</u>	N1	<u>N0</u>	=	E2		Switching (B) L FMS FMA TVM FM CM AMF VM = 5
СВ	1	CP	<u>T2</u>	<u>11</u>	то	RSA	RSB	<u>WSB</u>	=	8E		Adjust (C) AG DE1 DE0 TOP4 TOP3 TOP2 TOP1 TOP0 = 7
BB	X	X	X	<u>ADC</u>	<u>P3</u>	High	Mid	Low	=	44		Data (E) AGC Gate GIE VIE2 VIF1 VIE0 SIF1 SIF0 = 4
												Read
Read	1											Status (SR) AFCW VIEL FMIFL AFC4 AFC3 AFC2 AFC1 POR = 0
SB	POR	EL	1	1	1	<u>A2</u>	<u>A1</u>	<u>AŪ</u>	=	00	ľ	Close
					Clos	se)						
										,	-	
Fig 4	I	PAL	B/G	pro	gra	m						

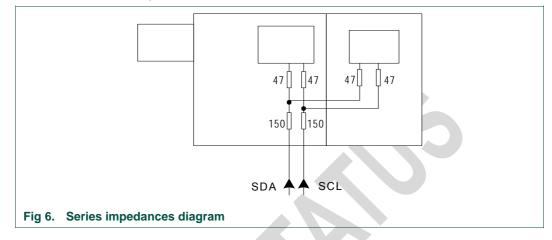
11.4.3.3 Example 3: to tune to SECAM program at 471.25 MHz (L system)

The settings are only for reference. Please refer to the demonstration software

5	Tuner IIC Data Bytes Image: Second state state MSB Bin6 Bin5 Bin4 Bin3 Bin2 Bin1 LSB Address ADB 7 7 0 0 MA1 MA0 RAW = C2 Write DB1 0 N14 N12 N11 N10 N8 = 1F DB2 N7 N6 N5 N4 N2 N1 N0 = E2 CB CP T2 T1 TO RSA RSB WSB = 8E BB X X ADC P3 High Mint Low = 44	IF I/C Data Bytes MSB Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 LSB Address I I I I I M2 RMW = 86 Sub (SAD) I I I I I I M2 RMW = 86 Sub (SAD) I I I I I M2 RMW = 86 Sub (SAD) I I I I I III III IIII IIII IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII
	Read SB POR 1 A2 A1 A0 = 00 Close	Read Status (SR) AFCW VIFL FMIFL AFC3 AFC2 AFC1 POR Close

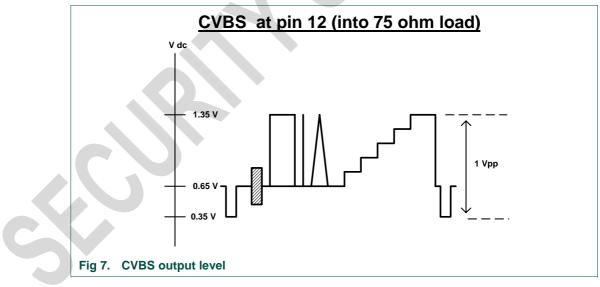
11.5 Loading of I²C-BUS

The FQ1216ME MK5 contains series impedances in the SCL and SDA as shown in the diagram below. Both lines also have capacitive loads of C = 39 pF max. Care must be taken to ensure that the total load on the bus does not exceed that as mentioned in the brochure "The I^2 C-Bus specifications".

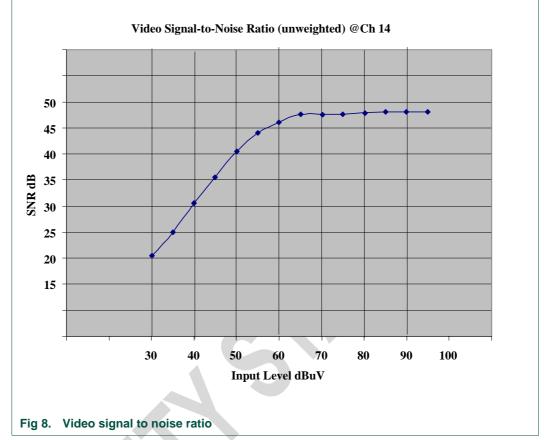


11.6 CVBS load and tuning voltage supply

A video buffer is built into the frontend to enable the unit to drive a 75 Ω load directly (e.g. into the SAA711x directly). A DC-DC converter for providing the required tuning voltage supply is already built into the FQ1216ME MK5



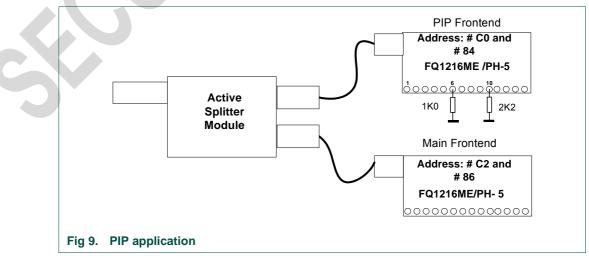
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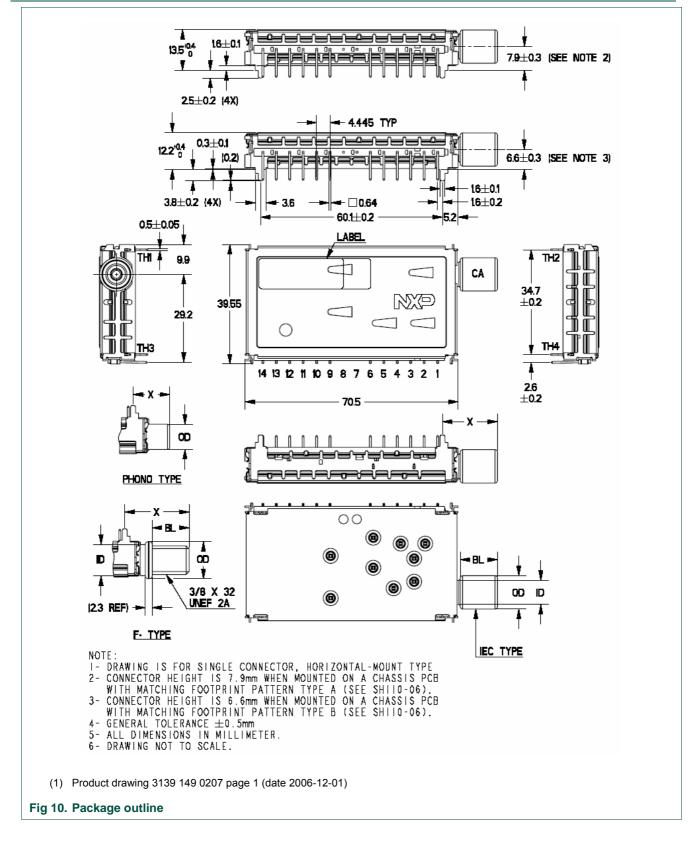
11.7 Video signal to noise ratio (B/G system)

11.8 PIP application

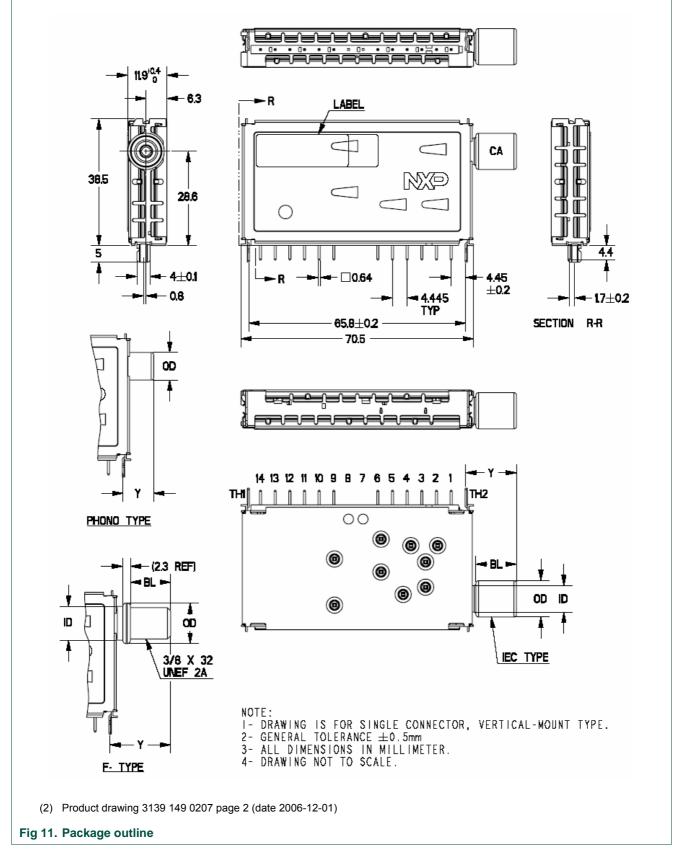
The FQ1216ME has a second user-defined address for the IF circuit. By setting a 2K2 resistor at pin 10, the AFRIC address is set to # 84. In the same manner, with a 1K resistor to ground at pin 6, the tuner is set to an address of # C0. The other FQ1216ME Mk3 remains unchanged with an address of # C2 and # 86 respectively. An example is shown below.



12. Package outline



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L - F - G -	CA CB CA CB	IEC FEMALE IEC MALE IEC FEMALE	18.2±0.5	15.35±0.5	12.2±0.3	Ø11.0±0.1	Ø 8.0±0.2
F G	СВ	IEC FEMALE				Ø 9.53±0.05	l í
F G			24.6±0.5	21.75±0.5	12.2±0.3	Ø11.2±0.1	Ø9.0±0.3
G -		•	-	-	-	-	-
G	CA CB	F- TYPE	213±0.5	18.45±0.5	12.2±0.3	Ø12.3+07-0.3	Ø 9.8 ±0.2
	CA CB	F. TYPE	25.6±0.5	22.75 ±0.5	16.5±0.3	Ø12.3+0/-0.3	Ø9.8±0.2
	CA CB	F- TYPE	29.0±0.5	26.15±0.5	19. 9± 0.3	Ø12.3+0/-0.3	Ø9.8±0.2
	CA CB	PHONO	12.1±0.5	9.25±0.5	-	Ø 8.35+0/-0. 1	-
			12 #				D
			F	PLUG			IEC PL
			(Ø7.9 REF Ø3.17	=} <u>+</u> -±0.03 +			
			PHONO	PLUG			
		For dimension to IEC 60010	ns which are na 69-24 (for F p	ot reflected in olug) and IEC 6	the drawing, r 00169-2 (for le	efer :C plugi.	

FQ1216ME_MK5

13. Packing information

The products are packed in the carton box and transferred to customers by Pallet Transport.

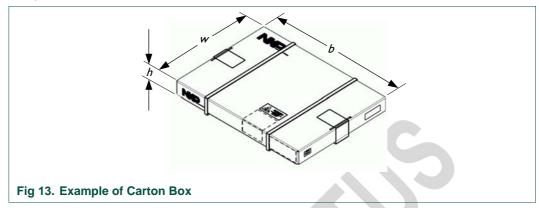


Table 32. Package information

Carton boxes are made of corrugated fibreboard which is free of environmentally banned substances

Mounting type	Package	Dimension L x W x H (cm)	Number of sets	Gross weight (kg)
Horizontal	Carton	46 x 34 x 5.4	40	2.34
	Pallet	120 x 105 x 105	4280	272.38
Vertical	Carton	46 x 34 x 10.2	120	6.38
	Pallet	120 x 105 x 105	6960	392.04

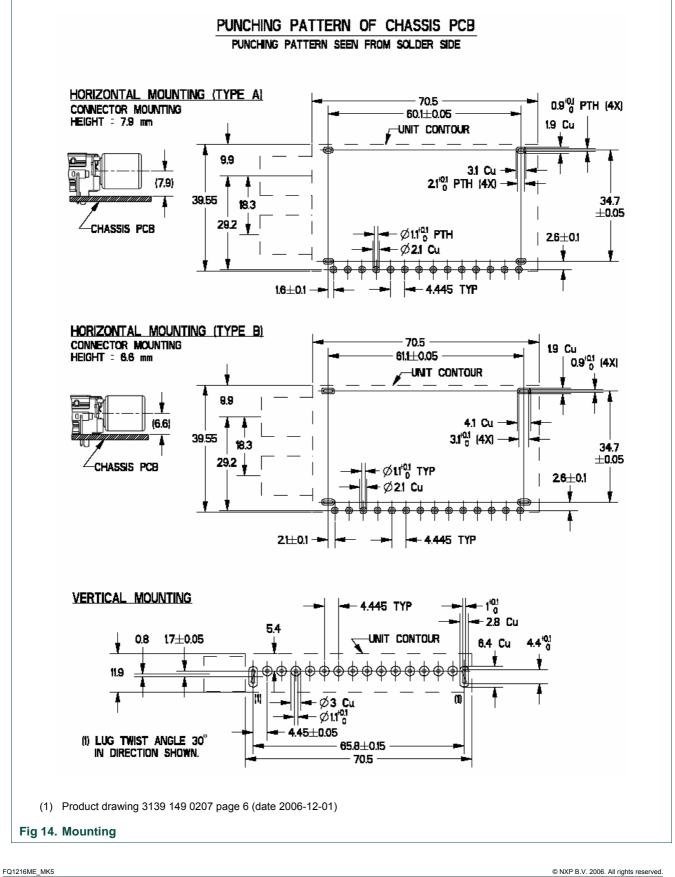
14. Mounting

14.1 Punching pattern of chassis PCB

For optimum mounting of the tuner to a PCB, the punching pattern is recommended

The tuner must be mounted without clearance between the tuner supporting surface and the printed circuit board (PCB). When mounted in this way, the tuner must be soldered to the PCB. This can be achieved by pressing the unit vertically onto the PCB during soldering

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14.2 Aerial connection

Standard connector in accordance with type order information found on <u>Table 3</u> and drawings found on <u>Fig 12</u>.

14.3 Solderability

The solderability of pins and mounting tags when tested initially and after 16 hour steam ageing in accordance with "IEC 60068-2-20", test TA, method 1 (solder bath 235 °C for 2 s), results in a wetted area of 95 %. No de-wetting will occur when soldered at 260 °C for 5 s.

14.4 Resistance to soldering heat

The product will not be damaged when tested in accordance with "IEC 60068-2-20", test Tb, method 1A (solder bath 260 °C for $10 \pm 1 s$)

14.5 Mass

Approximately : 45 g

14.6 Robustness of pins

The pins will not be damaged when tested in accordance with "IEC 60068-2-21"

- Test Ua1, tensile of 10 N in axial direction
- Test Ua2, thrust of 4 N in axial direction

Product data sheet

15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
FQ1216ME_MK5	30-04-2004	Preliminary data sheet	Rev.a	-	
Modifications	Draft				
FQ1216ME_MK5	07-06-2004	Preliminary data sheet	Rev.b	30-04-2004	
Modifications	Updating of applicUpdated mechaniUpdated product of	5			
FQ1216ME_MK5	13-07-2004	Preliminary data sheet	Rev.c	07-06-2004	
Modifications	 Pg 16 – Updated Pg 17 - Update ta 	26 : AGC TOP adjustment IF TOP setting for B/G = +2 dB and ble 28 : consolidated programming ated mechanical drawings			
FQ1216ME_MK5	02-08-2004	Preliminary data sheet	Rev.d	13-07-2004	
Modifications	• Pg 24 to 28 - Upd	ated mechanical drawings			
FQ1216ME_MK5	10-11-2004	Product data sheet	Rev.e	02-08-2004	
Modifications	• Pg 2 – add new ty	pe FQ1216ME/L H-5 in ordering int	formation		
FQ1216ME_MK5	12-01-2005	Product data sheet	Rev.f	10-11-2004	
Modifications	• Pg 15 - Add table	27 : AGC TOP settings recommend	ded		
FQ1216ME_MK5	11-03-2005	Product data sheet	Rev.g	12-01-2005	
Modifications	Pg 24 to 28 - Updated mechanical drawings				
FQ1216ME_MK5	02-11-2005	Product data sheet	Rev.h	11-03-2005	
Modifications	Pg 21 - Updated I	² C bus loading diagram			
FQ1216ME_MK5	28-02-2006	Product data sheet	Rev.i	02-11-2005	
Modifications	• Pg 1 – correction	of error			
FQ1216ME_MK5	18-09-2006	Product data sheet	Rev.j	28-02-2006	
Modifications	 Pg 1 & 2 – Add IEC 60950-1 (2nd edition) Pg 18 – Add a table note for table 31 : AFC window Update product code as SV23 introduce in WK 0643 				
FQ1216ME_MK5	14-06-2007	Product data sheet	Rev.k	18-09-2006	
Modifications	Update from Philip	os to NXP			

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <u>http://www.nxp.com</u>.

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