

ON Semiconductor®

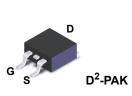
FQB10N50CF N-Channel QFET[®] FRFET[®] MOSFET 500 V, 10 A, 610 m Ω

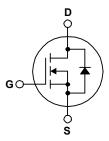
Features

- + 10 A, 500 V, $R_{DS(on)}$ = 610 m Ω (Max.) @ V_{GS} = 10 V, I_D = 5 A
- Low gate charge (Typ. 45 nC)
- Low Crss (Typ. 17.5 pF)
- 100% avalanche tested
- · Fast recovery body diode

Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.





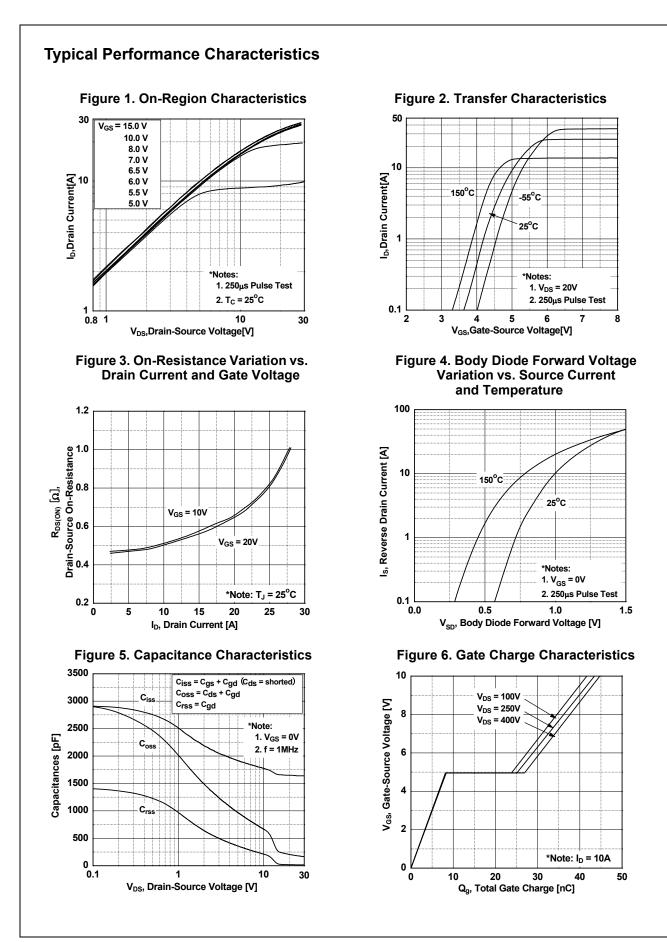
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

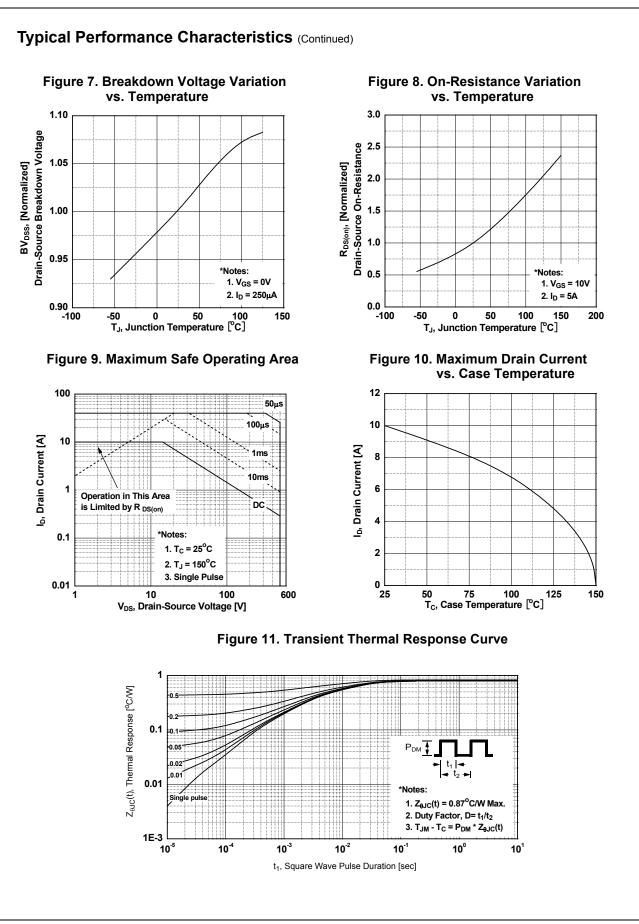
Symbol		FQB10N50CFTM-WS	Unit			
V _{DSS}	Drain to Source Voltage	500	V			
V _{GSS}	Gate to Source Voltage			±30	V	
ID	Drain Current	- Continuous ($T_C = 25^{\circ}C$)	- Continuous ($T_C = 25^{\circ}C$)		Α	
	Dramount	- Continuous ($T_C = 100^{\circ}C$)		6.35		
I _{DM}	Drain Current	- Pulsed	(Note 1)	40	A	
E _{AS}	Single Pulsed Avalanche E	nergy	(Note 2)	825	mJ	
I _{AR}	Avalanche Current		(Note 1)	10	А	
E _{AR}	Repetitive Avalanche Ener	ду	(Note 1)	14.3	mJ	
dv/dt	Peak Diode Recovery dv/d	t	(Note 3)	2.0	V/ns	
P _D	Dower Dissinction	(T _C = 25°C)		143	W	
	Power Dissipation	- Derate above 25°C		1.14	W/ºC	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	°C	
ΤL	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C	

Thermal Characteristics

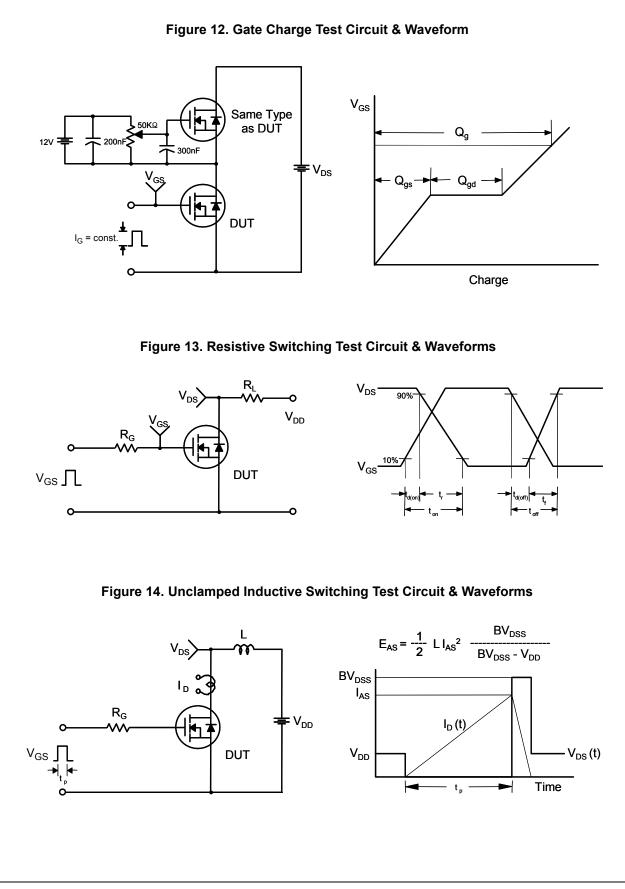
Symbol	Parameter	FQB10N50CFTM-WS	Unit	
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case, Max	0.87		
$R_{ hetaJA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	°C/W	
	Thermal Resistance, Junction to Ambient (1 in ² pad of 2 oz copper), Max.	40		

-		Device	Package	age Reel Size T		dth	Quantity	
		D2-PAK			24mm		800	
Electrica	l Cha	racteristics						
Symbol		Parameter		Test Conditions	Min.	Тур.	Max.	Unit
Off Charao	teristi	cs.	4					1
BV _{DSS}	Drain to Source Breakdown Voltage		e l_ = 2	I _D = 250μA, V _{GS} = 0V, T _J = 25 ^o C		_	-	V
ΔBV _{DSS}	Breakdown Voltage Temperature			$I_D = 250 \mu A$, $V_{GS} = 0V$, $I_J = 25^{\circ}C$ $I_D = 250 \mu A$, Referenced to $25^{\circ}C$			_	-
$/\Delta T_{J}$		Coefficient				0.5	-	V/°C
i	Zoro	Zero Gate Voltage Drain Current		$V_{DS} = 500V$, $V_{GS} = 0V$ $V_{DS} = 400V$, $T_C = 125^{\circ}C$		-	10	μΑ
IDSS	2010 0					-	- 100	
I _{GSS}	Gate to Body Leakage Current			±30V, V _{DS} = 0V	-	-	±100	nA
On Charac	teristi	cs						
V _{GS(th)}		Gate Threshold Voltage		V _{GS} = V _{DS} , I _D = 250μA		_	4.0	V
R _{DS(on)}		tatic Drain to Source On Resistance		$V_{GS} = V_{DS}, I_D = 250 \mu A$ $V_{GS} = 10V, I_D = 5A$		0.51	0.61	Ω
9FS	Forward Transconductance			$V_{\rm DS} = 20V, I_{\rm D} = 5A$		105	-	S
			03					
Dynamic C					I	1	1	1
C _{iss}	Input C	Capacitance	y' = 25y' y' = 0y'		-	1660	2210	pF
C _{oss}	Outpu	t Capacitance		V _{DS} = 25V, V _{GS} = 0V f = 1MHz		182	240	pF
C _{rss}	Revers	se Transfer Capacitance				17.5	26	pF
Q _{g(tot)}	Total C	Sate Charge at 10V			-	45	60	nC
Q _{gs}	Gate t	o Source Gate Charge		$V_{\rm DS}$ = 400V, I _D = 10A $V_{\rm GS}$ = 10V (Note 4)		8	-	nC
Q _{gd}	Gate t	o Drain "Miller" Charge	v _{GS} -			19	-	nC
Switching	Chara	cteristics	i		<u> </u>			
-		Dn Delay Time			-	25	60	ns
t _{d(on)} t _r		On Rise Time	V _{DD} =	$V_{DD} = 250V, I_D = 10A$ $R_G = 25\Omega$ (Note 4)		47	105	ns
t _{d(off)}		Off Delay Time				138	285	ns
t _f		Off Fall Time				55	120	ns
				(,	Note 4) -		120	ne
Drain-Sou	-	ode Characteristics					1	
I _S	Maxim	Maximum Continuous Drain to Source Diode Forward Current			-	-	10	A
I _{SM}		Maximum Pulsed Drain to Source Diode Forward Current			-	-	40	A
V _{SD}		o Source Diode Forward Vol		0V, I _{SD} = 10A	-	-	1.4	V
t _{rr}		e Recovery Time		V _{GS} = 0V, I _{SD} = 10A dI _F /dt = 100A/μs		91	-	ns
Q _{rr}	Revers	e Recovery Charge	∣dl _F /dt			220	-	nC





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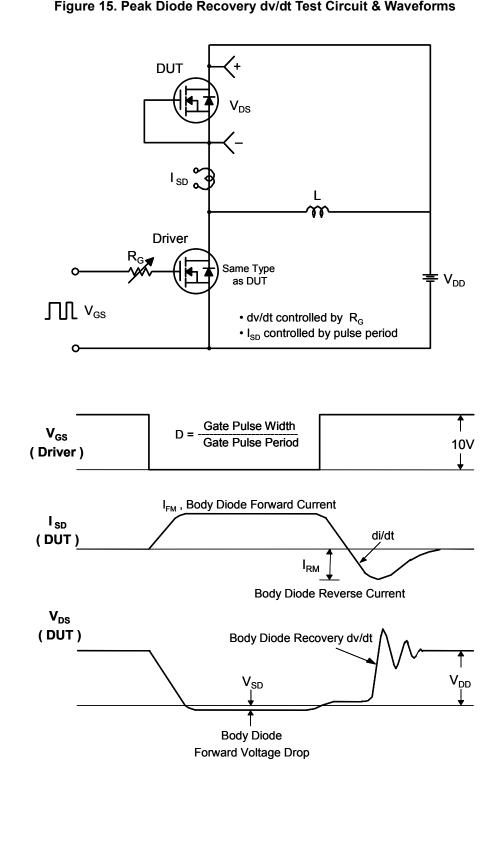
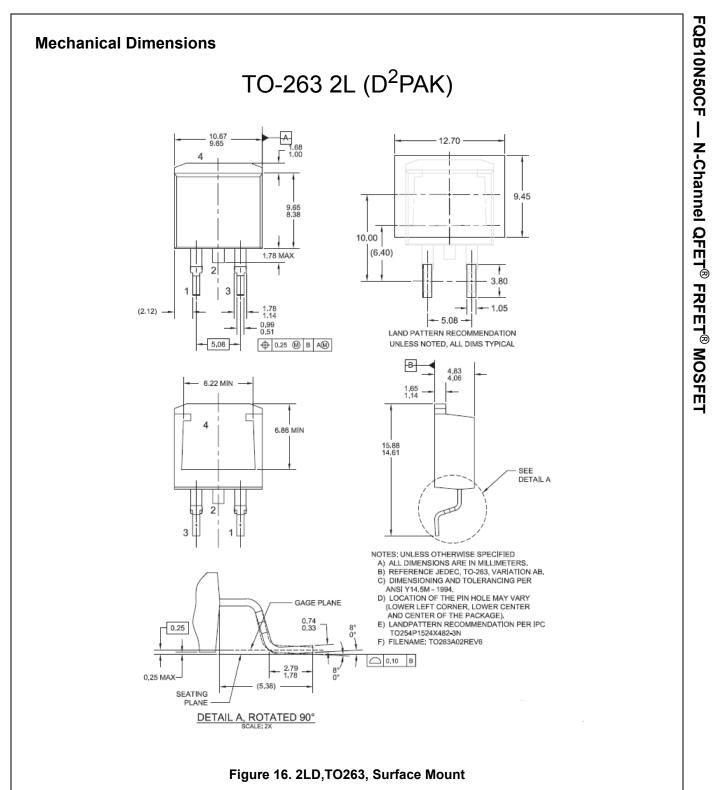


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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Dimension in Millimeters

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