

FQB34P10TM_F085

100V P-Channel MOSFET

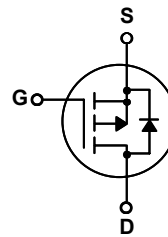
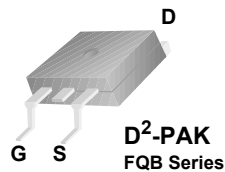
General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Features

- -33.5A, -100V, $R_{DS(on)} = 0.06\Omega @ V_{GS} = -10V$
- Low gate charge (typical 85 nC)
- Low Crss (typical 170 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating
- Qualified to AEC Q101
- RoHS Compliant



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FQB34P10TM_F085	Units
V _{DSS}	Drain-Source Voltage	-100	V
I _D	Drain Current - Continuous (T _C = 25°C)	-33.5	A
	- Continuous (T _C = 100°C)	-23.5	A
I _{DM}	Drain Current - Pulsed (Note 1)	-134	A
V _{GSS}	Gate-Source Voltage	± 25	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	2200	mJ
I _{AR}	Avalanche Current (Note 1)	-33.5	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	15.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-6.0	V/ns
P _D	Power Dissipation (T _A = 25°C) *	3.75	W
	Power Dissipation (T _C = 25°C)	155	W
	- Derate above 25°C	1.03	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	--	0.97	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient *	--	40	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	--	-0.1	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	μA
		$V_{DS} = -80\text{ V}, T_C = 150^\circ\text{C}$	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -16.75\text{ A}$	--	0.049	0.06	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -16.75\text{ A}$ (Note 4)	--	23	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2240	2910	pF
C_{oss}	Output Capacitance		--	730	950	pF
C_{rss}	Reverse Transfer Capacitance		--	170	220	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -50\text{ V}, I_D = -33.5\text{ A},$ $R_G = 25\ \Omega$	--	25	60	ns	
t_r	Turn-On Rise Time		--	250	510	ns	
$t_{d(off)}$	Turn-Off Delay Time		--	160	330	ns	
t_f	Turn-Off Fall Time		(Note 4, 5)	--	210	430	ns
Q_g	Total Gate Charge		$V_{DS} = -80\text{ V}, I_D = -33.5\text{ A},$ $V_{GS} = -10\text{ V}$	--	85	110	nC
Q_{gs}	Gate-Source Charge	(Note 4, 5)	--	15	--	nC	
Q_{gd}	Gate-Drain Charge		--	45	--	nC	

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	-33.5	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-134	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -33.5\text{ A}$	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -33.5\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$	--	160	--	ns
Q_{rr}	Reverse Recovery Charge	(Note 4)	--	0.88	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 3.9\text{ mH}, I_{AS} = -33.5\text{ A}, V_{DD} = -25\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq -33.5\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

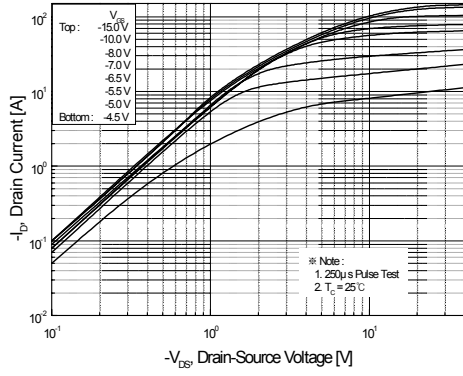


Figure 1. On-Region Characteristics

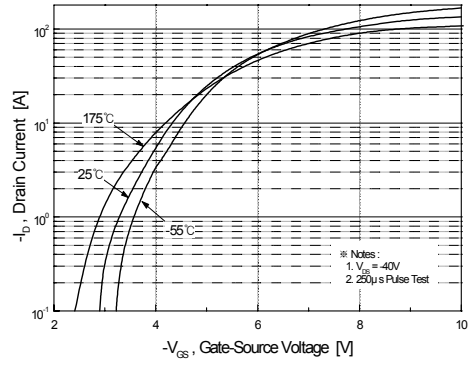


Figure 2. Transfer Characteristics

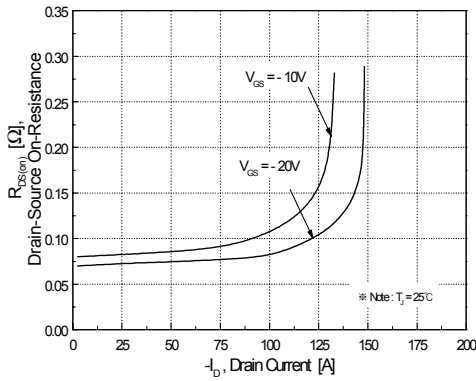


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

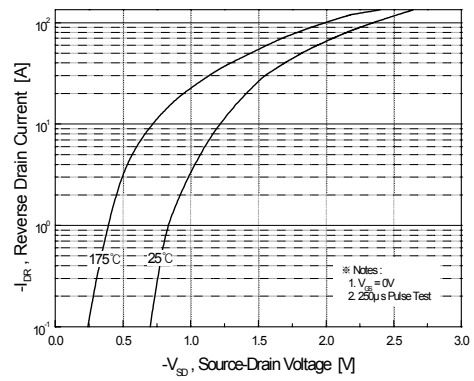


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

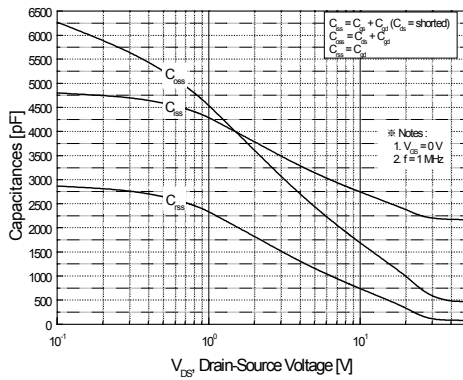


Figure 5. Capacitance Characteristics

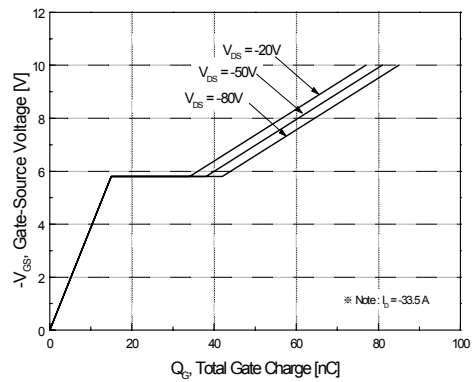


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

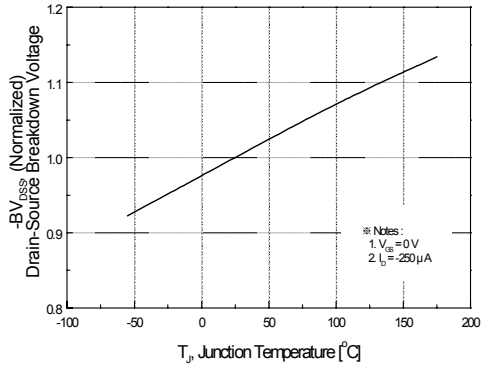


Figure 7. Breakdown Voltage Variation vs. Temperature

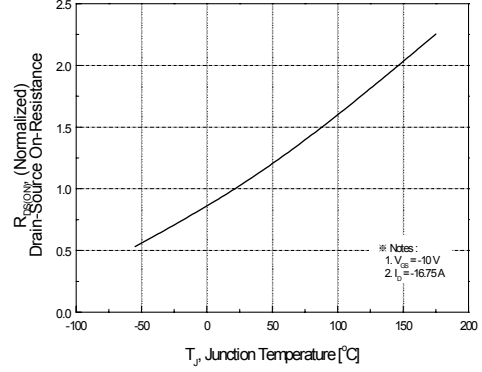


Figure 8. On-Resistance Variation vs. Temperature

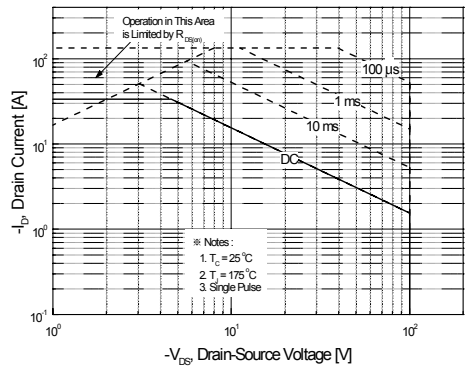


Figure 9. Maximum Safe Operating Area

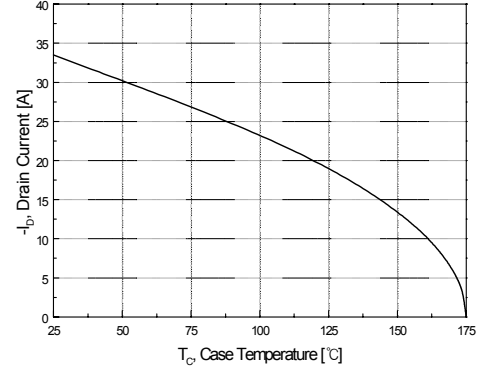


Figure 10. Maximum Drain Current vs. Case Temperature

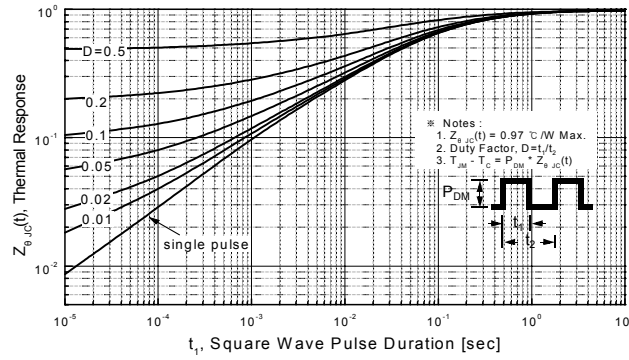
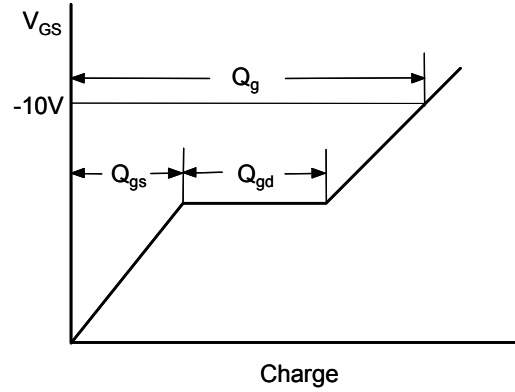
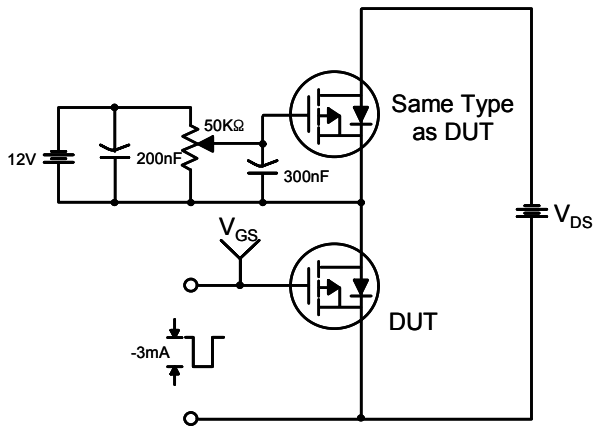
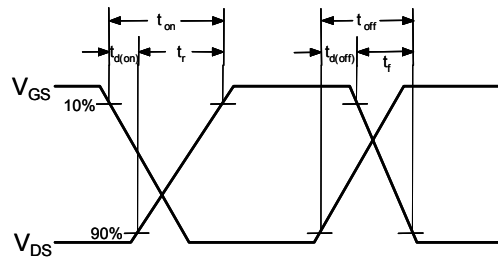
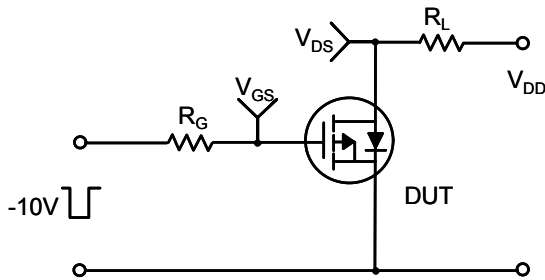


Figure 11. Transient Thermal Response Curve

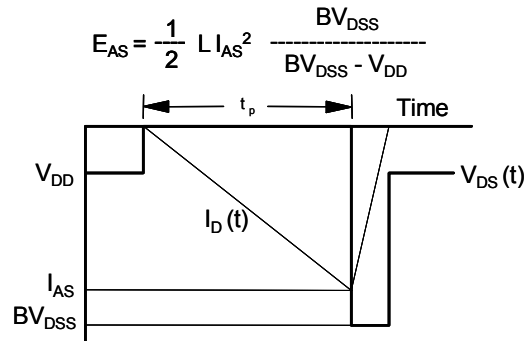
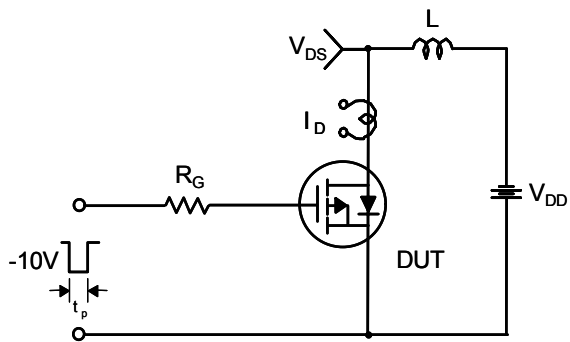
Gate Charge Test Circuit & Waveform



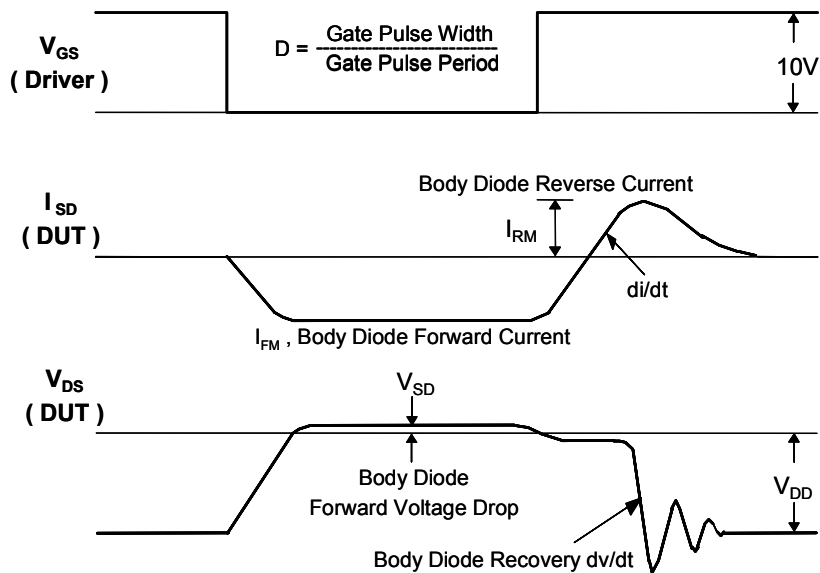
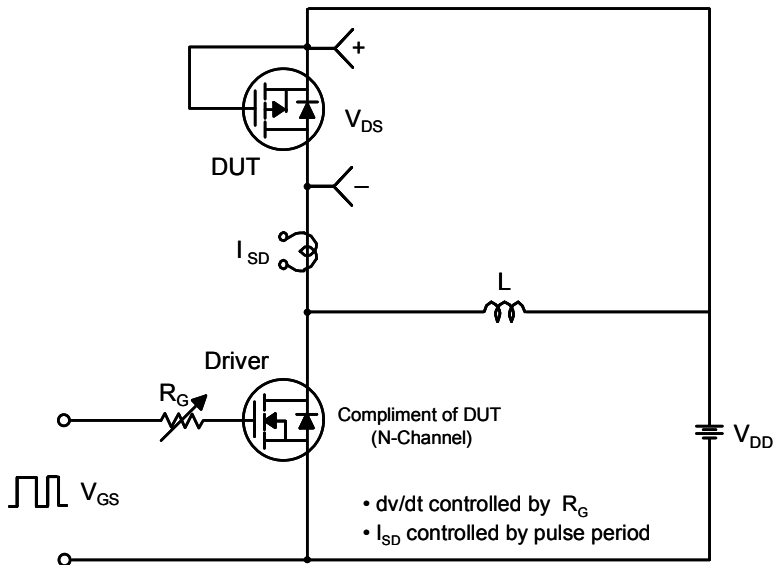
Resistive Switching Test Circuit & Waveforms

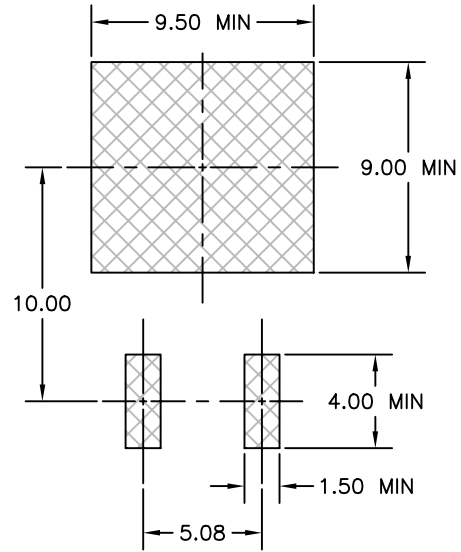
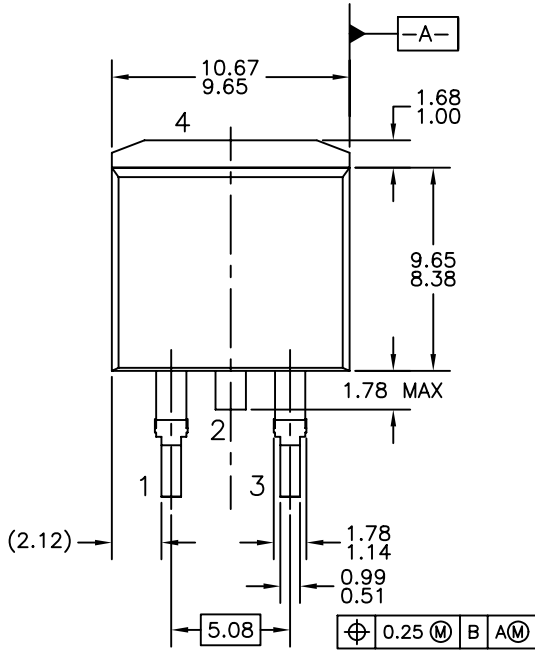


Unclamped Inductive Switching Test Circuit & Waveforms

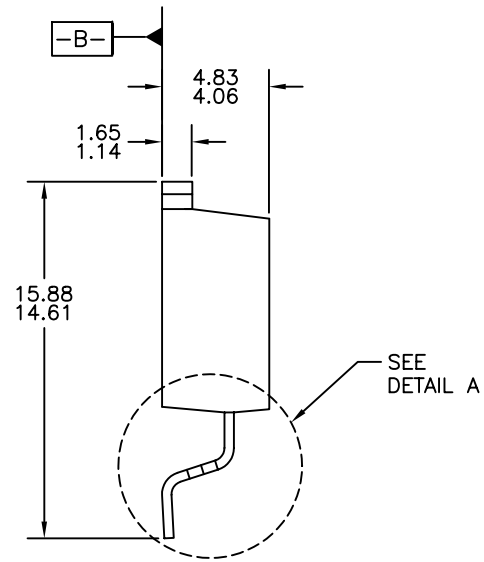
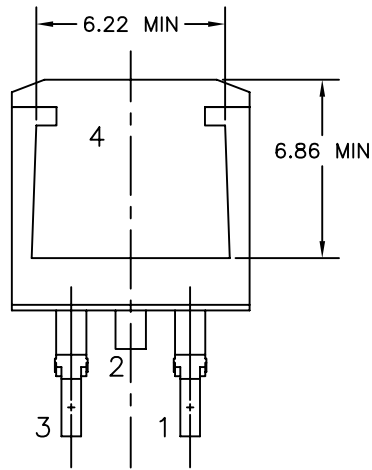


Peak Diode Recovery dv/dt Test Circuit & Waveforms



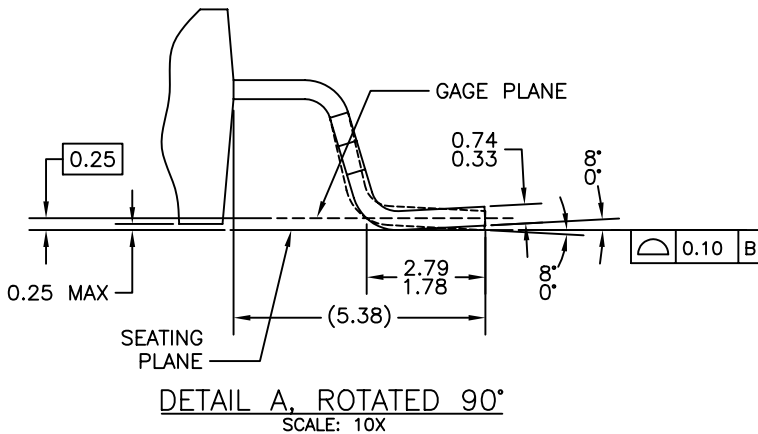


LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED






- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
- C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
- D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
- E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- F) FILENAME: T0263A02REV5





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