FAIRCHILD
SEMICONDUCTOR®

October 2008

**QFET®**

FQB7N65C
650V N-Channel MOSFET

Features

- 7A, 650V, $R_{DS(on)}$ = 1.4Ω @V_{GS} = 10 V
- Low gate charge (typical 28 nC)
- Low Crss (typical 12 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS Compliant

100% LEAD-FREE IMPLEMENTATION

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.

G S **D²-PAK**
FQB Series
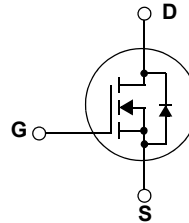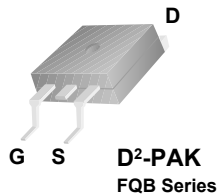
Absolute Maximum Ratings

Symbol	Parameter		FQB7N65C	Units
V_{DSS}	Drain-Source Voltage		650	V
I_D	Drain Current - Continuous (T_C = 25°C)		7	A
	- Continuous (T_C = 100°C)		4.45	A
I_{DM}	Drain Current - Pulsed	(Note 1)	28	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	212	mJ
I_{AR}	Avalanche Current	(Note 1)	7	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	17.3	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		173	W
	- Derate above 25°C		1.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQB7N65C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB7N65C	FQB7N65CTM	D2-PAK	330mm	24mm	800

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	650	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.8	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 520 V, T_C = 125°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A	--	1.2	1.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D =3.5 A (Note 4)	--	8	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	955	1245	pF
C_{oss}	Output Capacitance		--	100	130	pF
C_{rss}	Reverse Transfer Capacitance		--	12	16	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 325 V, I_D = 7A, R_G = 25 Ω	--	20	50	ns
t_r	Turn-On Rise Time		--	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time	(Note 4, 5)	--	90	190	ns
t_f	Turn-Off Fall Time		--	55	120	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 7A, V_{GS} = 10 V	--	28	36	nC
Q_{gs}	Gate-Source Charge		--	4.5	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	12	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	28	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 7 A, dI_F / dt = 100 A/µs	--	400	--	ns
Q_{rr}	Reverse Recovery Charge	(Note 4)	--	3.3	--	µC

NOTES:

1. Repetitive Rating : Pulse width limited by maximum junction temperature

2. L = 8mH, I_{AS} = 7A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C

3. I_{SD} ≤ 7A, di/dt ≤200A/µs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%

5. Essentially independent of operating temperature

Typical Performance Characteristics

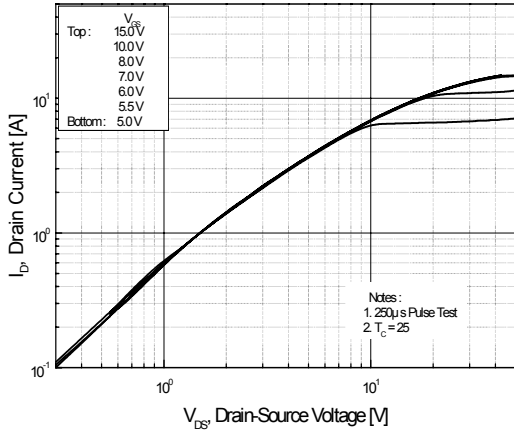### Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage
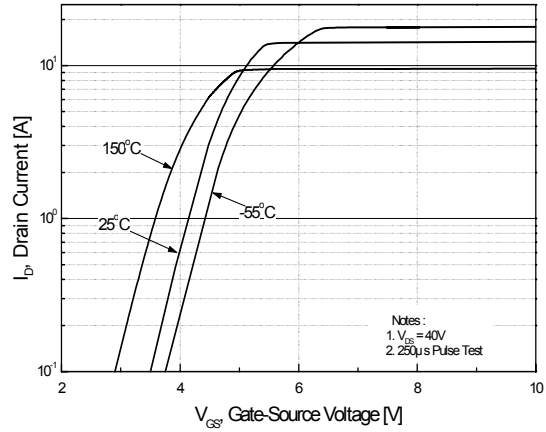
Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

Figure 5. Capacitance Characteristics
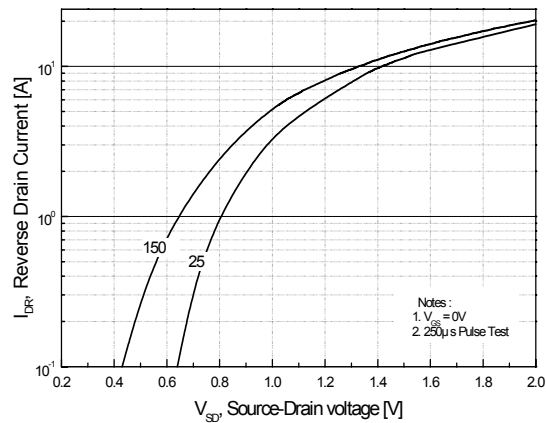
Figure 6. Gate Charge Characteristics
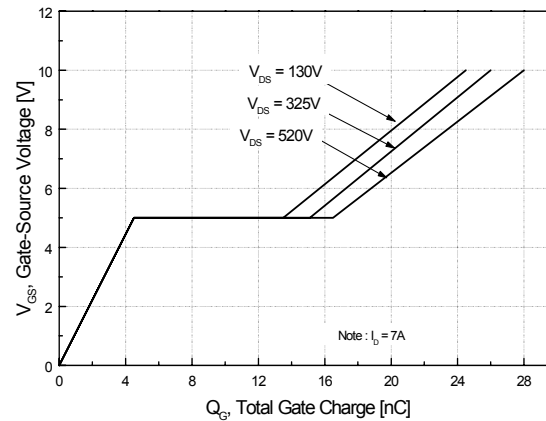
Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

Notes :
1. $V_{GS} = 0V$
2. $I_D = 250\,\mu A$
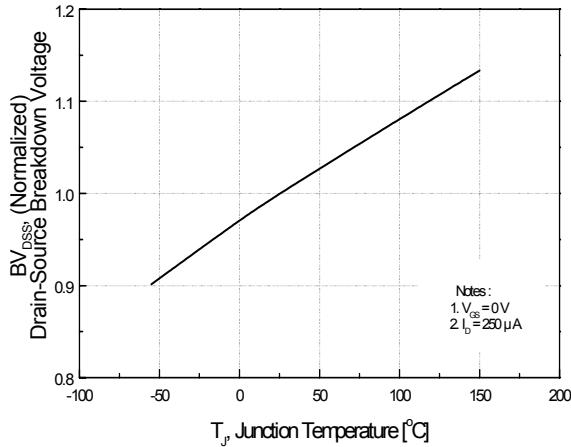
Figure 8. On-Resistance Variation vs. Temperature

Notes :
1. $V_{GS} = 10V$
2. $I_D = 3.5A$
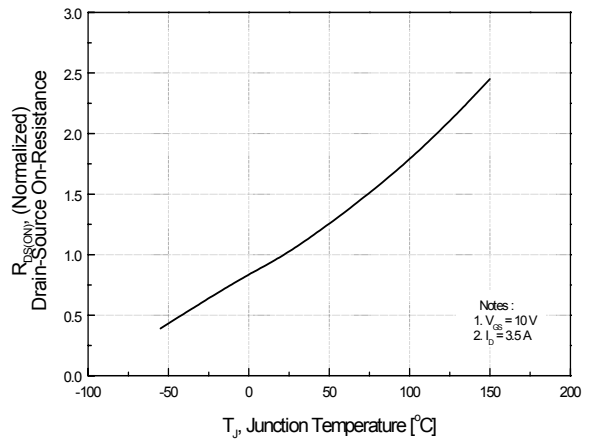
Figure 9. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

10 μs
100 μs
1ms
10ms
100ms
DC

* Notes :
1. $T_C = 25\,^{\circ}C$
2. $T_J = 150\,^{\circ}C$
3. Single Pulse
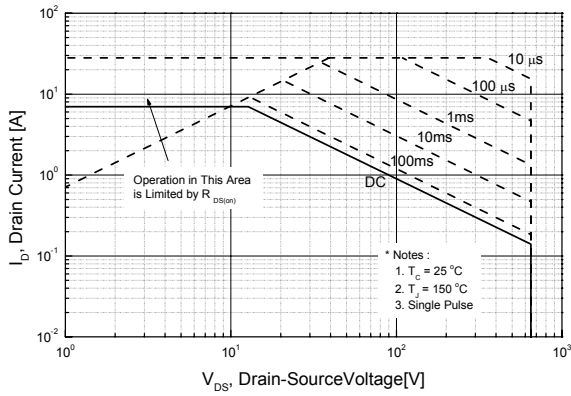
Figure 10. Maximum Drain Current vs. Case Temperature
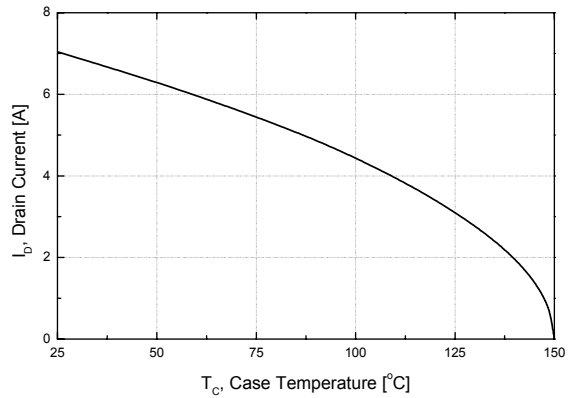
Figure 11. Transient Thermal Response Curve

D=0.5
0.2
0.1
0.05
0.02
0.01

single pulse

* Notes :
1. $Z_{thJC}(t) = 0.75\,^{\circ}C/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{thJC}(t)$
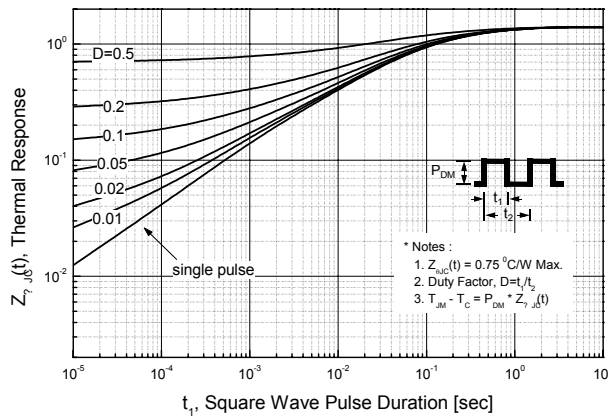
Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms
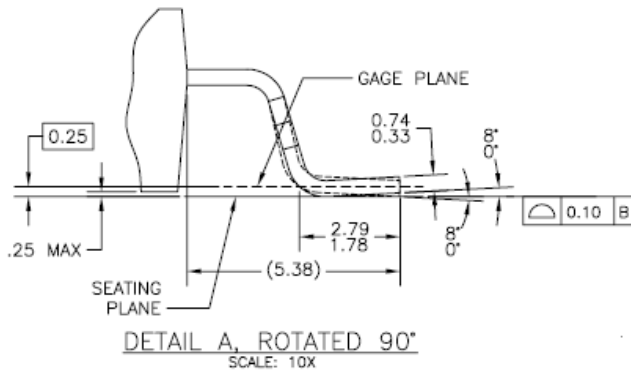

Unclamped Inductive Switching Test Circuit & Waveforms

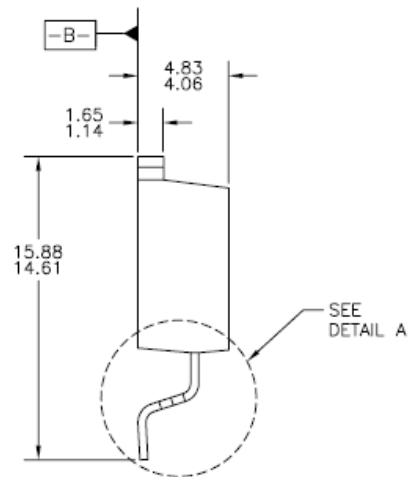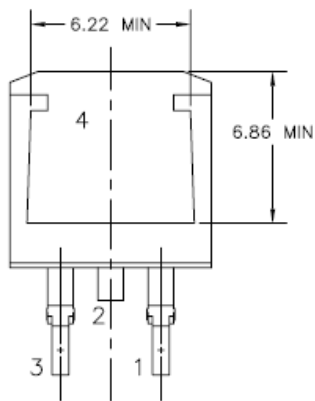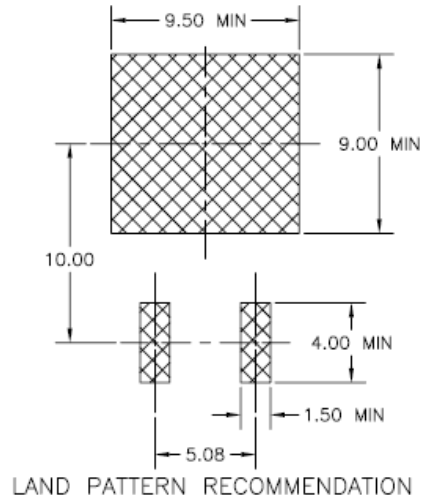$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

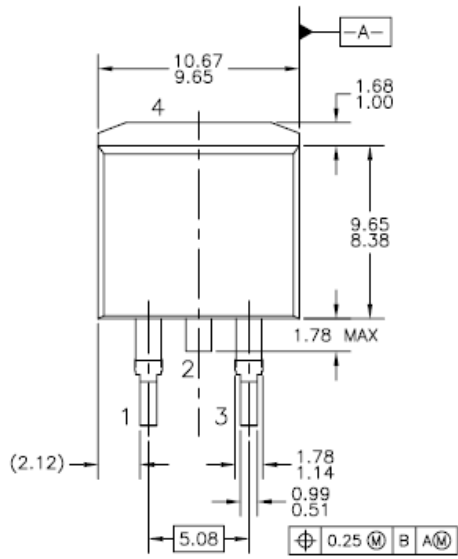**Peak Diode Recovery dv/dt Test Circuit & Waveforms**

Mechanical Dimensions

D² - PAK

LAND PATTERN RECOMMENDATION

DETAIL A, ROTATED 90°
SCALE: 10X

Dimensions in Millimeters

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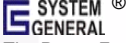
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Rev. I37