



FQD15N10

100V N-Channel MOSFET

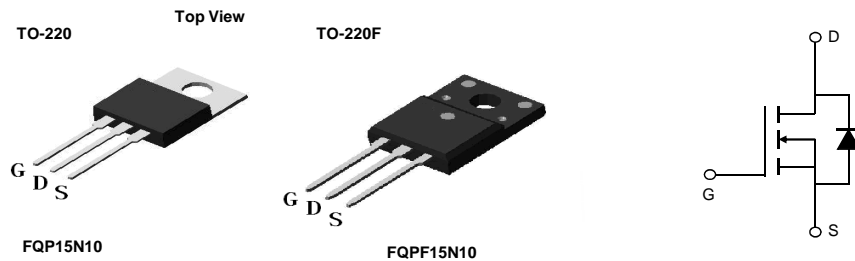
General Description

The FQP15N10 & FQPF15N10 uses trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$, C_{iss} and C_{oss} . This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	15A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	$< 80m\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	$< 75m\ \Omega$

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	FQP15N10	FQPF15N10	Units
Drain-Source Voltage	V_{DS}	100		V
Gate-Source Voltage	V_{GS}	± 20		V
Continuous Drain Current	I_D	$T_C=25^\circ C$	15	A
		$T_C=100^\circ C$	14	
Pulsed Drain Current ^C	I_{DM}	40		
Continuous Drain Current	I_{DSM}	$T_A=25^\circ C$	5	A
		$T_A=70^\circ C$	4	
Avalanche Current ^C	I_{AS}	8		A
Avalanche energy $L=0.1mH$ ^C	E_{AS}	3		mJ
Power Dissipation ^B	P_D	$T_C=25^\circ C$	31.5	W
		$T_C=100^\circ C$	18.5	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ C$	2.1	
		$T_A=70^\circ C$	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175		$^\circ C$

Thermal Characteristics

Parameter	Symbol	FQP15N10	FQPF15N10	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	10	$^\circ C/W$
Maximum Junction-to-Ambient ^{A, D}		Steady-State	40	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.2	5.4	$^\circ C/W$



Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	2	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	40			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =8A T _J =125°C		75 88	90 98	mΩ
		V _{GS} =4.5V, I _D =3A		65	73.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A		28		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz		870		pF
C _{oss}	Output Capacitance			68		pF
C _{riss}	Reverse Transfer Capacitance			3.5		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		7		Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =8A		12.5	20	nC
Q _{g(4.5V)}	Total Gate Charge			5.5	10	nC
Q _{gs}	Gate Source Charge			2.5		nC
Q _{gd}	Gate Drain Charge			2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =5Ω, R _{GEN} =3Ω		7.5		ns
t _r	Turn-On Rise Time			3.5		ns
t _{D(off)}	Turn-Off DelayTime			23		ns
t _f	Turn-Off Fall Time			5.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =10A, di/dt=500A/μs		20		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =10A, di/dt=500A/μs		88		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. The maximum current limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

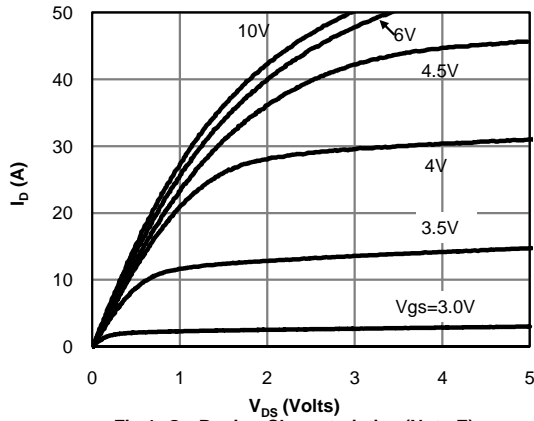


Fig 1: On-Region Characteristics (Note E)

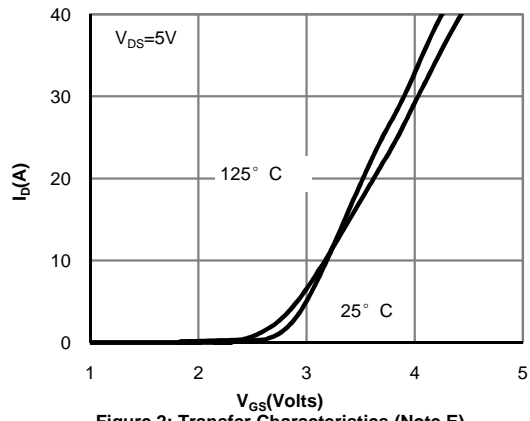


Figure 2: Transfer Characteristics (Note E)

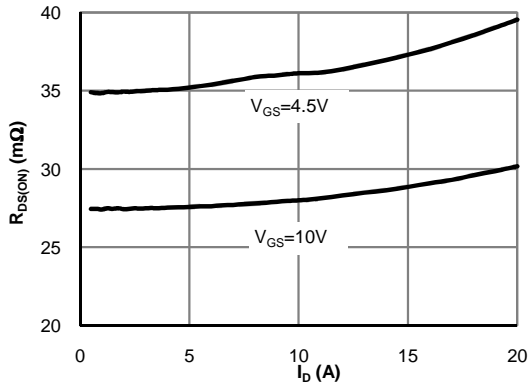


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

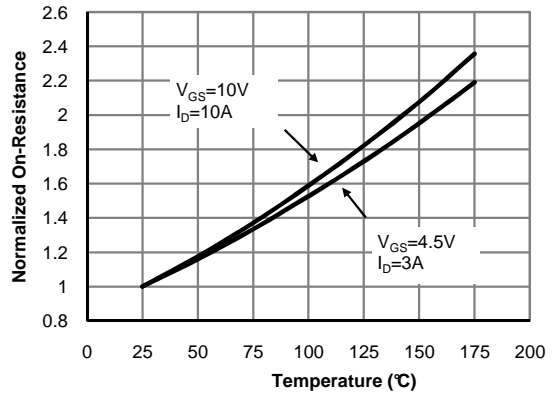


Figure 4: On-Resistance vs. Junction Temperature (Note E)

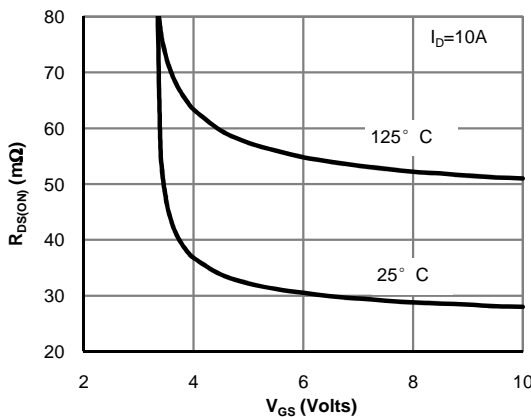


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

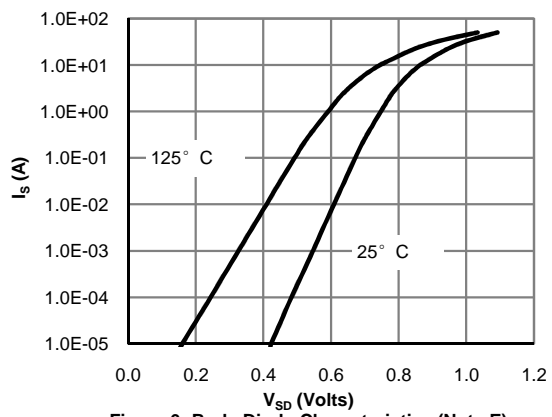


Figure 6: Body-Diode Characteristics (Note E)



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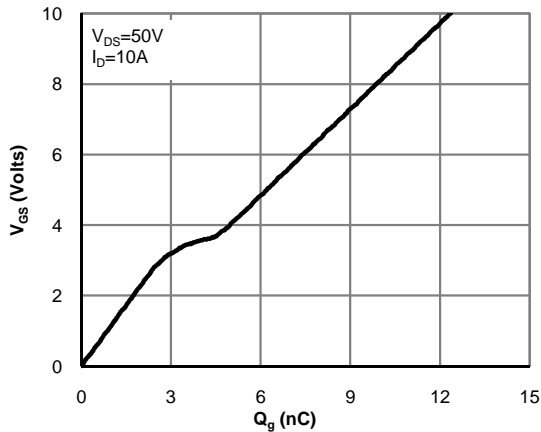


Figure 7: Gate-Charge Characteristics

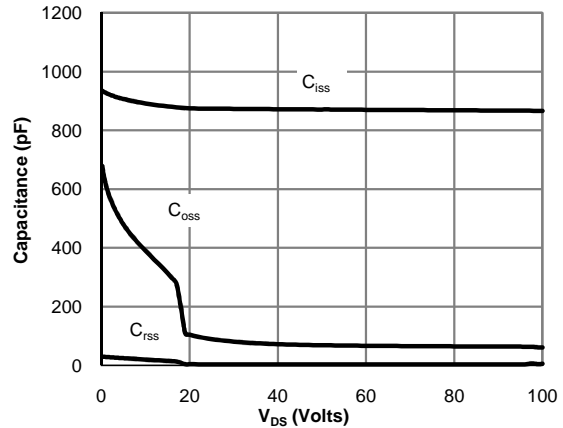


Figure 8: Capacitance Characteristics

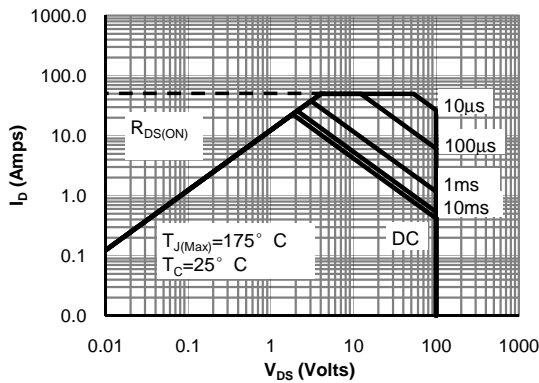


Figure 9: Maximum Forward Biased Safe Operating Area for AOT2916L (Note F)

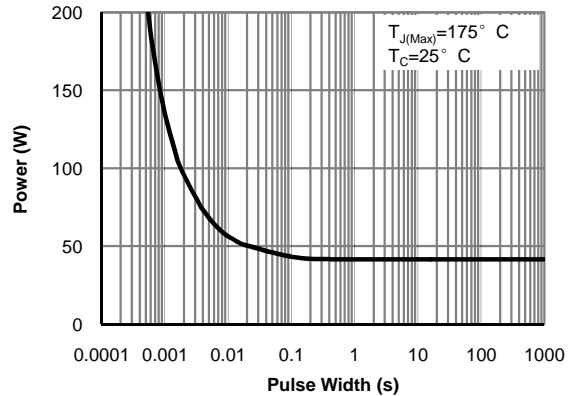


Figure 10: Single Pulse Power Rating Junction-to-Case for AOT2916L (Note F)

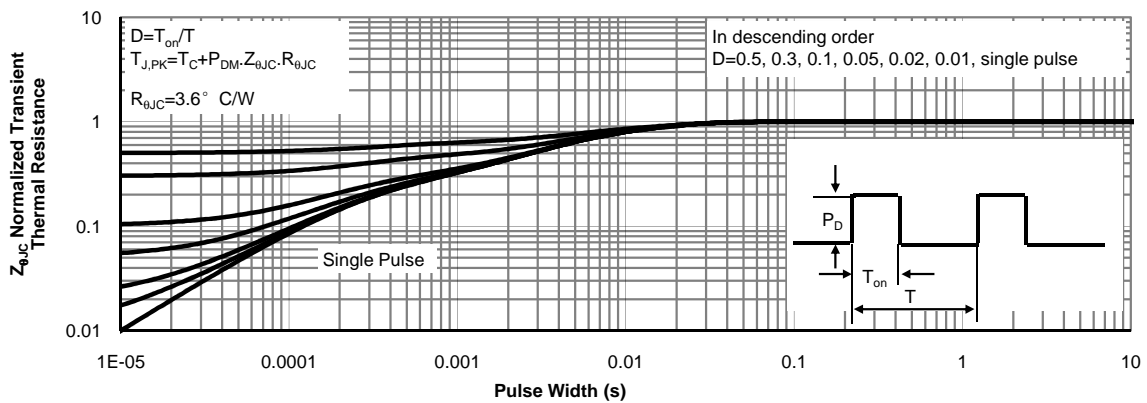


Figure 11: Normalized Maximum Transient Thermal Impedance for AOT2916L (Note F)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

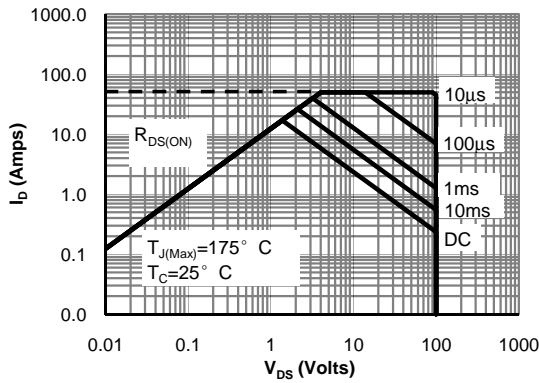


Figure 9: Maximum Forward Biased Safe Operating Area for AOTF2916L

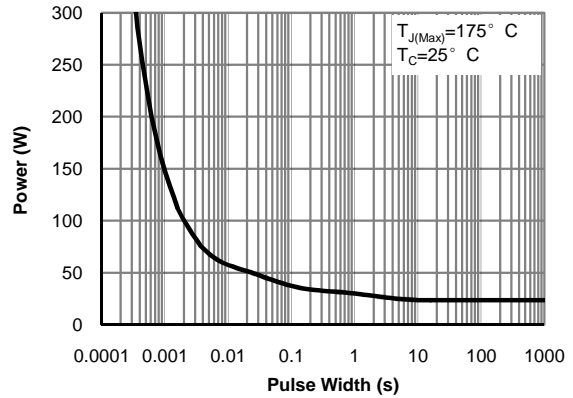


Figure 10: Single Pulse Power Rating Junction-to-Case for AOTF2916L (Note F)

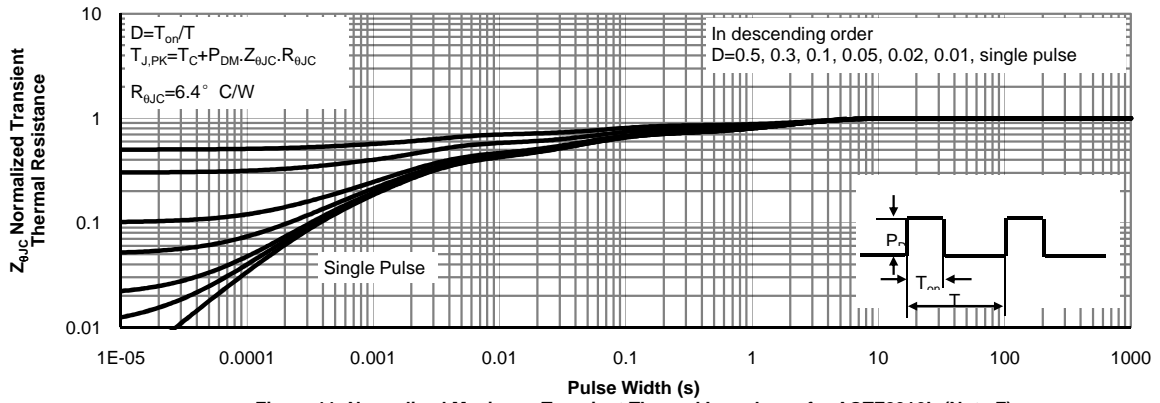


Figure 11: Normalized Maximum Transient Thermal Impedance for AOTF2916L (Note F)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

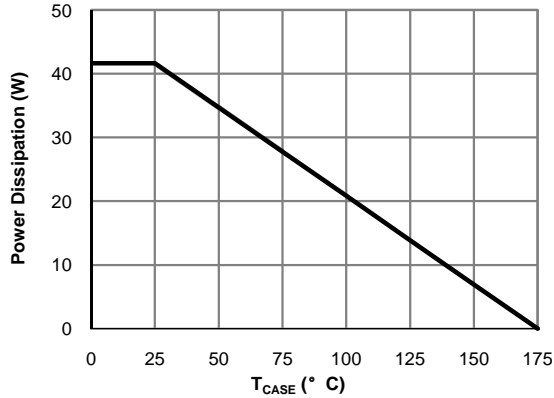


Figure 12: Power De-rating (Note F)

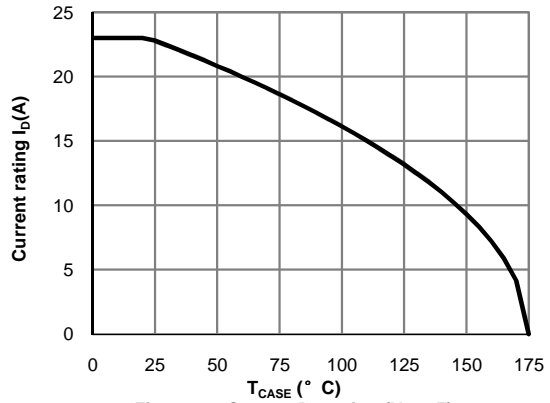


Figure 13: Current De-rating (Note F)

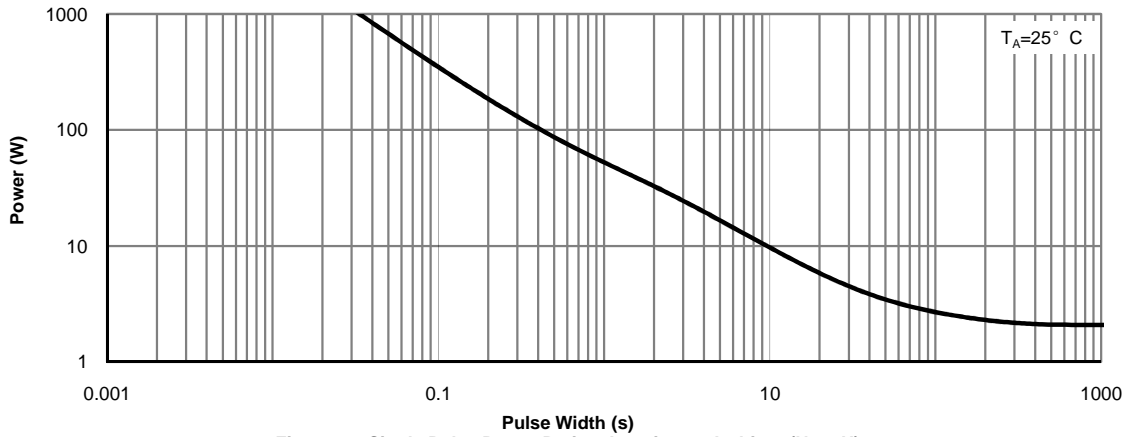


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

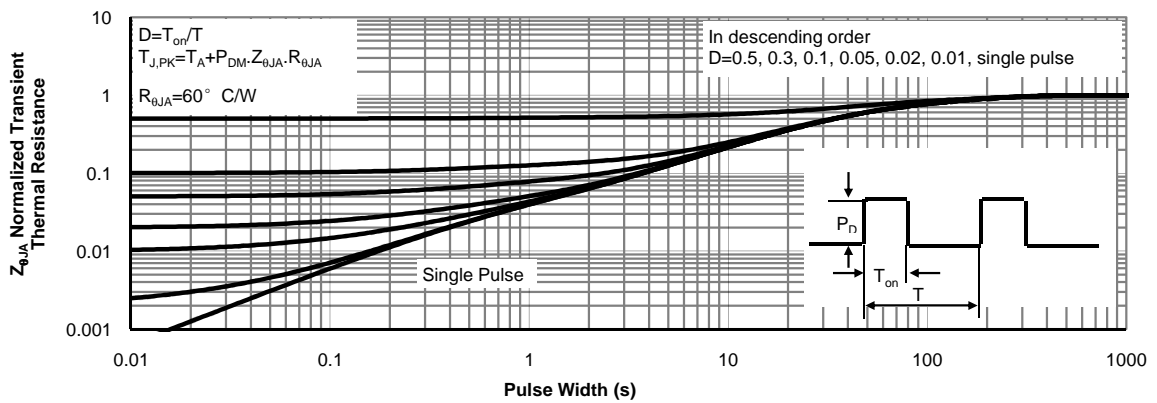
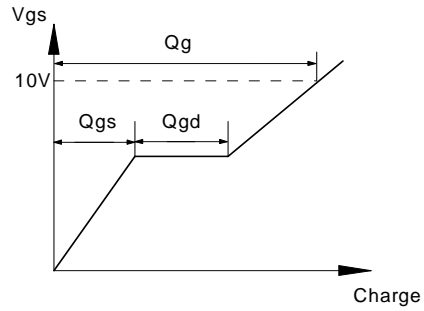
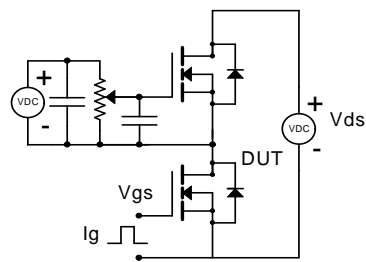
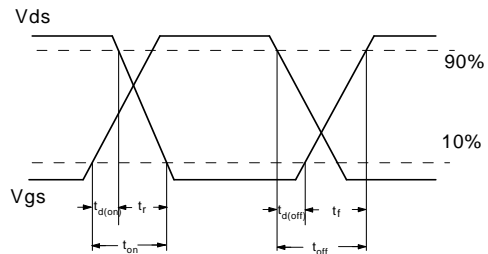
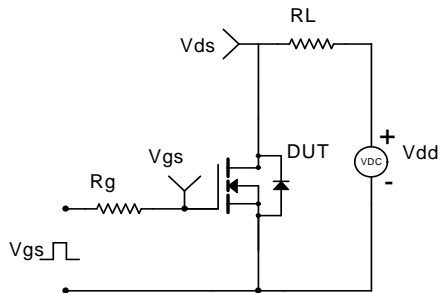


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

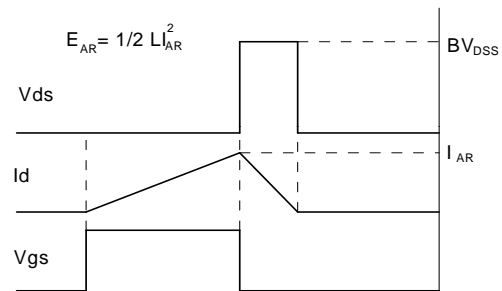
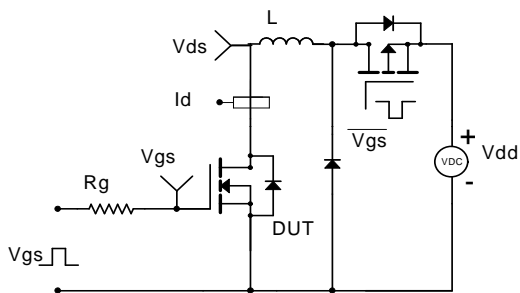
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

