FAIRCHILD
SEMICONDUCTOR ™

May 2000

QFET™

FQD1N50B / FQU1N50B

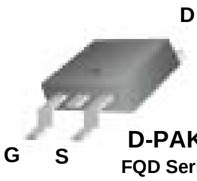
500V N-Channel MOSFET

General Description

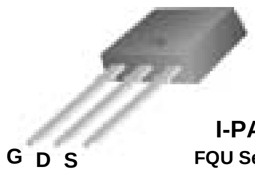
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

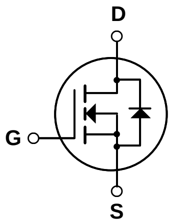
- 1.1A, 500V, $R_{DS(on)} = 9.0\Omega$ @V_{GS} = 10 V
- Low gate charge (typical 4.0 nC)
- Low Crss (typical 3.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



D-PAK
FQD Series



I-PAK
FQU Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQD1N50 / FQU1N50	Units
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_C = 25°C)		1.1	A
	- Continuous (T_C = 100°C)		0.7	A
I_{DM}	Drain Current - Pulsed	(Note 1)	4.4	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	80	mJ
I_{AR}	Avalanche Current	(Note 1)	1.1	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		25	W
	- Derate above 25°C		0.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	5.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

T_C = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.5	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.3	3.0	3.7	V
		V_{DS} = V_{GS}, I_D = 250 mA	3.6	4.3	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.55 A	--	6.8	9.0	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 0.55 A (Note 4)	--	0.98	--	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	115	150	pF
C_{oss}	Output Capacitance		--	20	30	pF
C_{rss}	Reverse Transfer Capacitance		--	3	4	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 1.4 A, R_G = 25 Ω (Note 4, 5)	--	5	20	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	8	25	ns
t_f	Turn-Off Fall Time		--	20	50	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 1.4 A, V_{GS} = 10 V (Note 4, 5)	--	4.0	5.5	nC
Q_{gs}	Gate-Source Charge		--	1.1	--	nC
Q_{gd}	Gate-Drain Charge		--	2.2	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.4	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	4.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.4 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 1.4 A, dI_F / dt = 100 A/µs (Note 4)	--	170	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.4	--	µC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 120mH, I_{AS} = 1.1A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \le$ 1.4A, di/dt $\le$ 200A/µs, $V_{DD} \le BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width $\le$ 300µs, Duty cycle $\le$ 2%
5. Essentially independent of operating temperature

Typical Characteristics

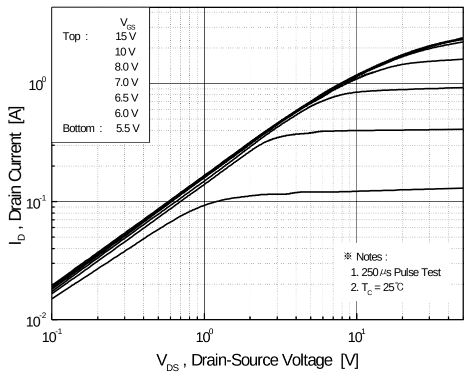


Figure 1. On-Region Characteristics.

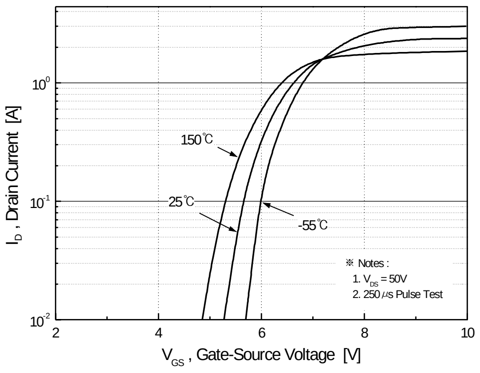


Figure 2. Transfer Characteristics.

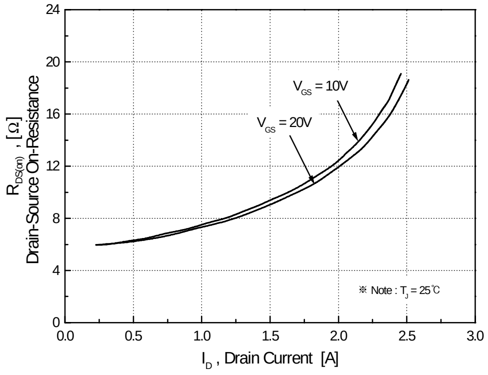


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage.

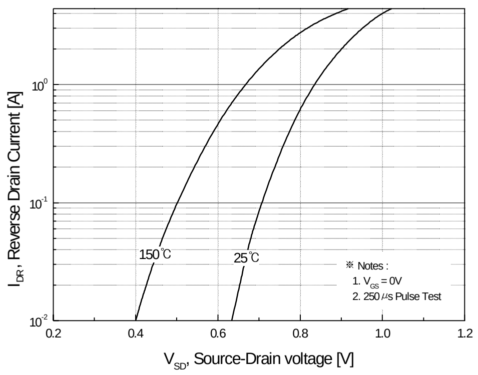


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature.

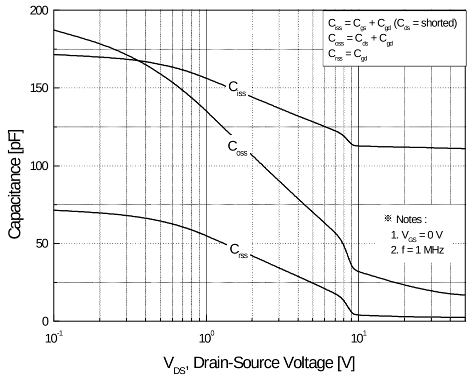


Figure 5. Capacitance Characteristics.

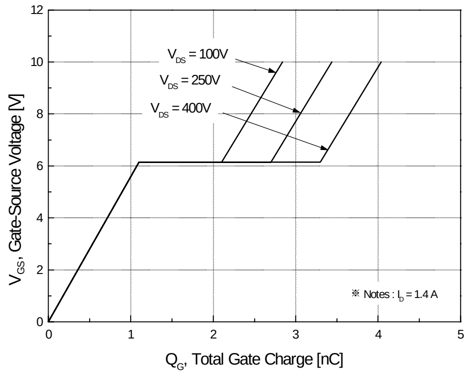


Figure 6. Gate -Charge Characteristics.

Typical Characteristics (Continued)

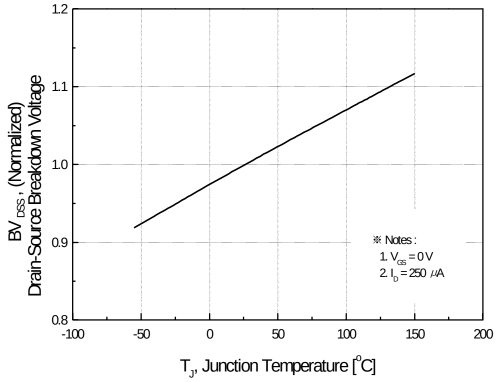


Figure 7. Breakdown Voltage Variation vs Temperature.

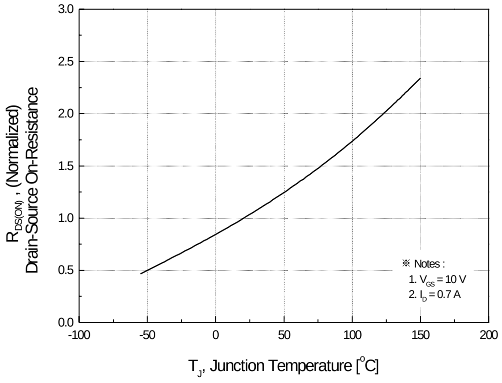


Figure 8. On-Resistance Variation vs Temperature.

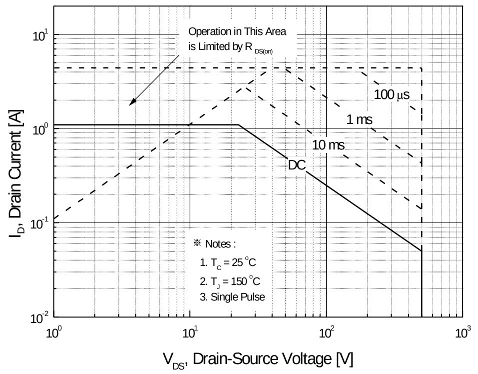


Figure 9. Maximum Safe Operating Area.

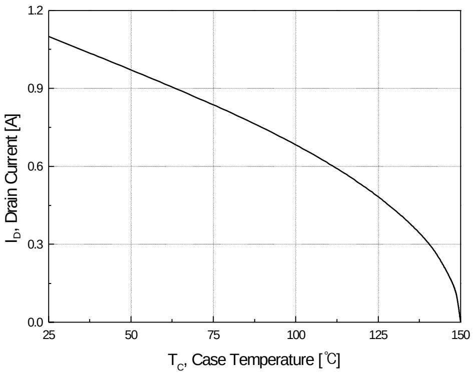


Figure 10. Maximum Drain Current vs Case Temperature.

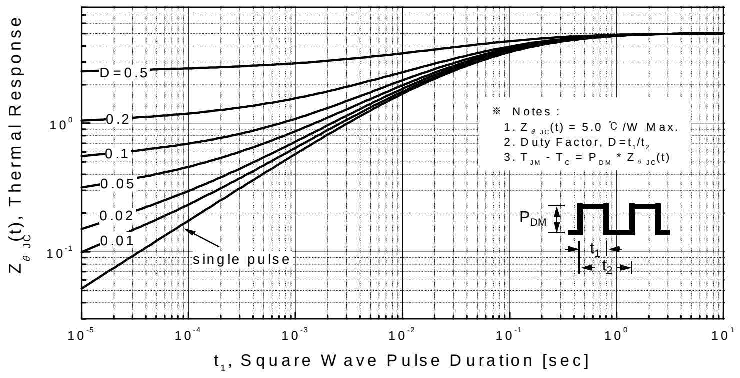
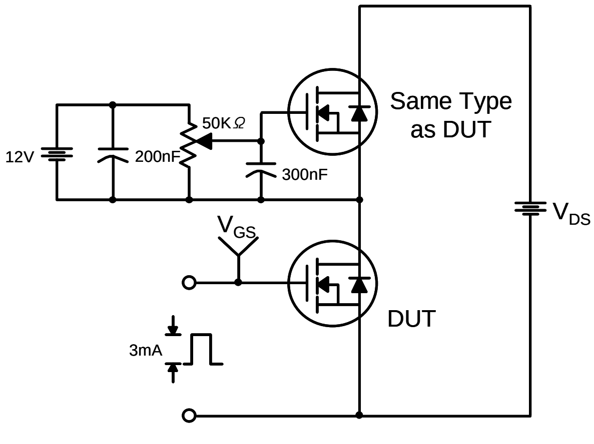
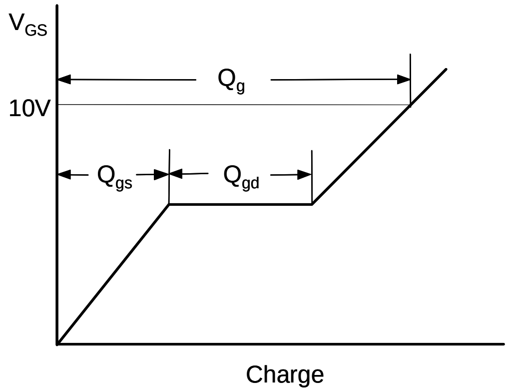


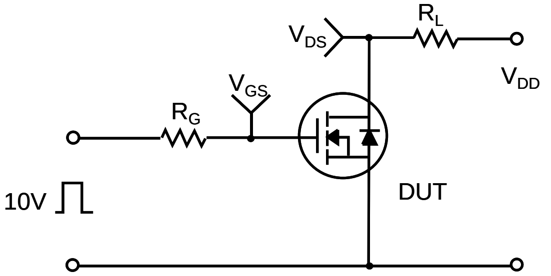
Figure 11. Transient Thermal Response Curve.

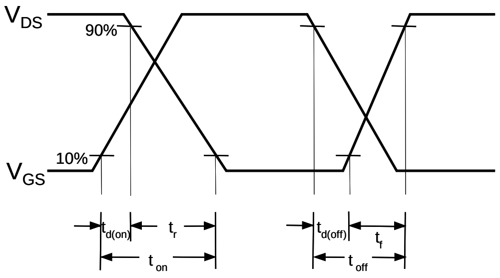
Gate Charge Test Circuit & Waveform



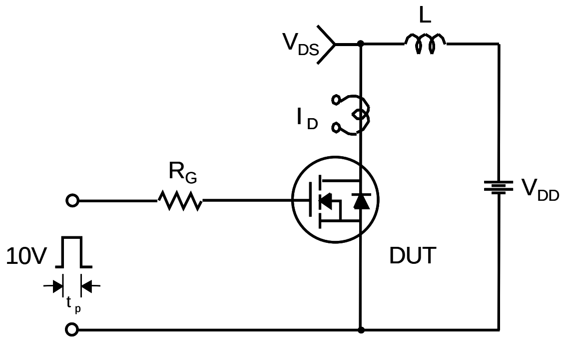


Resistive Switching Test Circuit & Waveforms

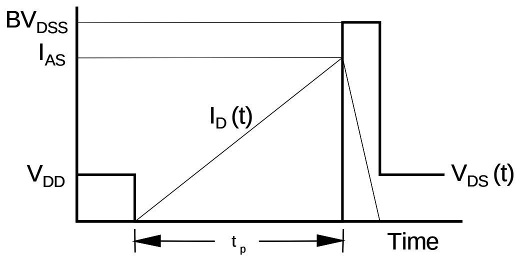




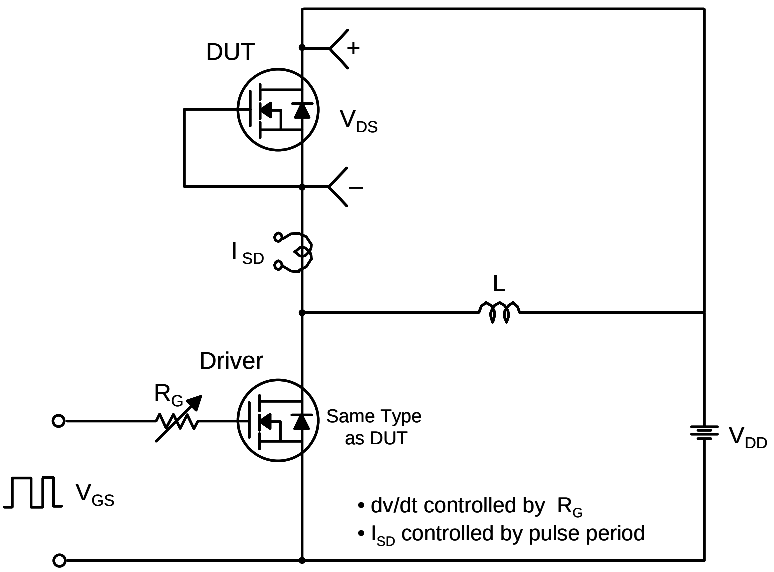
Unclamped Inductive Switching Test Circuit & Waveforms

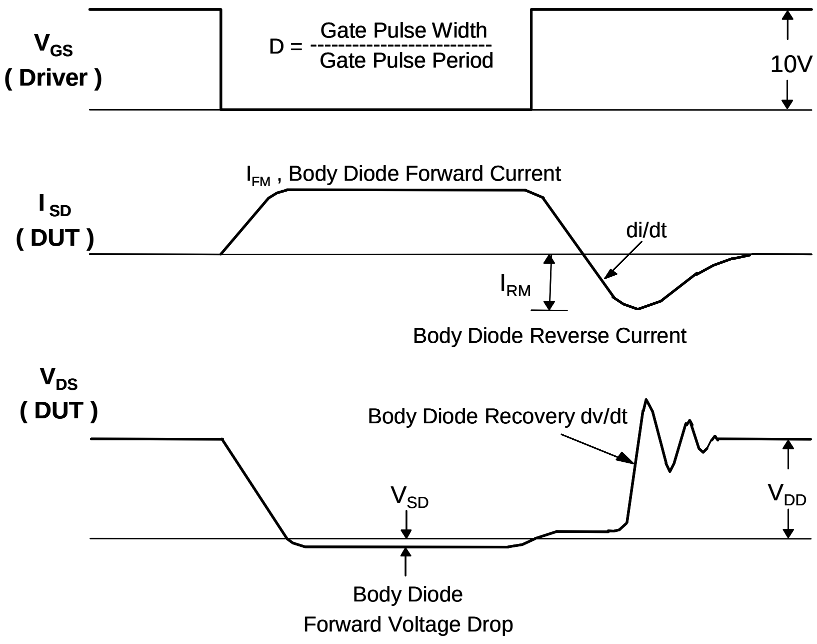


$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

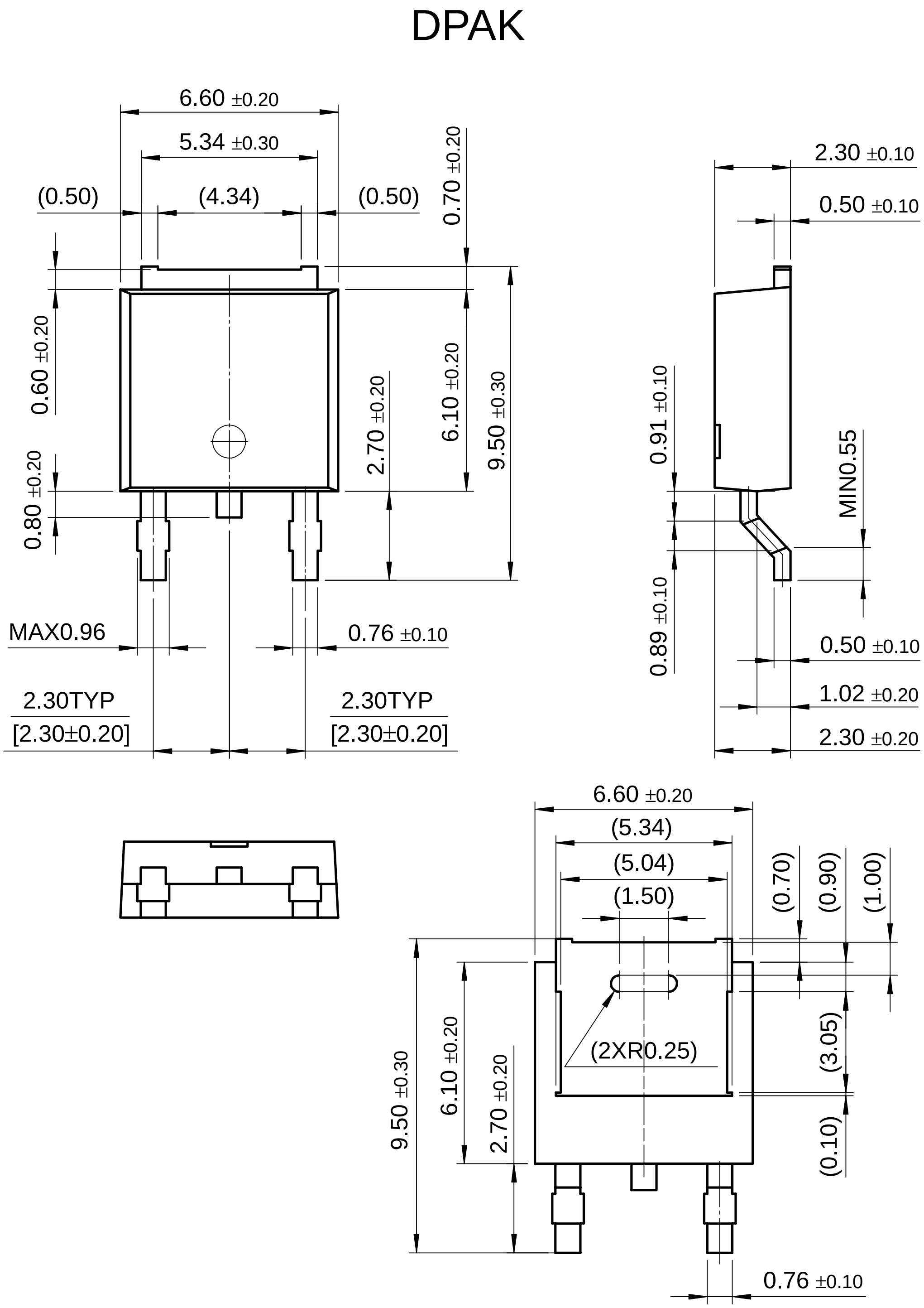


Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions



Package Dimensions (Continued)

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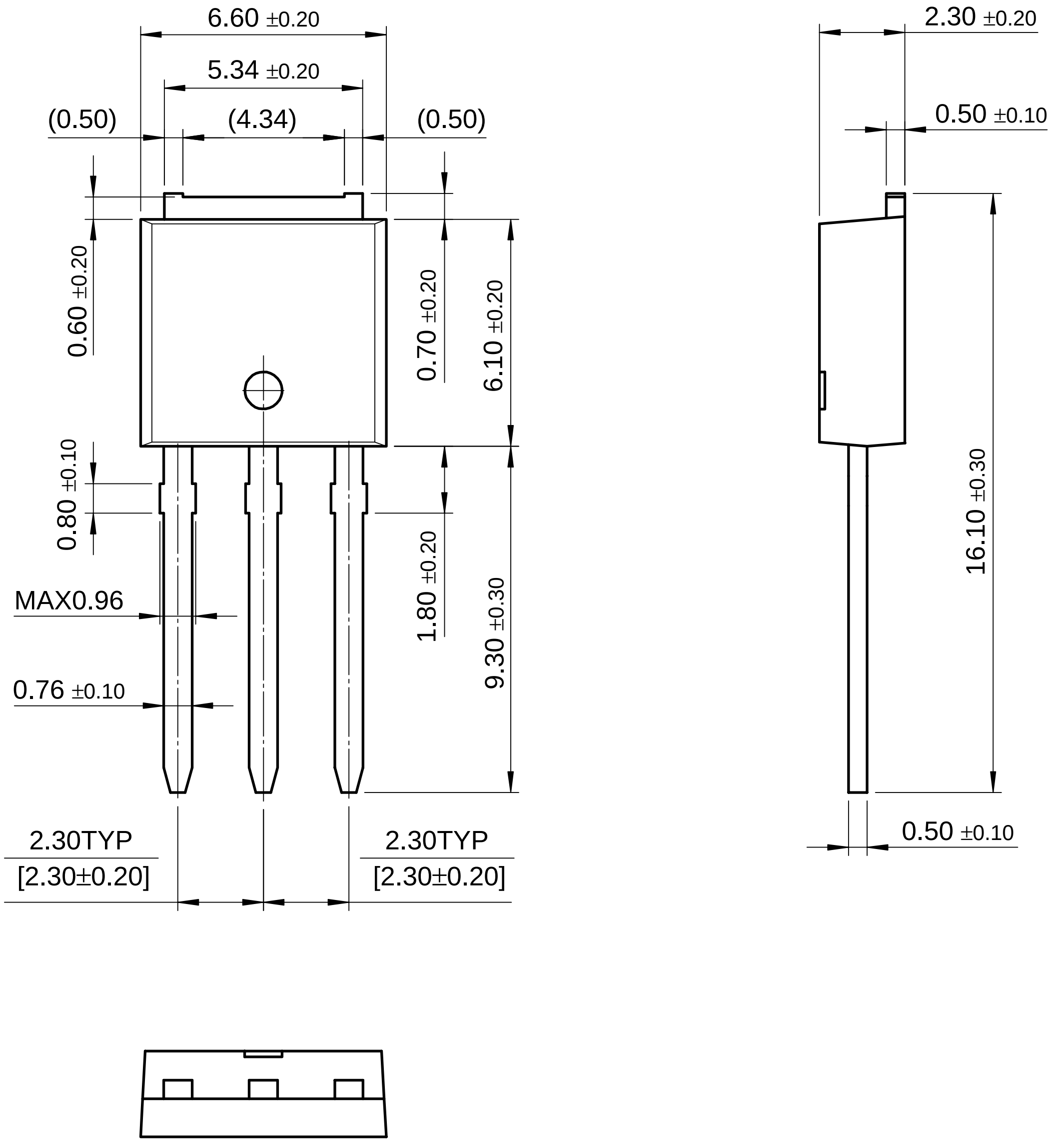

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