

MOSFET – N-Channel, QFET®

600 V, 1.9 A, 4,7 Ω

FQD2N60C / FQU2N60C

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

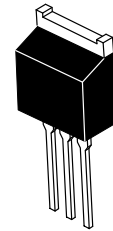
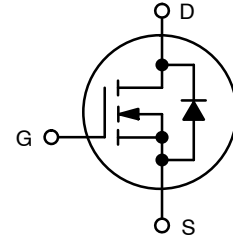
- 1.9 A, 600 V, $R_{DS(on)} = 4.7 \Omega$ (Max.) @ $V_{GS} = 10$ V, $I_D = 0.95$ A
- Low Gate Charge (Typ. 8.5 nC)
- Low C_{rss} (Typ. 4.3 pF)
- 100% Avalanche Tested
- These Devices are Halid Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

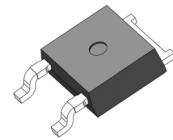
Symbol	Rating	Value	Unit
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$) – Continuous ($T_C = 100^\circ\text{C}$)	1.9	A
		1.14	
I_{DM}	Drain Current – Pulsed (Note 1)	7.6	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	120	mJ
I_{AR}	Avalanche Current (Note 1)	1.9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) * – Derate above 25°C	2.5	W
		44 0.35	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" (from case for 5 seconds)	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
600 V	4.7 Ω @ 10 V	1.9 A

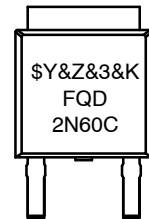
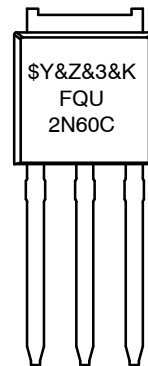


DPAK3 (IPAK)
CASE 369AR



DPAK3 (TO-252 3 LD)
CASE 369AS

MARKING DIAGRAMS



FQD2N60C,
FQU2N60C = Device Code
 \$Y = onsemi Logo
 &Z = Assembly Location
 &3 = Date Code
 &K = Lot Run Traceability Code

ORDERING INFORMATION

Device	Package	Shipping†
FQD2N60CTM	DPAK3 (TO-252 3 LD) (Pb-Free)	2500 / Tape & Reel
FQU2N60CTU	DPAK3 (IPAK) (Pb-Free)	70 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FQD2N60C / FQU2N60C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.87	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (minimum pad of 2 oz copper), Max.	110	$^{\circ}\text{C}/\text{W}$
	Thermal Resistance, Junction-to-Ambient (* 1 in ² pad of 2 oz copper), Max.	50	

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	600	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.6	-	$\text{V}/^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{V}, V_{GS} = 0 \text{V}$	-	-	1	μA
		$V_{DS} = 480 \text{V}, T_C = 125^{\circ}\text{C}$	-	-	10	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{V}, V_{DS} = 0 \text{V}$	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{V}, V_{DS} = 0 \text{V}$	-	-	-100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain-Source On Resistance	$V_{GS} = 10 \text{V}, I_D = 0.95 \text{A}$	-	3.6	4.7	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40 \text{V}, I_D = 0.95 \text{A}$	-	5.0	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{V}, V_{GS} = 0 \text{V}, f = 1.0 \text{MHz}$	-	180	235	pF
C_{oss}	Output Capacitance		-	20	25	
C_{rss}	Reverse Transfer Capacitance		-	4.3	5.6	

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300 \text{V}, I_D = 2 \text{A}, R_G = 25 \Omega$ (Note 4)	-	9	28	ns
t_r	Turn-On Rise Time		-	25	60	
$t_{d(off)}$	Turn-Off Delay Time		-	24	58	
t_f	Turn-Off Fall Time		-	28	66	
Q_g	Total Gate Charge	$V_{DS} = 480 \text{V}, I_D = 2 \text{A}, V_{GS} = 10 \text{V}$ (Note 4)	-	8.5	12	nC
Q_{gs}	Gate-Source Charge		-	1.3	-	
Q_{gd}	Gate-Drain Charge		-	4.1	-	

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	1.9	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	-	-	7.6	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{V}, I_S = 1.6 \text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{V}, I_S = 2 \text{A}, di/dt = 100 \text{A}/\mu\text{s}$	-	230	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.0	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $L = 56 \text{mH}, I_{AS} = 2 \text{A}, V_{DD} = 50 \text{V}, R_G = 25 \Omega$, Starting $T_J = 25^{\circ}\text{C}$.
3. $I_{SD} \leq 2.0 \text{A}, di/dt \leq 200 \text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$.
4. Essentially independent of operating temperature.

FQD2N60C / FQU2N60C

TYPICAL CHARACTERISTICS

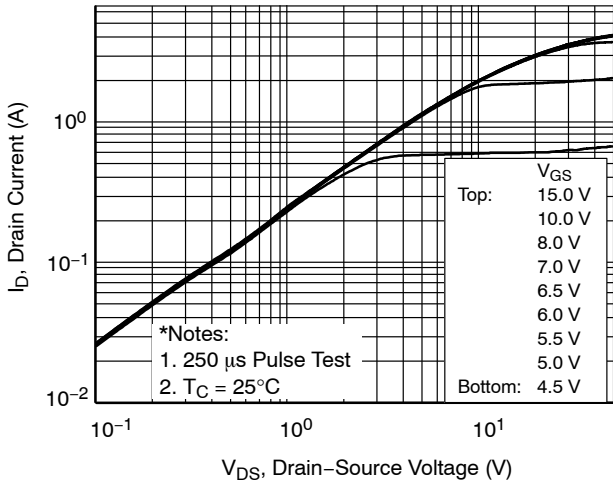


Figure 1. On-Region Characteristics

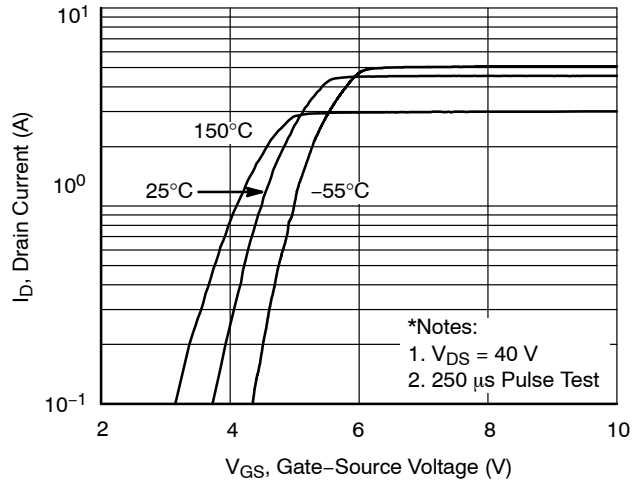


Figure 2. Transfer Characteristics

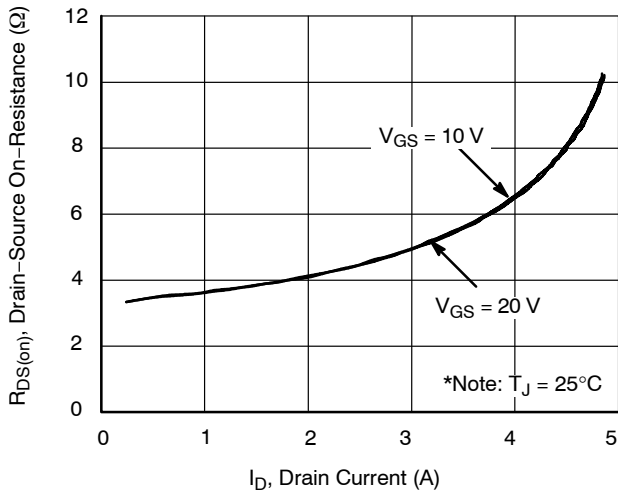


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

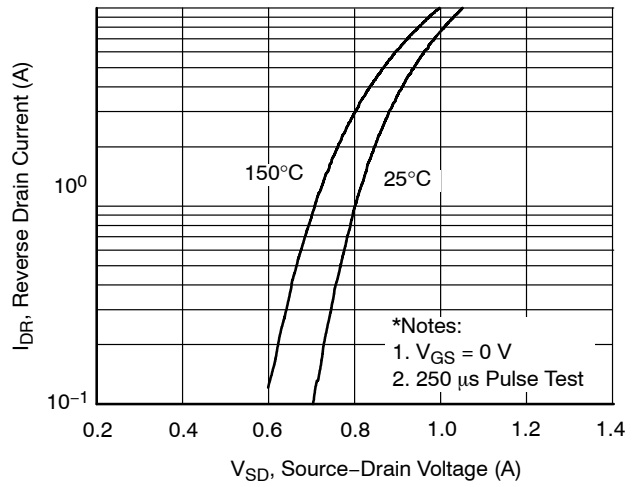


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

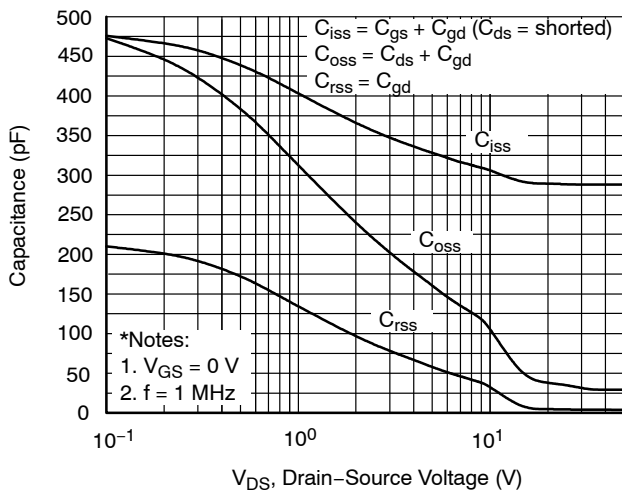


Figure 5. Capacitance Characteristics

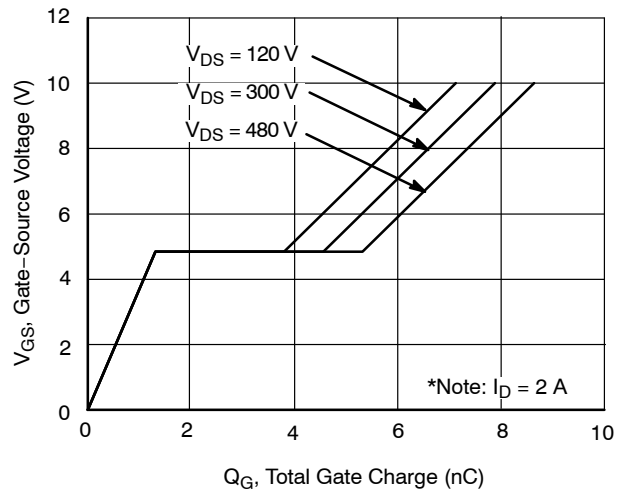


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (continued)

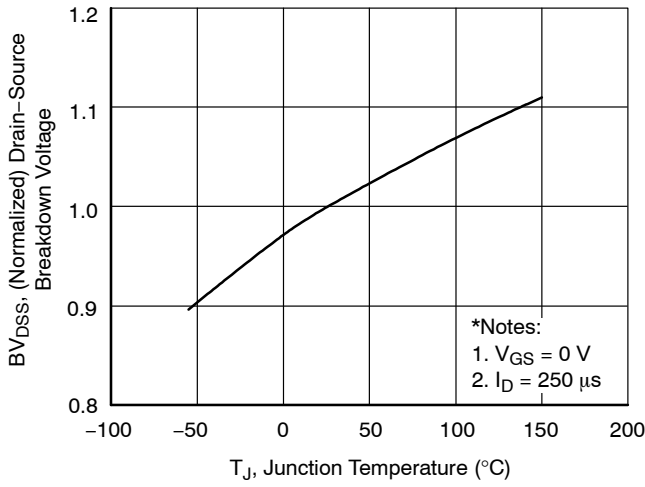


Figure 7. Breakdown Voltage Variation vs. Temperature

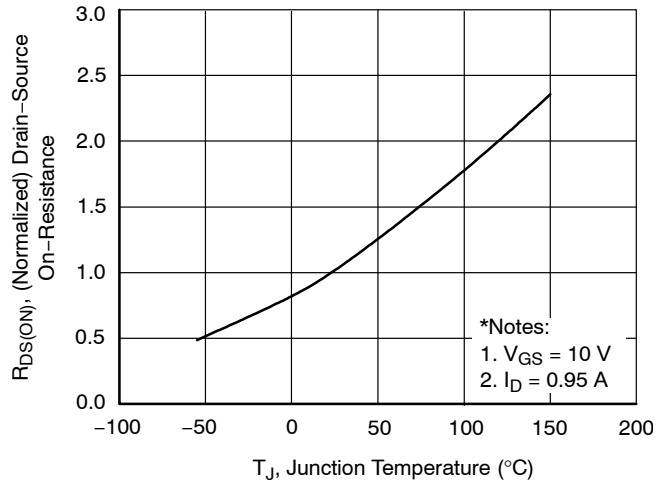


Figure 8. On-Resistance Variation vs. Temperature

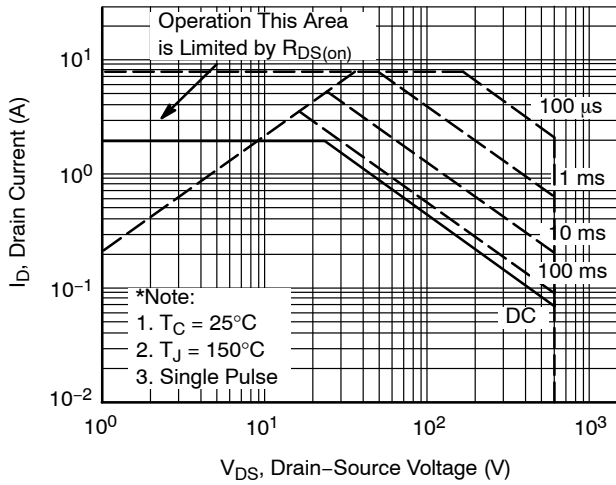


Figure 9. Maximum Safe Operating Area

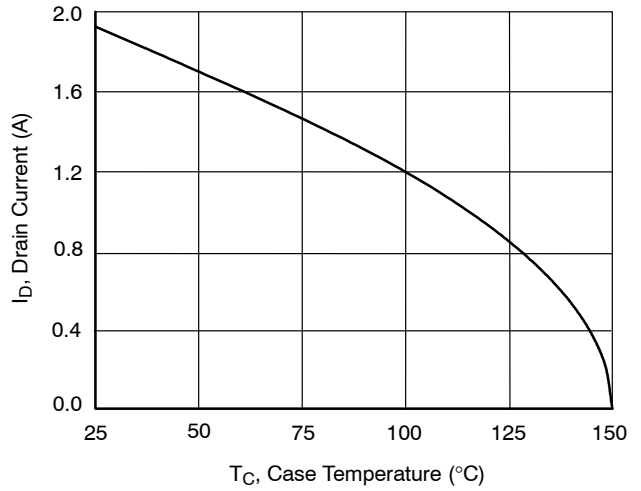


Figure 10. Maximum Drain Current vs. Case Temperature

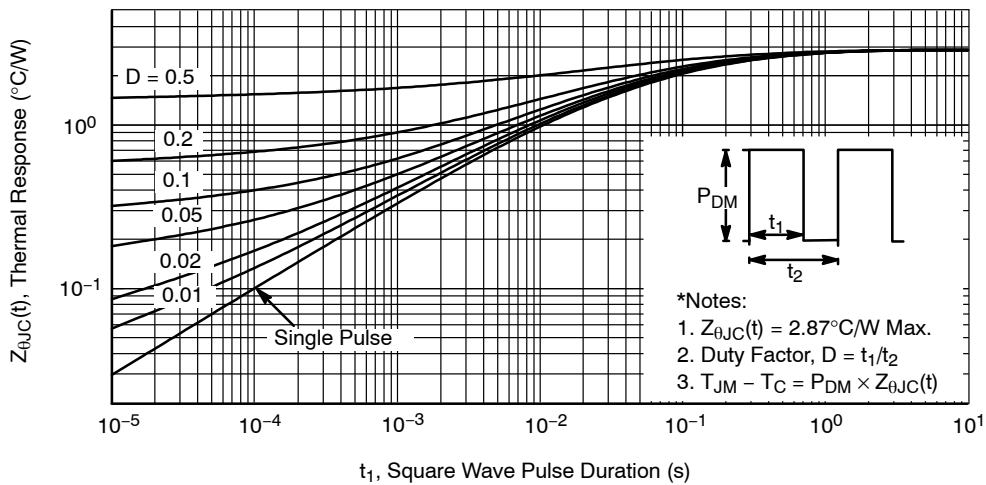


Figure 11. Transient Thermal Response Curve

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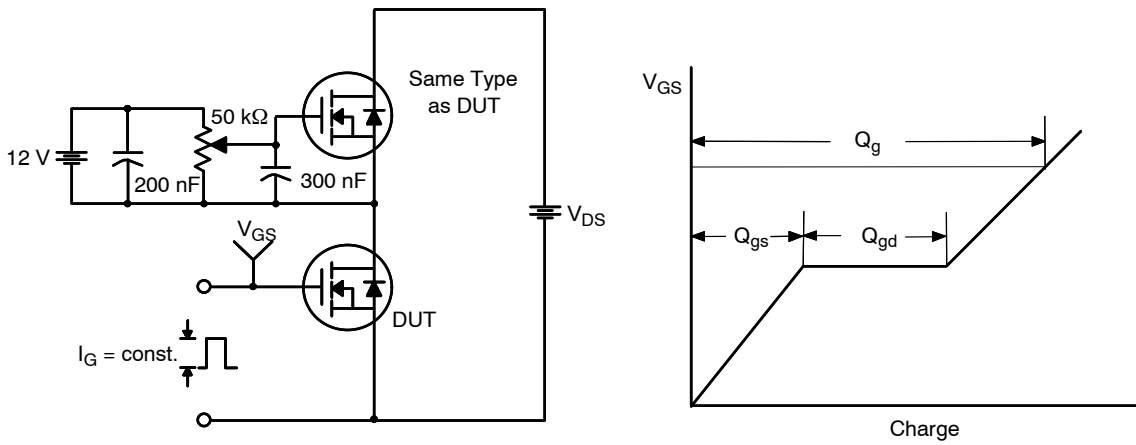


Figure 12. Gate Charge Test Circuit & Waveform

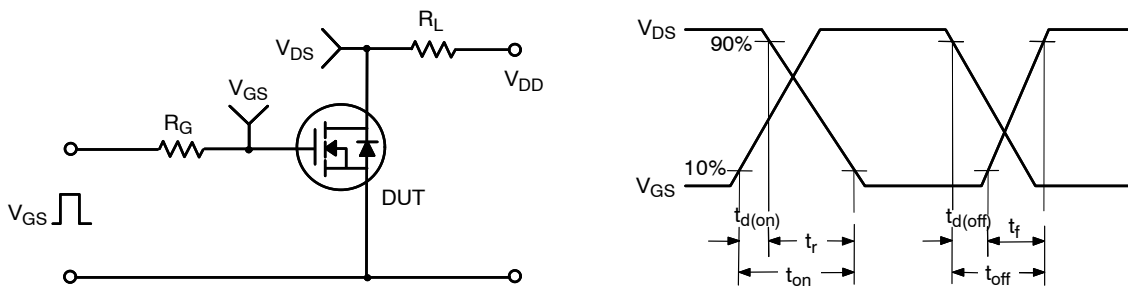


Figure 13. Resistive Switching Test Circuit & Waveforms

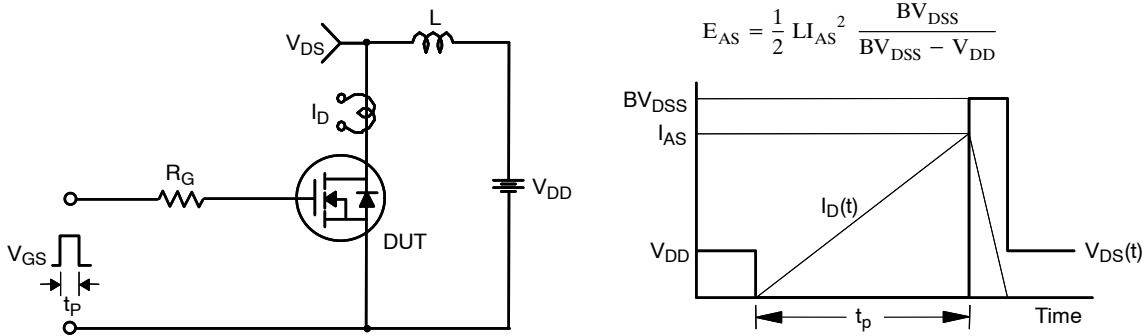


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FQD2N60C / FQU2N60C

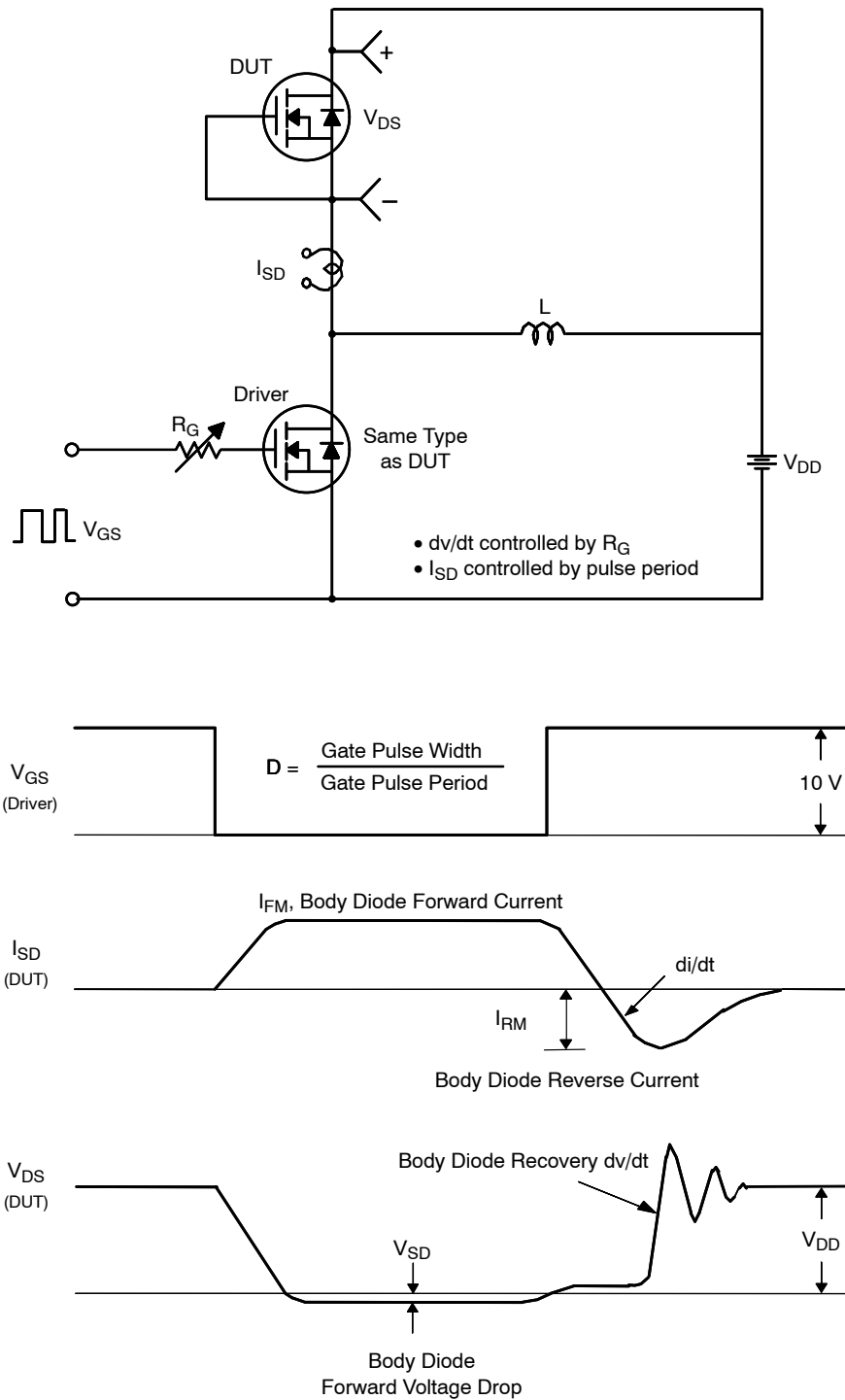


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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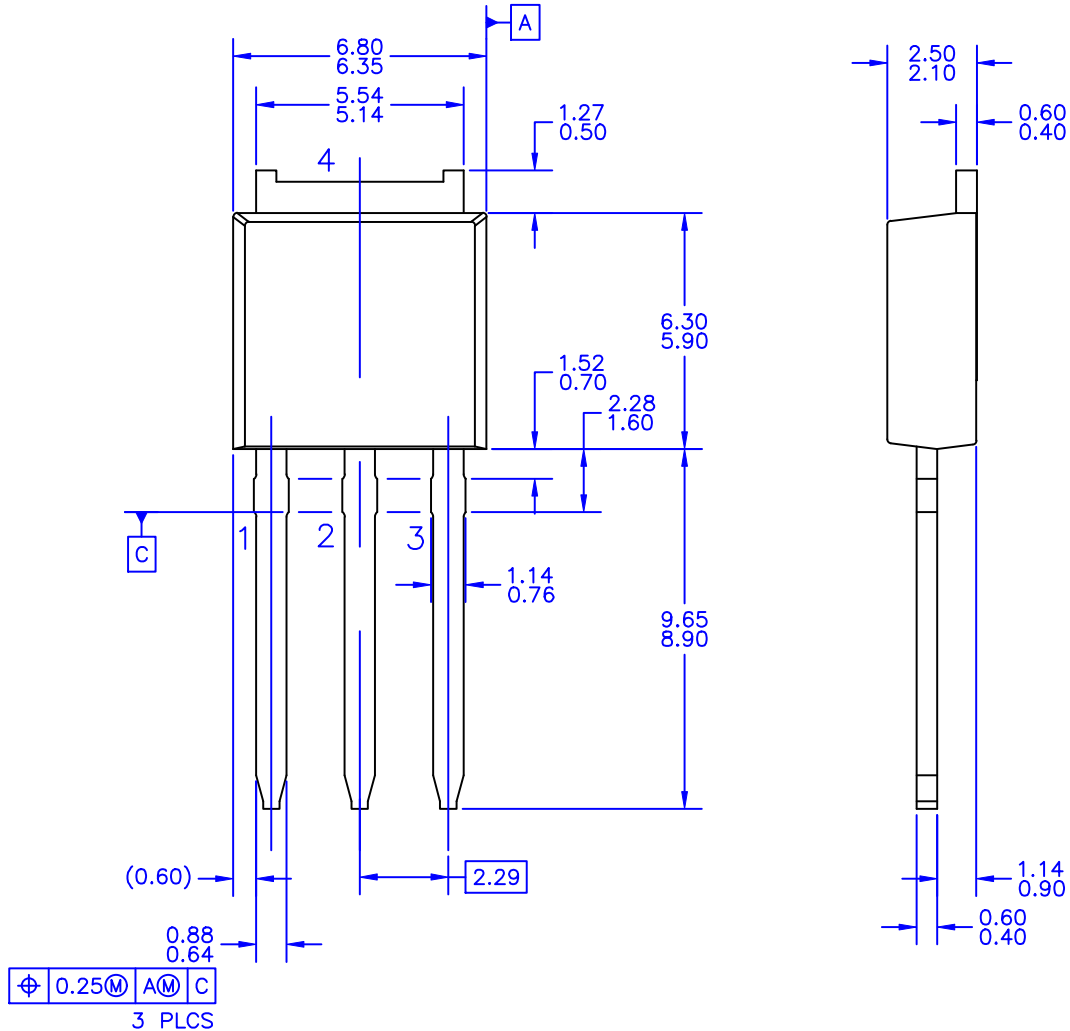
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



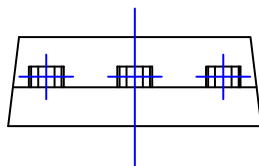
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CASE 369AR
ISSUE O

DATE 30 SEP 2016



NOTES: UNLESS OTHERWISE SPECIFIED

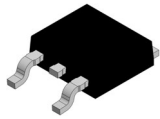
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- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.



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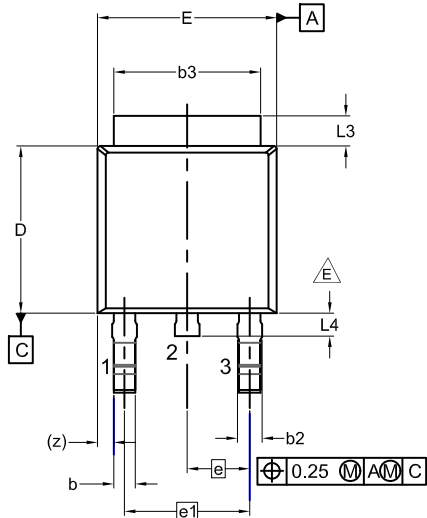
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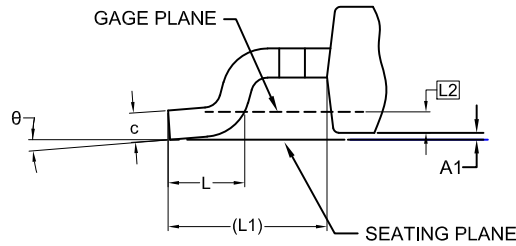


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DATE 28 SEP 2022

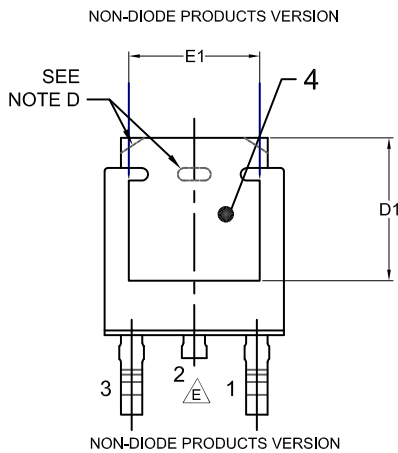


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 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	-	-
E	6.35	6.54	6.73
E1	4.32	-	-
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	-	-	1.02
theta	0°	--	10°

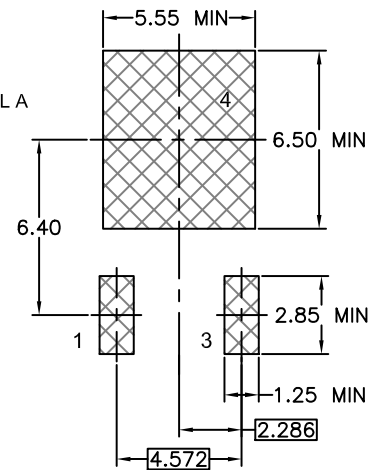
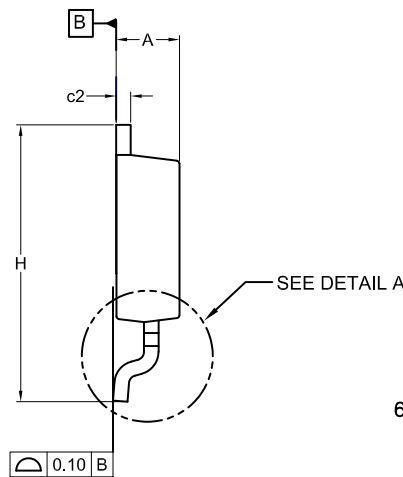


GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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