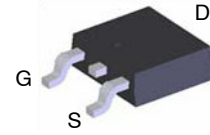


MOSFET – P-Channel, QFET®

-500 V, 4.9 Ω, -2.1 A

FQD3P50



DPAK3
CASE 369AS

Description

This P-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

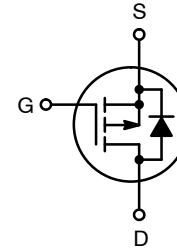
- -2.1 A, -500 V, $R_{DS(on)} = 4.9 \Omega$ (Max.) @ $V_{GS} = -10$ V, $I_D = -1.05$ A
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 9.5 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_C = 20^\circ\text{C}$ unless otherwise noted)

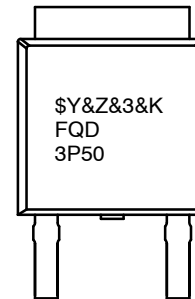
Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	-500	V
I_D	Drain Current		A
	- Continuous ($T_C = 25^\circ\text{C}$)	-2.1	
	- Continuous ($T_C = 100^\circ\text{C}$)	-1.33	
I_{DM}	Drain Current - Pulsed (Note 1)	-8.4	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	250	mJ
I_{AR}	Avalanche Current (Note 1)	-2.1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) (Note 4)	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	50 0.4	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $L = 102$ mH, $I_{AS} = -2.1$ A, $V_{DD} = -50$ V, $R_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq -2.7$ A, $di/dt \leq 200$ A/ms, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.
4. When mounted on the minimum pad size recommended (PCB Mount).



MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Code
- &3 = Date Code (Year and Week)
- &K = Lot Code
- FQD3P50 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FQD3P50	DPAK3 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FQD3P50

THERMAL CHARACTERISTICS

Symbol	Parameter	FQD3P50	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case, Max.	2.5	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient, Max. (Note 5)	50	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W

5. When mounted on the minimum pad size recommended (PCB Mount).

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 mA	-500	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = -250 mA, Referenced to 25°C	-	0.42	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -500 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -400 V, T _C = 125°C	-	-	-10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = -30 V, V _{DS} = 0 V	-	-	-100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = 30 V, V _{DS} = 0 V	-	-	100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 mA	-3.0	-	-5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -1.05 A	-	3.9	4.9	Ω
g _{FS}	Forward Transconductance	V _{DS} = -50 V, I _D = -1.05 A	-	2.1	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -25 V, V _{GS} = 0 V, f = 1.0 MHz	-	510	660	pF
C _{oss}	Output Capacitance		-	70	90	pF
C _{rss}	Reverse Transfer Capacitance		-	9.5	12	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -250 V, I _D = -2.7 A, R _G = 25 Ω (Note 6)	-	12	35	ns
t _r	Turn-On Rise Time		-	56	120	ns
t _{d(off)}	Turn-Off Delay Time		-	35	80	ns
t _f	Turn-Off Fall Time		-	45	100	ns
Q _g	Total Gate Charge	V _{DS} = -400 V, I _D = -2.7 A, V _{GS} = -10 V (Note 6)	-	18	23	nC
Q _{gs}	Gate-Source Charge		-	3.6	-	nC
Q _{gd}	Gate-Drain Charge		-	9.2	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current	-	-	-2.1	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	-	-	-8.4	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -2.1 A	-	-	-5.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = -2.7 A, dI _F /dt = 100 A/ms	-	270	-	ns
Q _{rr}	Reverse Recovery Charge		-	1.5	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CURVES

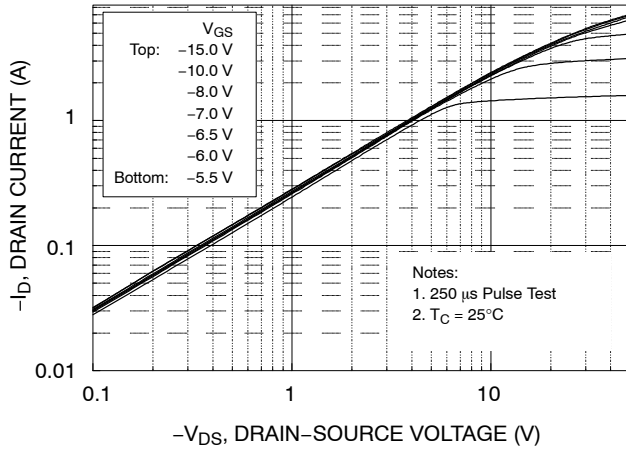


Figure 1. On-Region Characteristics

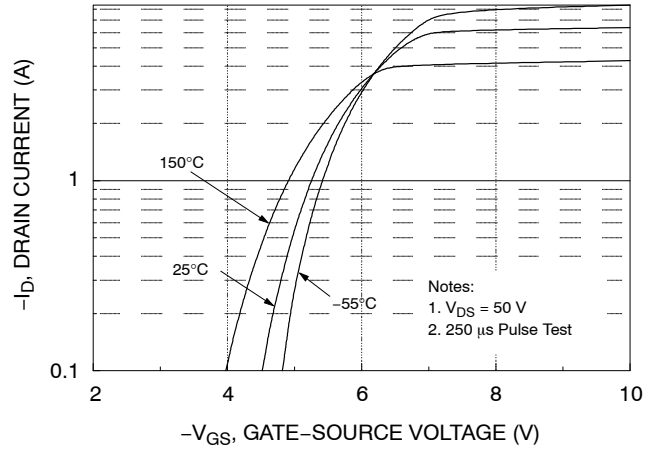


Figure 2. Transfer Characteristics

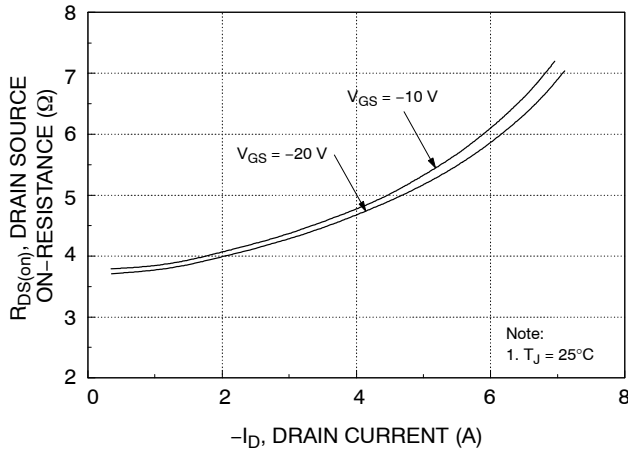


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

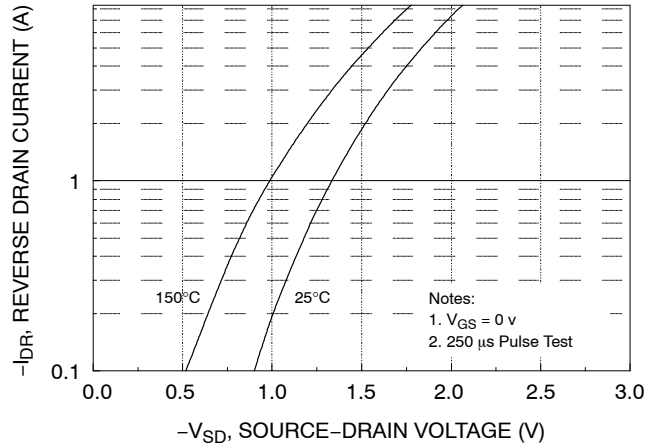


Figure 4. Body Diode Forward Voltage Variant vs. Source Current and Temperature

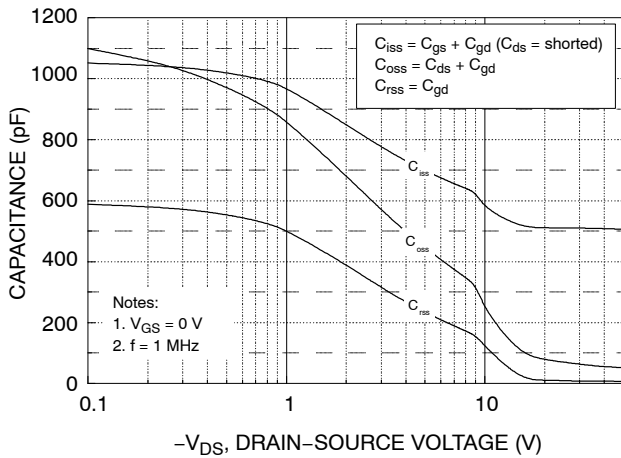


Figure 5. Capacitance Characteristics

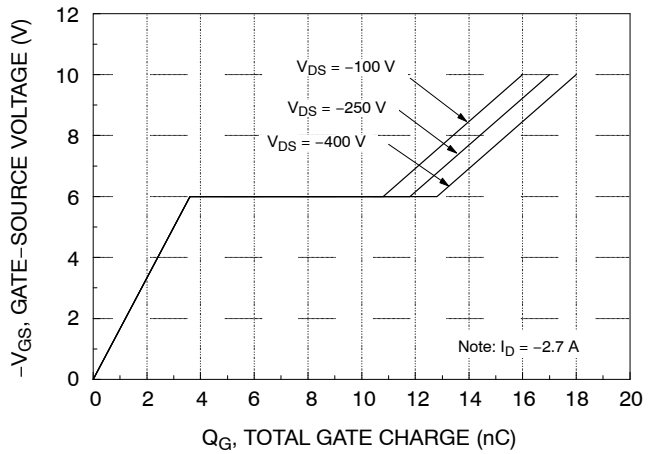


Figure 6. Gate Charge Characteristics

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TYPICAL PERFORMANCE CURVES (CONTINUED)

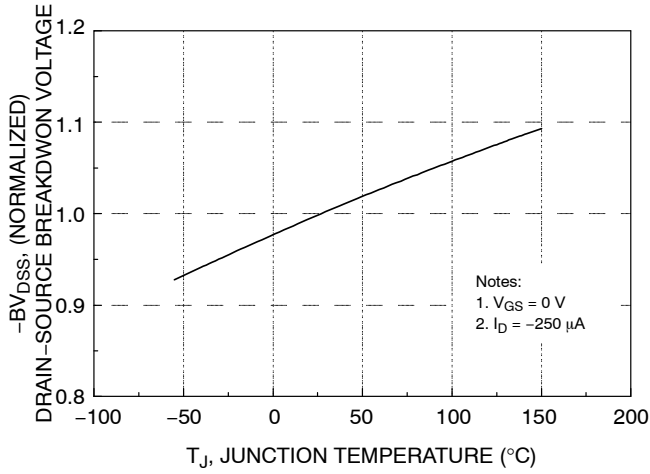


Figure 7. Breakdown Voltage Variation vs. Temperature

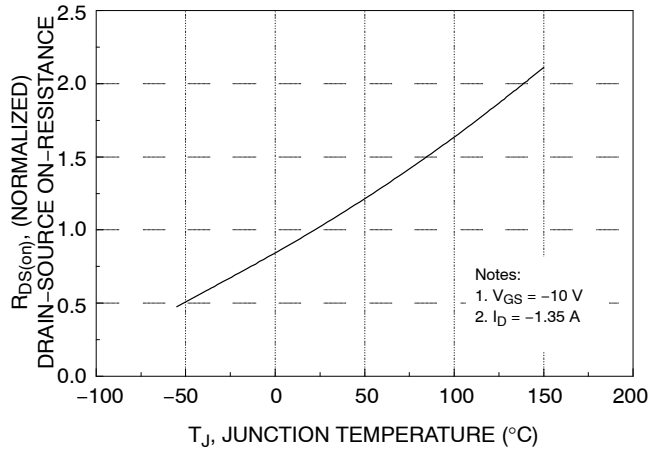


Figure 8. On-Resistance Variation vs. Temperature

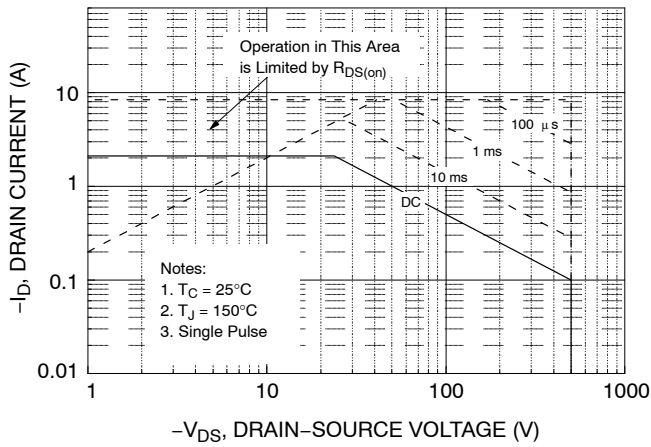


Figure 9. Maximum Safe Operation Area

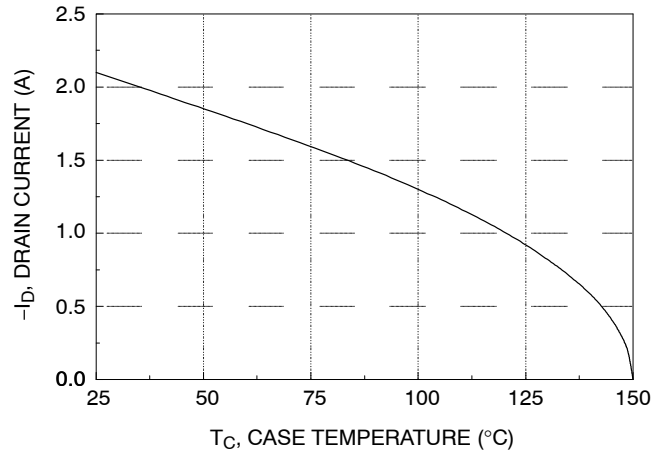


Figure 10. Maximum Drain Current vs. Case Temperature

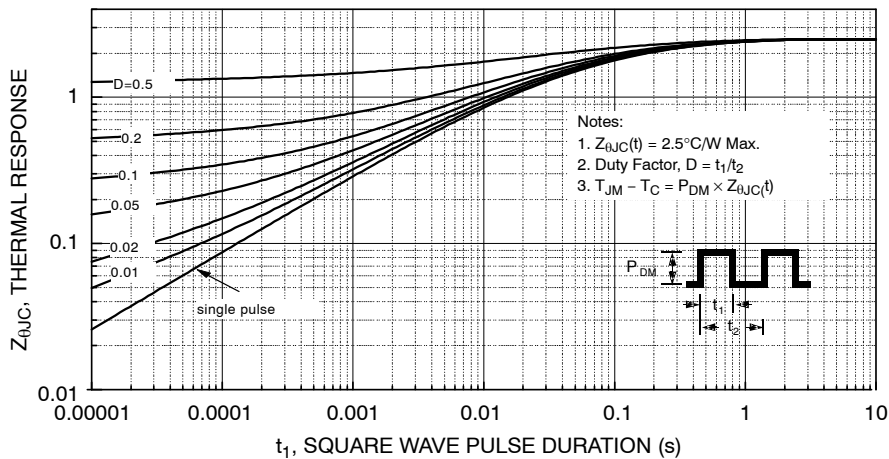


Figure 11. Transient Thermal Response Curve

FQD3P50

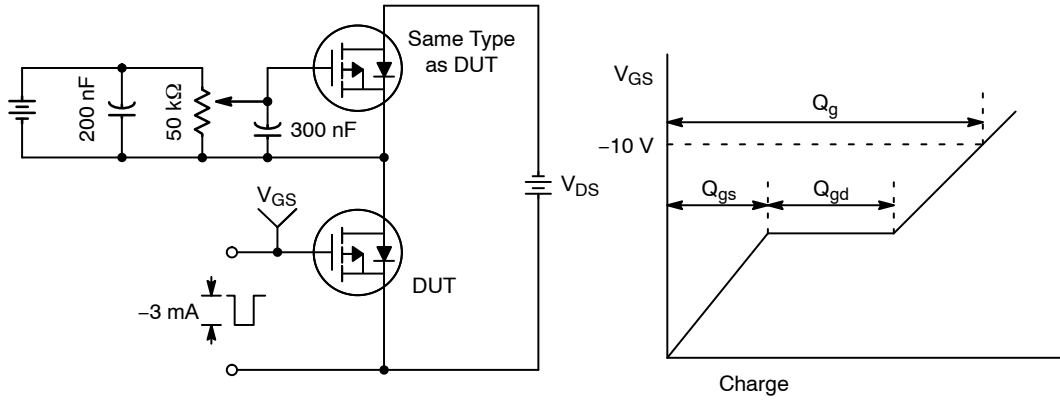


Figure 12. Gate Charge Test Circuit & Waveform

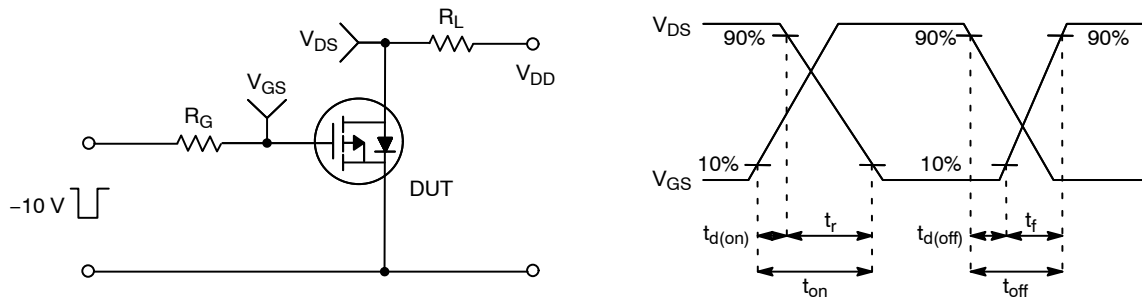


Figure 13. Resistive Switching Test Circuit & Waveforms

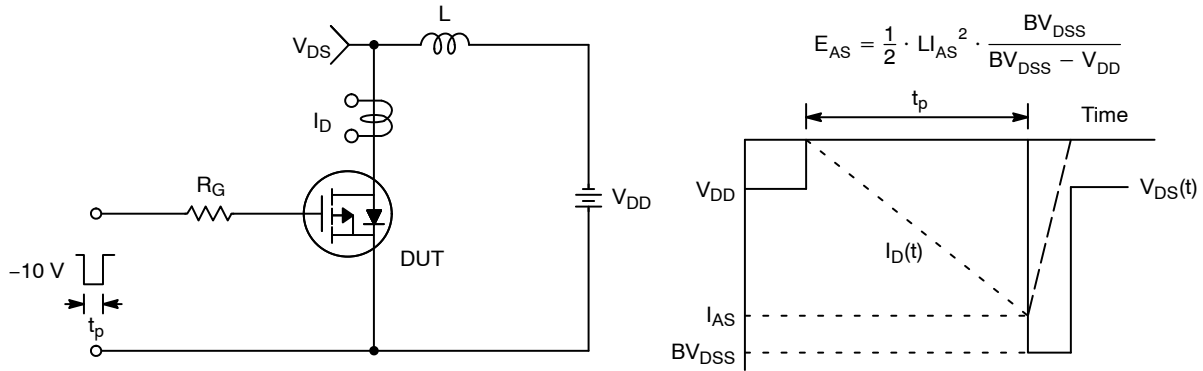


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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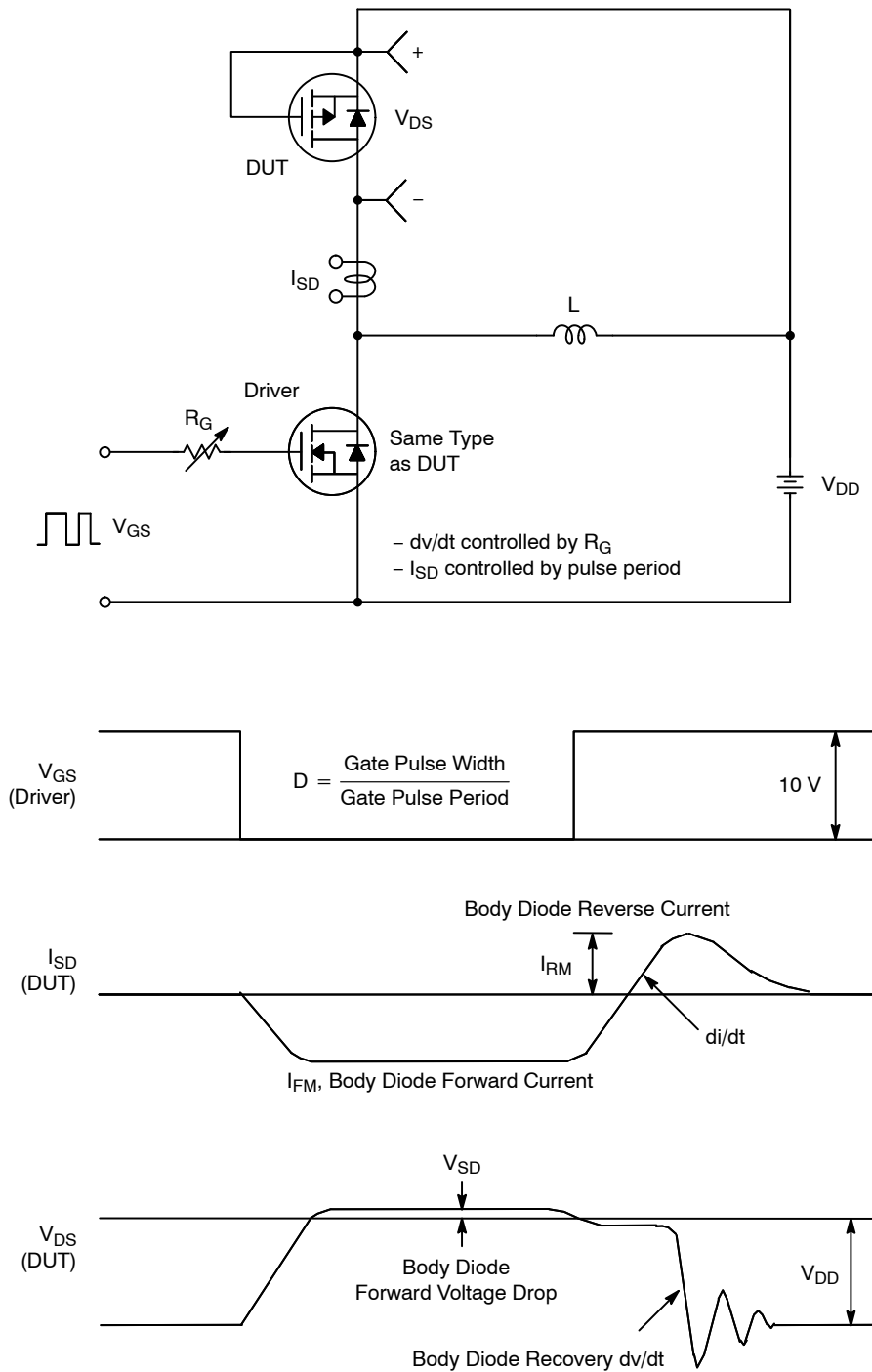
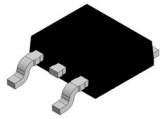


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

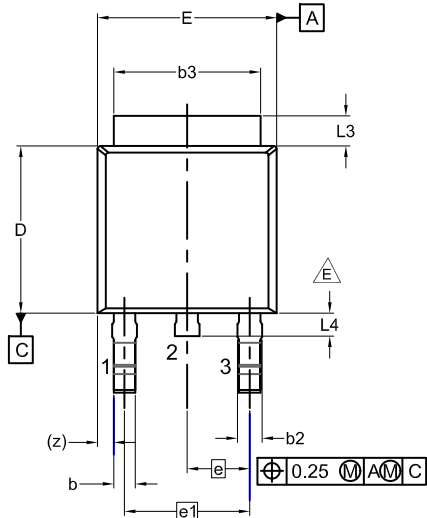
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

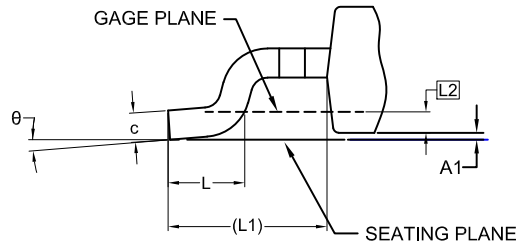


DPAK3 (TO-252 3 LD) CASE 369AS ISSUE A

DATE 28 SEP 2022

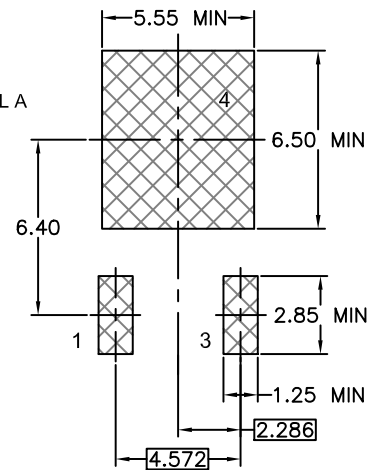
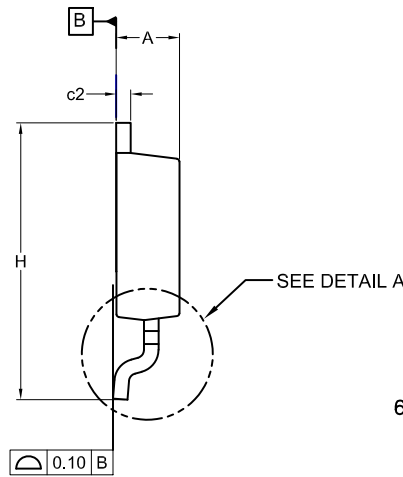
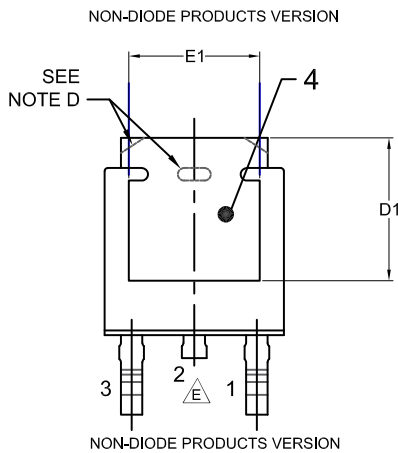


- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	-	-
E	6.35	6.54	6.73
E1	4.32	-	-
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	-	-	1.02
theta	0°	--	10°



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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