



ON Semiconductor®

FQD3P50TM-F085

500V P-Channel MOSFET

General Description

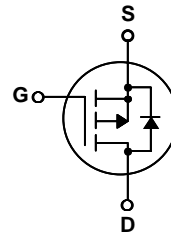
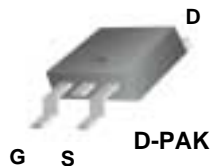
These P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on complimentary half bridge.

Features

- -2.1A, -500V, $R_{DS(on)} = 4.9\Omega @ V_{GS} = -10V$
- Low gate charge (typical 18 nC)
- Low Crss (typical 9.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Qualified to AEC Q101
- RoHS Compliant



FQD3P50TM-F085 500V P-Channel MOSFET



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	FQD3P50TM-F085	Units
V _{DSS}	Drain-Source Voltage	-500	V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)	-2.1	A
		-1.33	A
I _{DM}	Drain Current - Pulsed (Note 1)	-8.4	A
V _{GSS}	Gate-Source Voltage	± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	250	mJ
I _{AR}	Avalanche Current (Note 1)	-2.1	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
P _D	Power Dissipation (T _A = 25°C) *	2.5	W
	Power Dissipation (T _C = 25°C) - Derate above 25°C	50	W
		0.4	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	--	2.5	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	--	0.42	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	μA
		$V_{DS} = -400\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.05\text{ A}$	--	3.9	4.9	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.05\text{ A}$ (Note 4)	--	2.1	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	510	660	pF
C_{oss}	Output Capacitance		--	70	90	pF
C_{rss}	Reverse Transfer Capacitance		--	9.5	12	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -250\text{ V}, I_D = -2.7\text{ A},$ $R_G = 25\ \Omega$	--	12	35	ns	
t_r	Turn-On Rise Time		--	56	120	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	35	80	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	45	100	ns
Q_g	Total Gate Charge	$V_{DS} = -400\text{ V}, I_D = -2.7\text{ A},$ $V_{GS} = -10\text{ V}$	--	18	23	nC	
Q_{gs}	Gate-Source Charge		(Note 4, 5)	--	3.6	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	9.2	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	-2.1	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-8.4	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -2.7\text{ A},$	--	270	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	1.5	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 102\text{mH}, I_{AS} = -2.1\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq -2.7\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

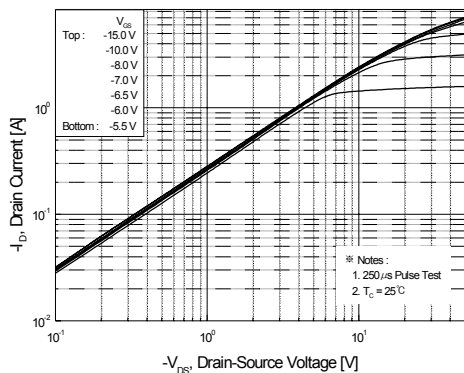


Figure 1. On-Region Characteristics

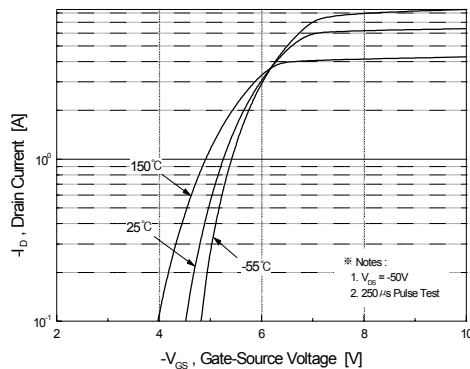


Figure 2. Transfer Characteristics

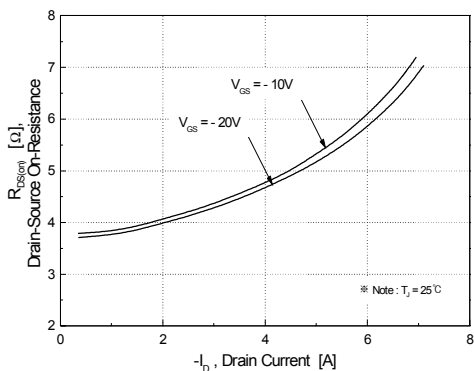


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

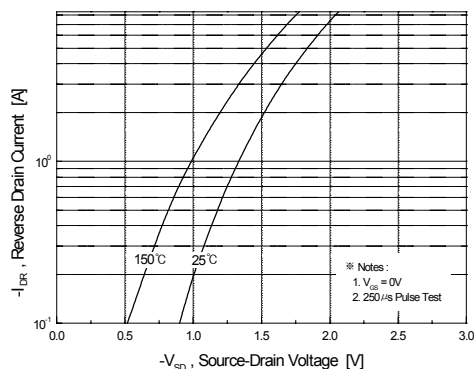


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

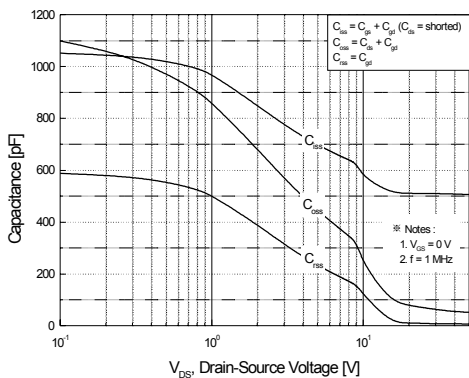


Figure 5. Capacitance Characteristics

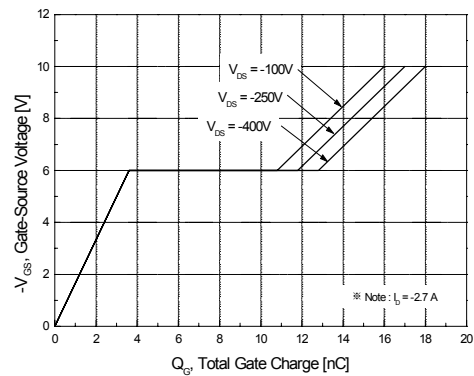


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

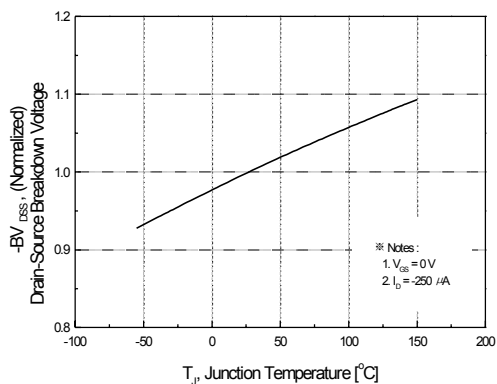


Figure 7. Breakdown Voltage Variation vs. Temperature

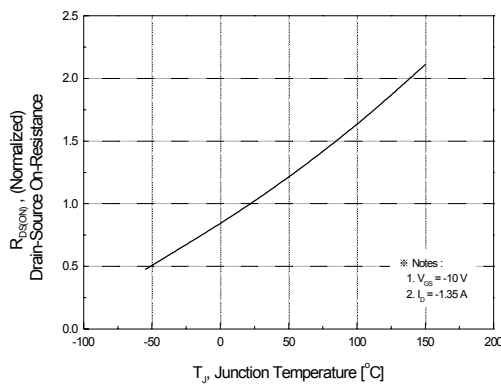


Figure 8. On-Resistance Variation vs. Temperature

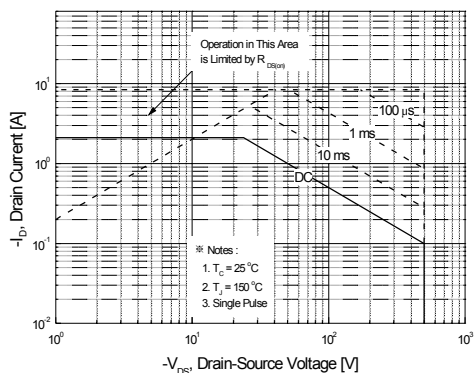


Figure 9. Maximum Safe Operating Area

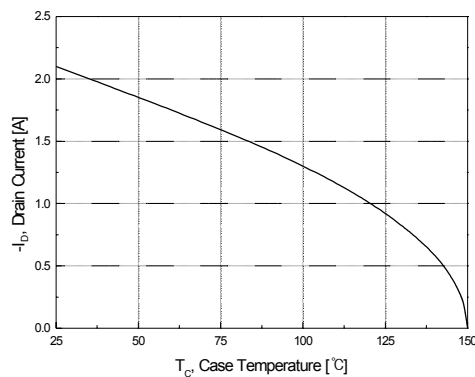


Figure 10. Maximum Drain Current vs. Case Temperature

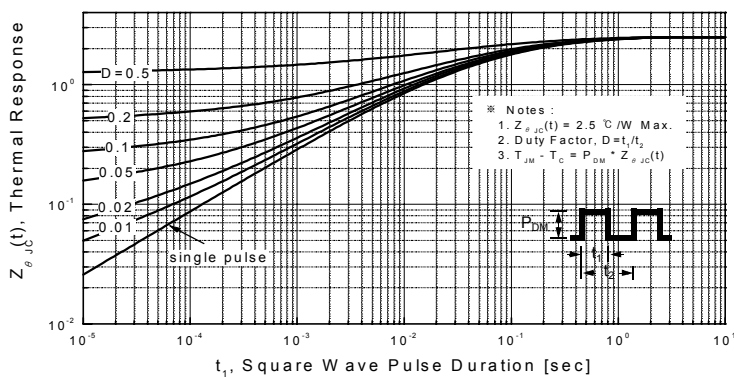
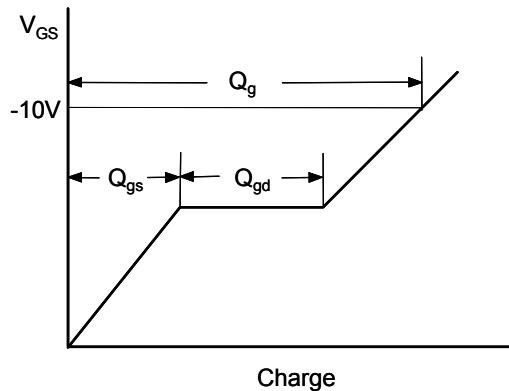
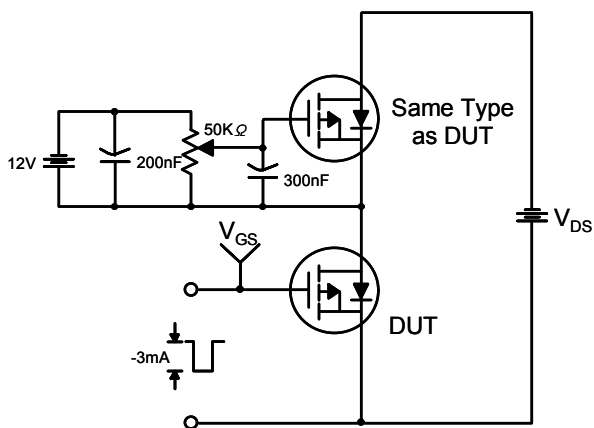
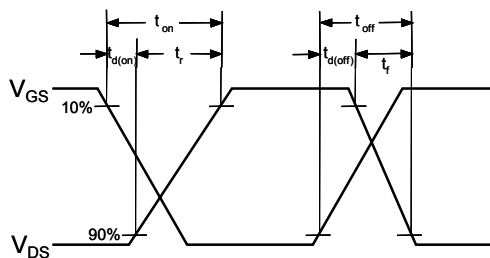
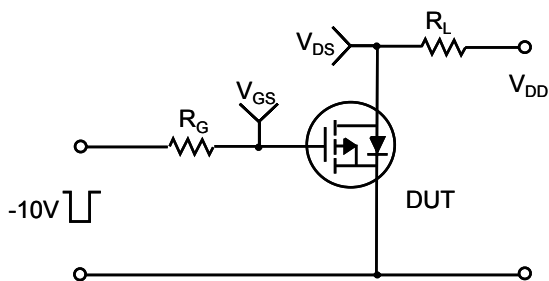


Figure 11. Transient Thermal Response Curve

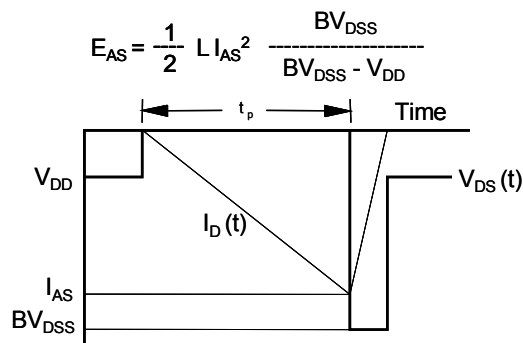
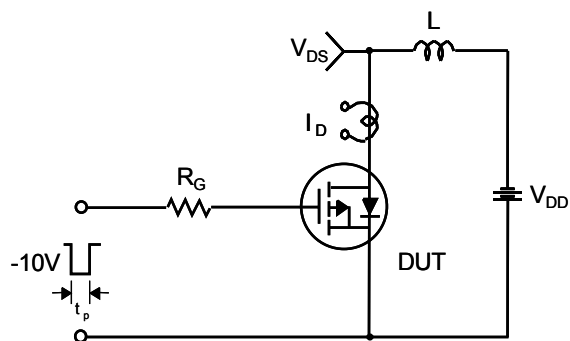
Gate Charge Test Circuit & Waveform



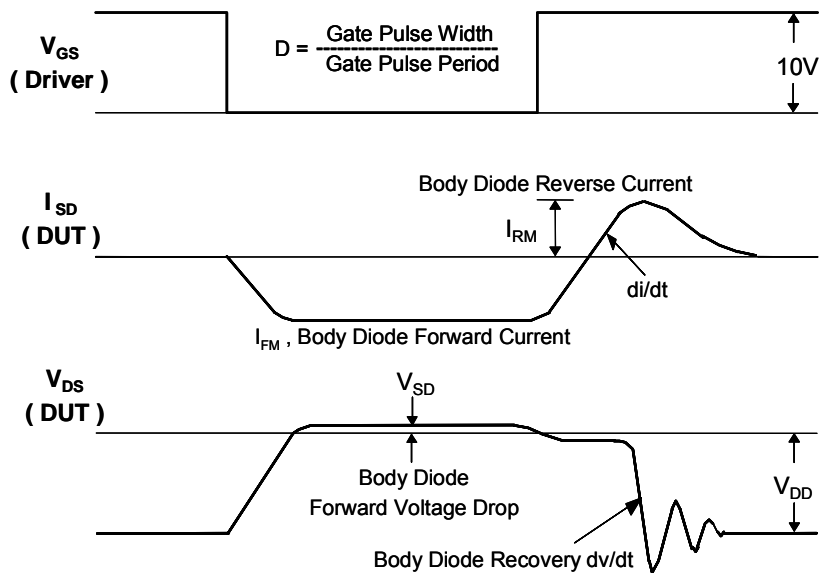
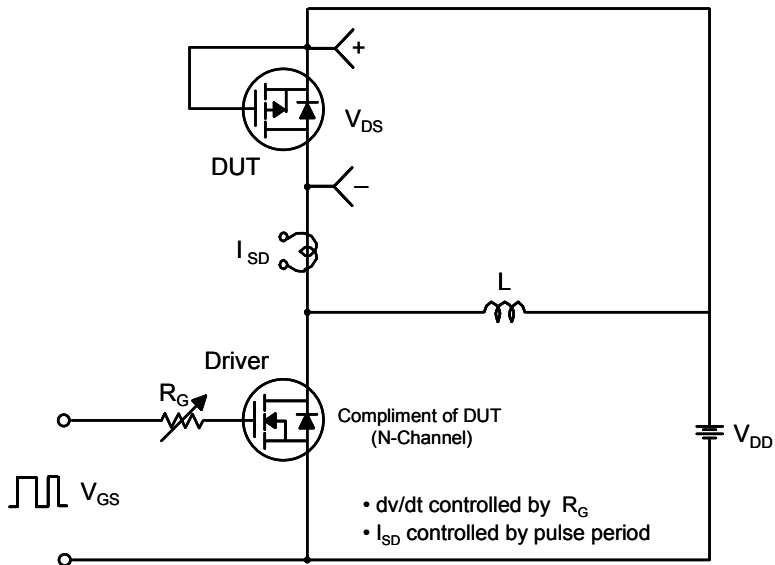
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

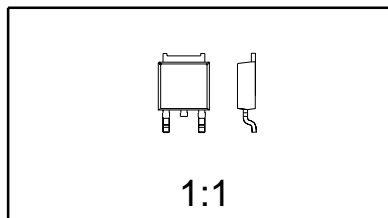
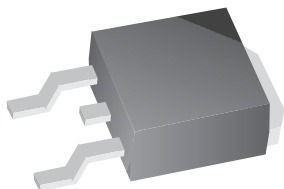


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-252 (DPAK) (FS PKG Code 36)

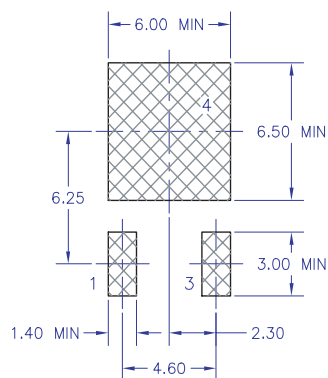
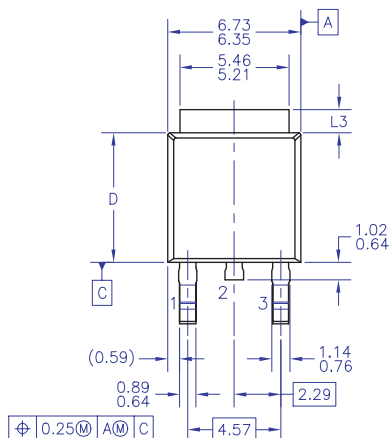


1:1

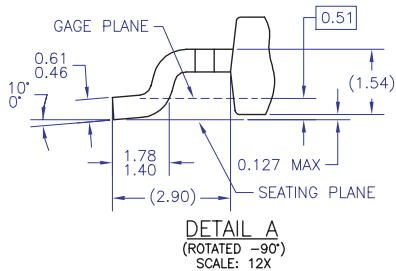
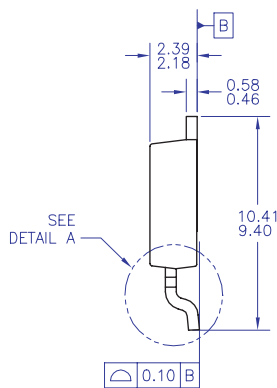
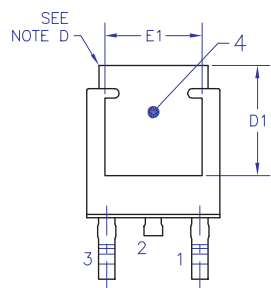
Scale 1:1 on letter size paper

Dimensions shown below are in:
millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative