

FQG4902

250V Dual N & P-Channel MOSFET

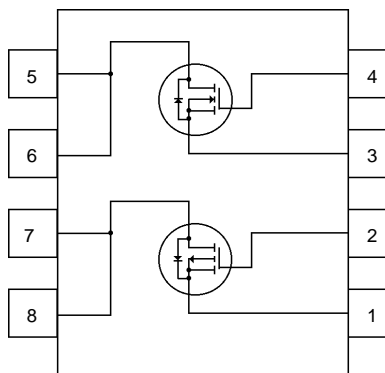
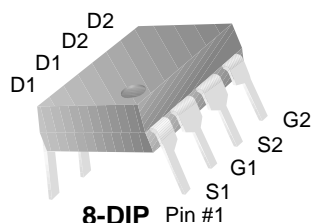
General Description

These dual N and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on half bridge.

Features

- N-Channel 0.54A, 250V, $R_{DS(on)} = 2.0 \Omega @ V_{GS} = 10 V$
P-Channel -0.54A, -250V, $R_{DS(on)} = 2.0 \Omega @ V_{GS} = -10 V$
- Low gate charge (typical N-Channel 6.0 nC)
(typical P-Channel 12.0 nC)
- Fast switching
- Improved dv/dt capability



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V _{DSS}	Drain-Source Voltage	250	-250	V
I _D	Drain Current - Continuous (T _A = 25°C) - Continuous (T _A = 100°C)	0.54	-0.54	A
		0.34	-0.34	A
I _{DM}	Drain Current - Pulsed (Note 1)	4.32	-4.32	A
V _{GSS}	Gate-Source Voltage	± 30		V
dv/dt	Peak Diode Recovery dv/dt (Note 2)	5.5	-5.5	V/ns
P _D	Power Dissipation (T _A = 25°C) - Derate above 25°C	1.4		W
		0.011		W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150		°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 5a)	--	90	°C/W

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	250	--	--	V
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-250	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	N-Ch	--	0.24	--	$\text{V}/^\circ\text{C}$
		$I_D = -250\ \mu\text{A}$, Referenced to 25°C	P-Ch	--	-0.2	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	N-Ch	--	--	10	μA
		$V_{DS} = 200\text{ V}, T_A = 125^\circ\text{C}$		--	--	100	μA
		$V_{DS} = -250\text{ V}, V_{GS} = 0\text{ V}$	P-Ch	--	--	-10	μA
		$V_{DS} = -200\text{ V}, T_A = 125^\circ\text{C}$		--	--	-100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	All	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	All	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	2.0	--	4.0	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.27\text{ A}$	N-Ch	--	1.1	2.0	Ω
		$V_{GS} = -10\text{ V}, I_D = -0.27\text{ A}$	P-Ch	--	1.5	2.0	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 0.27\text{ A}$	N-Ch	--	1.3	--	S
		$V_{DS} = -40\text{ V}, I_D = -0.27\text{ A}$	P-Ch	--	1.1	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	N-Channel $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch	--	195	250	pF
			P-Ch	--	345	445	pF
C_{oss}	Output Capacitance	P-Channel $V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch	--	40	55	pF
			P-Ch	--	65	85	pF
C_{riss}	Reverse Transfer Capacitance	N-Channel $V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch	--	7	9.5	pF
			P-Ch	--	11	14.5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD} = 125\text{ V}, I_D = 0.54\text{ A},$ $R_G = 25\ \Omega$	N-Ch	--	5.5	20	ns
			P-Ch	--	8.0	25	ns
t_r	Turn-On Rise Time	P-Channel $V_{DD} = -125\text{ V}, I_D = -0.54\text{ A},$ $R_G = 25\ \Omega$	N-Ch	--	17	45	ns
			P-Ch	--	19	50	ns
$t_{d(off)}$	Turn-Off Delay Time	N-Channel $V_{DD} = 125\text{ V}, I_D = 0.54\text{ A},$ $R_G = 25\ \Omega$	N-Ch	--	29	70	ns
			P-Ch	--	44	100	ns
t_f	Turn-Off Fall Time	P-Channel $V_{DD} = -125\text{ V}, I_D = -0.54\text{ A},$ $R_G = 25\ \Omega$	N-Ch	--	23	55	ns
			P-Ch	--	33	75	ns
Q_g	Total Gate Charge	N-Channel $V_{DS} = 200\text{ V}, I_D = 0.54\text{ A},$ $V_{GS} = 10\text{ V}$	N-Ch	--	6.0	7.8	nC
			P-Ch	--	12.0	15.6	nC
Q_{gs}	Gate-Source Charge	P-Channel $V_{DS} = -200\text{ V}, I_D = -0.54\text{ A},$ $V_{GS} = -10\text{ V}$	N-Ch	--	1.1	--	nC
			P-Ch	--	2.2	--	nC
Q_{gd}	Gate-Drain Charge	N-Channel $V_{DS} = 200\text{ V}, I_D = 0.54\text{ A},$ $V_{GS} = 10\text{ V}$	N-Ch	--	2.7	--	nC
			P-Ch	--	5.3	--	nC

Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch	--	--	0.54	A
			P-Ch	--	--	-0.54	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		N-Ch	--	--	4.32	A
			P-Ch	--	--	-4.32	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.54\text{ A}$	N-Ch	--	--	1.5	V
		$V_{GS} = 0\text{ V}, I_S = -0.54\text{ A}$	P-Ch	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 0.54\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 3)	N-Ch	--	90	--	ns
Q_{rr}	Reverse Recovery Charge			--	189	--	nC
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -0.54\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 3)	P-Ch	--	77	--	ns
Q_{rr}	Reverse Recovery Charge			--	210	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{SD} \leq 0.54\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
3. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance. $R_{\theta CA}$ is determined by the user's board design
Maximum $R_{\theta JA}$ using the different board layouts on 3"x4.5" FR-4 PCB in a still air environment :
 - a. $90^\circ\text{C}/\text{W}$ when mounted without any pad copper
 - b. $62.5^\circ\text{C}/\text{W}$ when mounted on a 4.5 in^2 pad of 2oz copper. In such an environment, the power dissipation can be enhanced up to 2W

Typical Characteristics : N-Channel

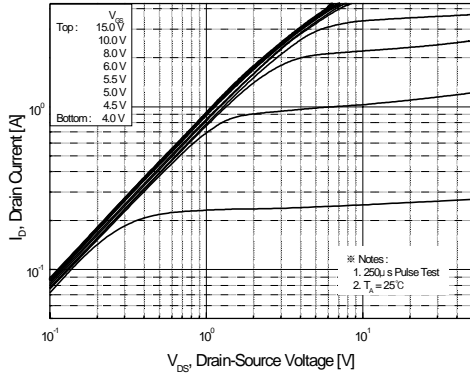


Figure 1. On-Region Characteristics

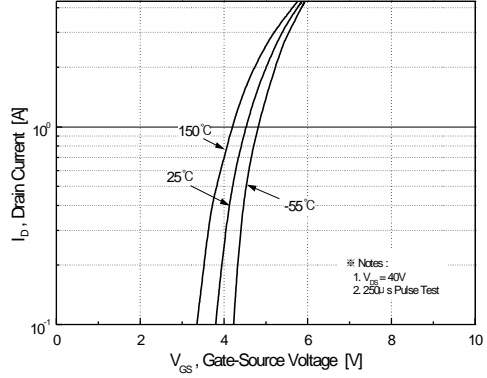


Figure 2. Transfer Characteristics

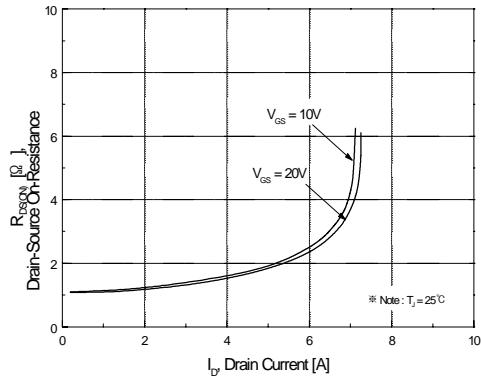


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

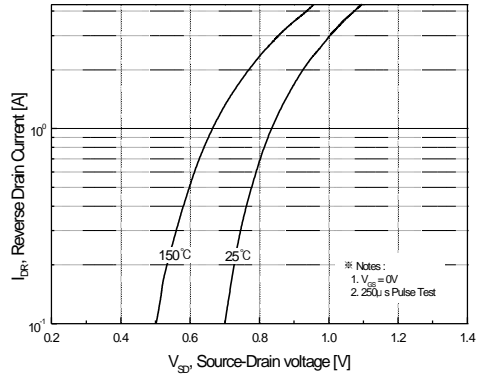


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

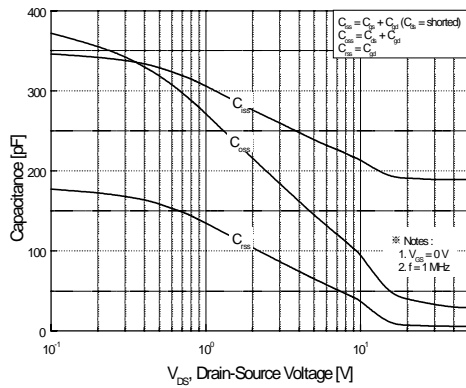


Figure 5. Capacitance Characteristics

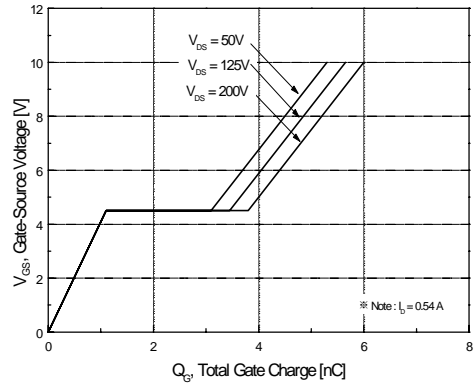


Figure 6. Gate Charge Characteristics

Typical Characteristics : N-Channel (Continued)

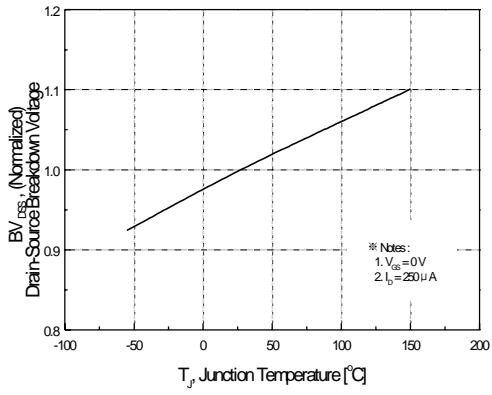


Figure 7. Breakdown Voltage Variation vs. Temperature

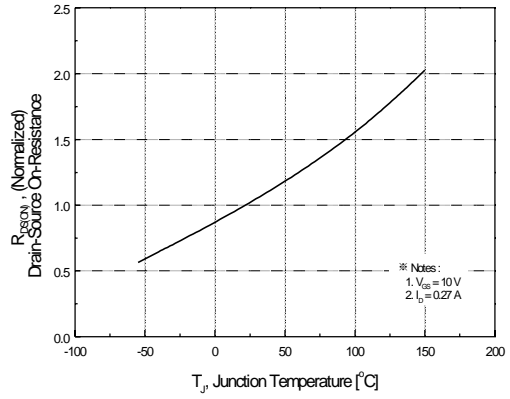


Figure 8. On-Resistance Variation vs. Temperature

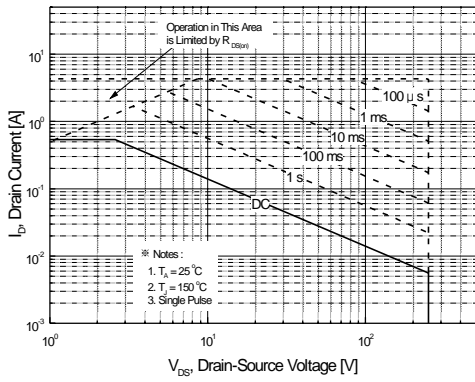


Figure 9. Maximum Safe Operating Area

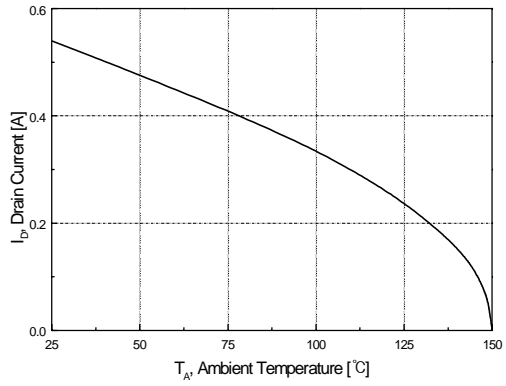


Figure 10. Maximum Drain Current vs. Ambient Temperature

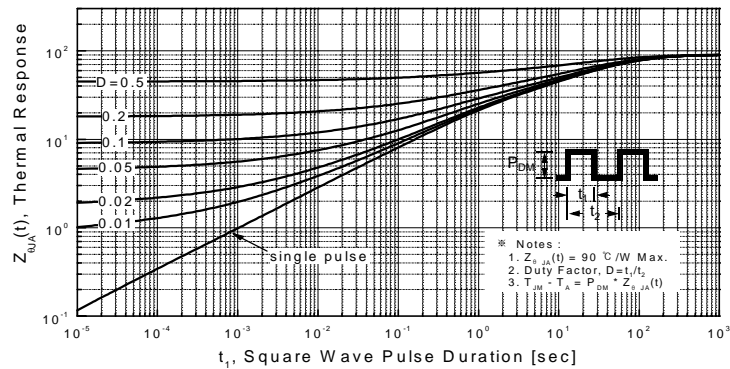


Figure 11. Transient Thermal Response Curve

Typical Characteristics : P-Channel

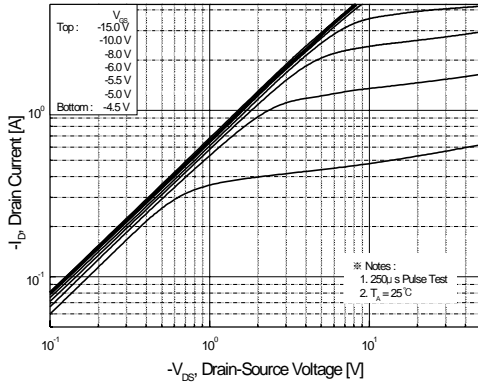


Figure 1. On-Region Characteristics

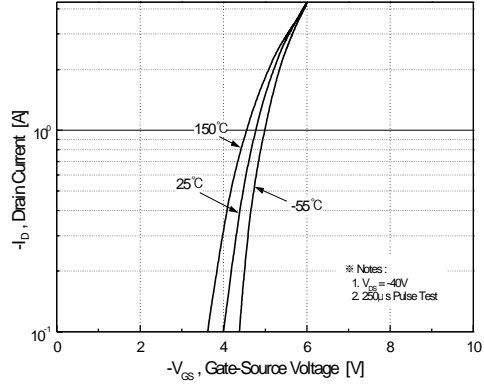


Figure 2. Transfer Characteristics

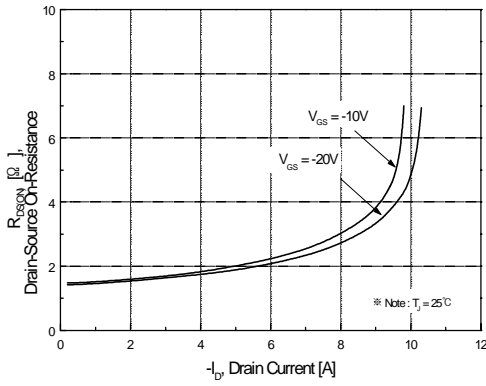


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

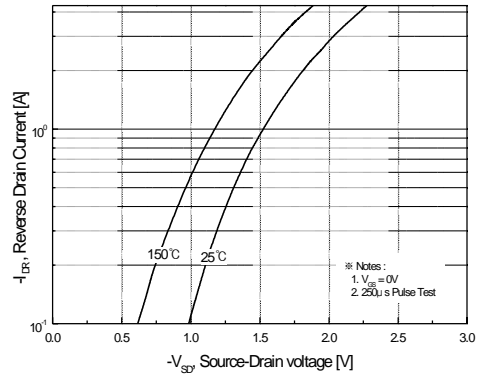


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

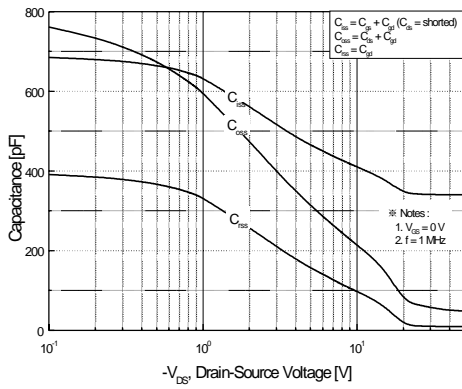


Figure 5. Capacitance Characteristics

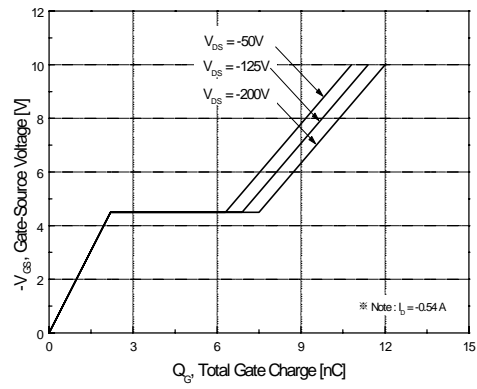


Figure 6. Gate Charge Characteristics

Typical Characteristics : P-Channel (Continued)

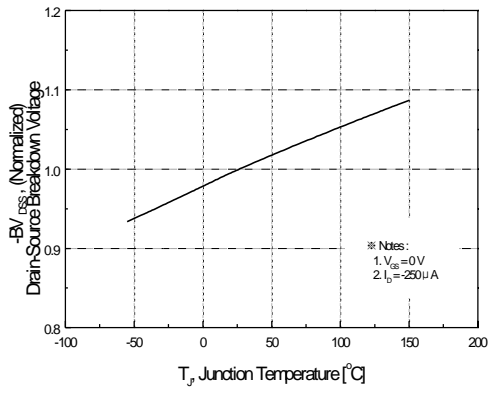


Figure 7. Breakdown Voltage Variation vs. Temperature

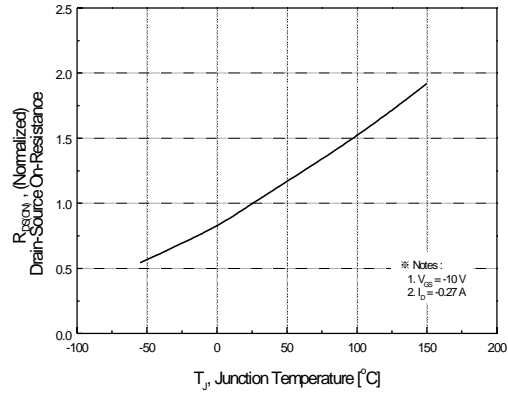


Figure 8. On-Resistance Variation vs. Temperature

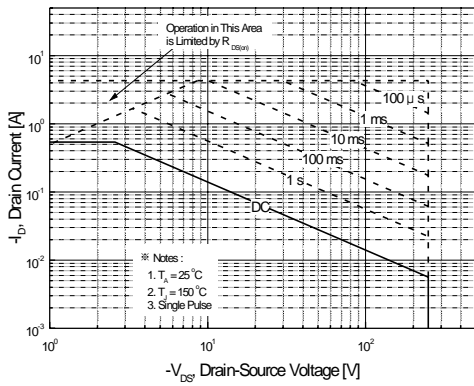


Figure 9. Maximum Safe Operating Area

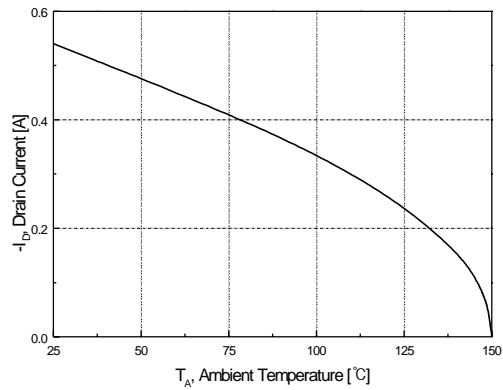


Figure 10. Maximum Drain Current vs. Ambient Temperature

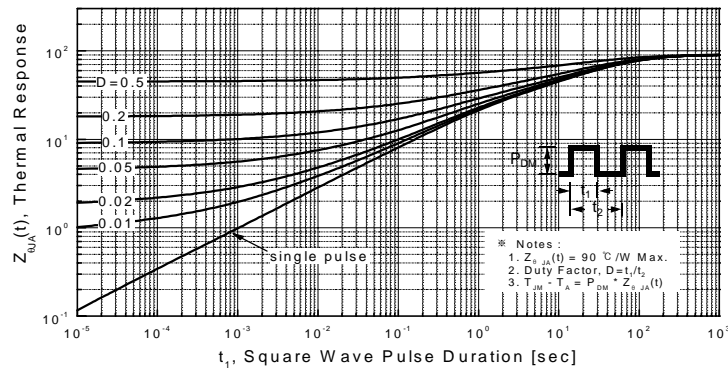
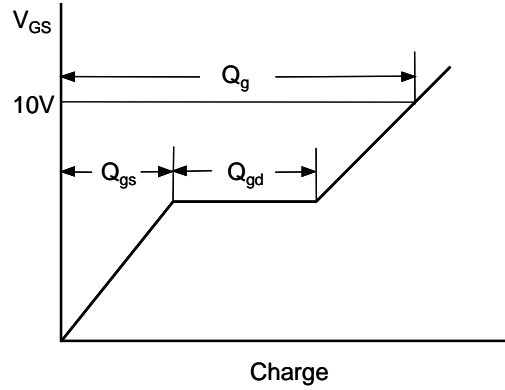
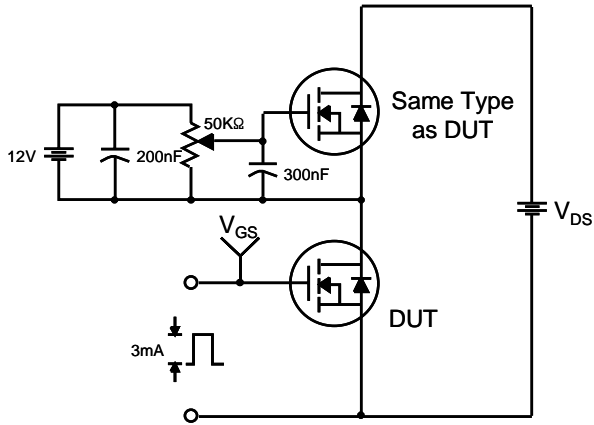
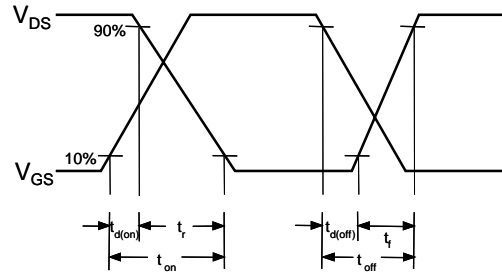
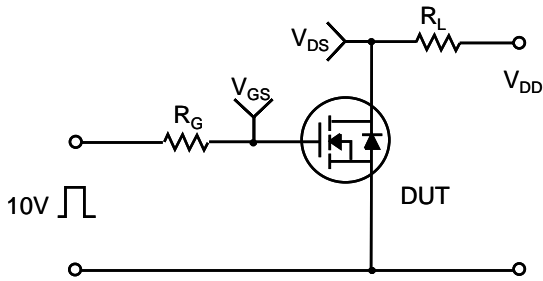


Figure 11. Transient Thermal Response Curve

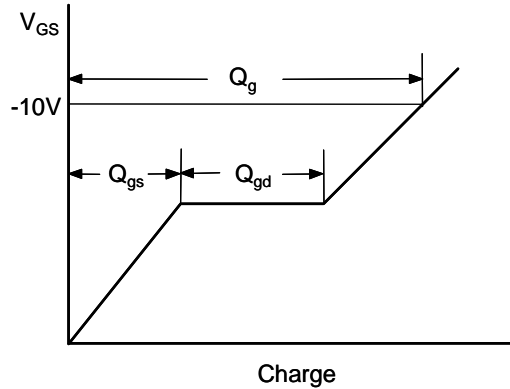
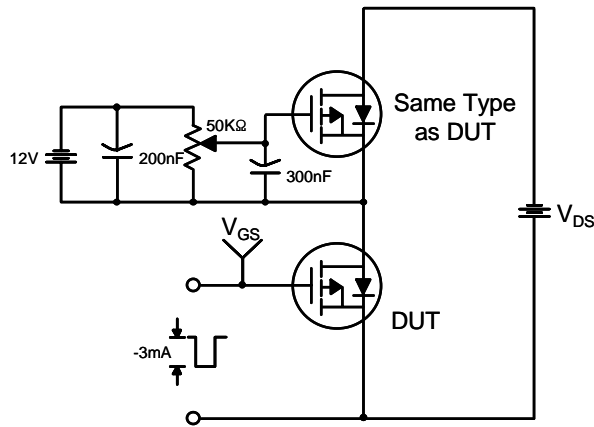
Gate Charge Test Circuit & Waveform (N-Channel)



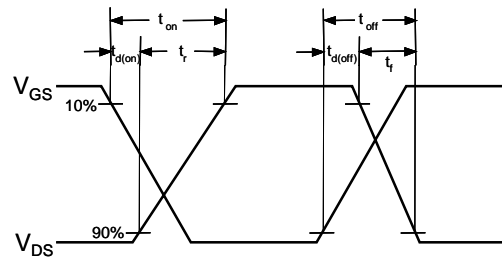
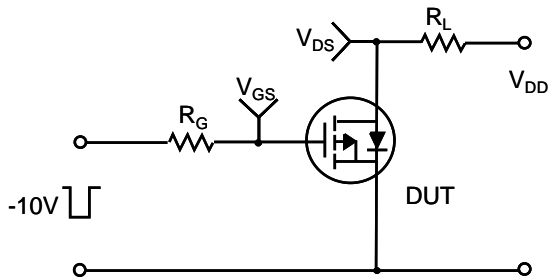
Resistive Switching Test Circuit & Waveforms (N-Channel)



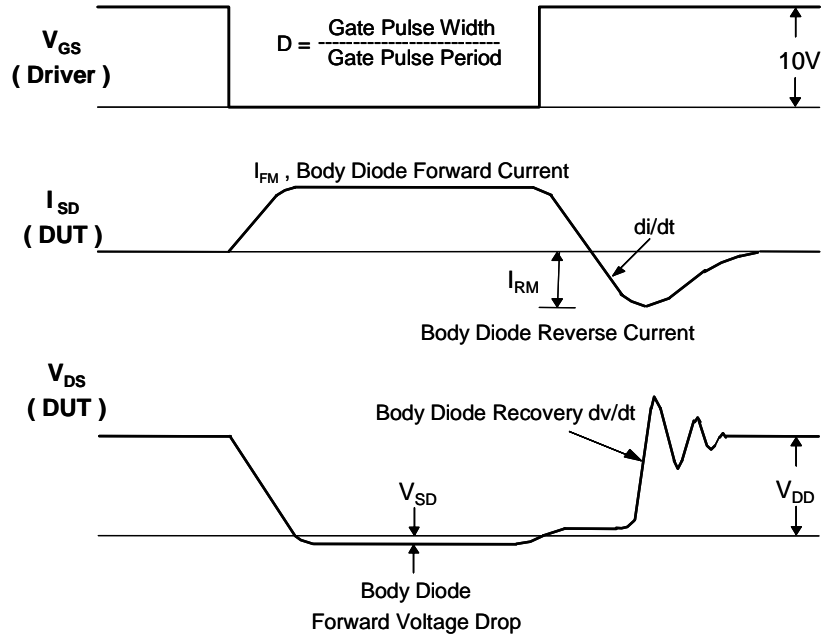
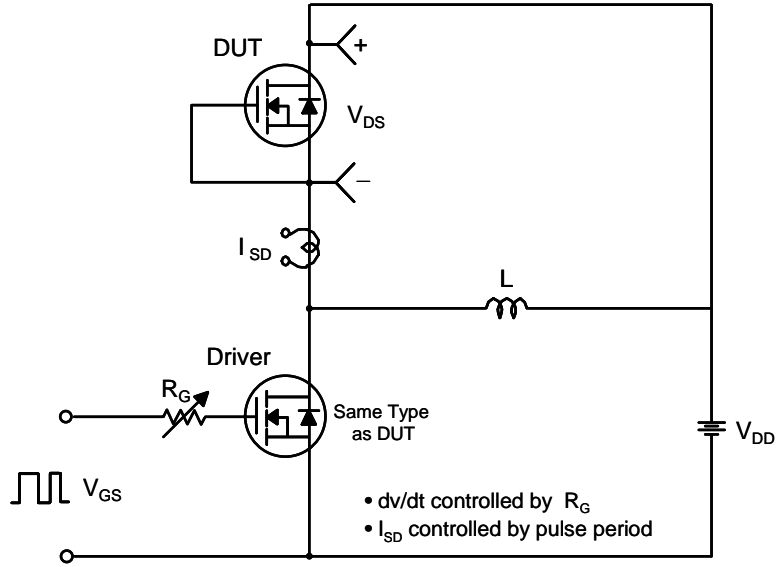
Gate Charge Test Circuit & Waveform (P-Channel)



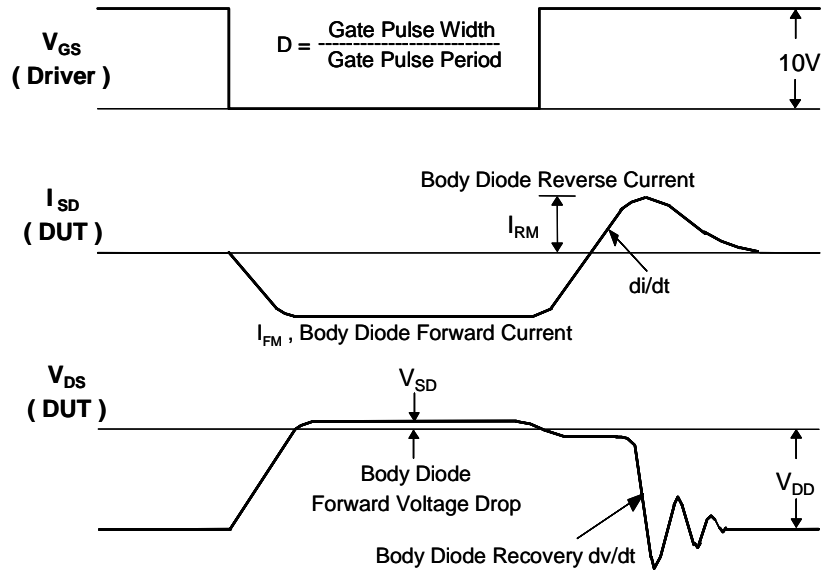
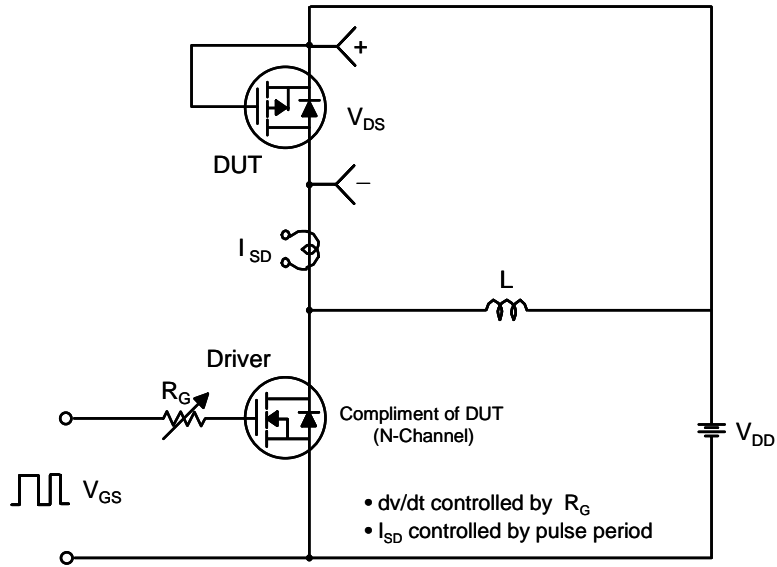
Resistive Switching Test Circuit & Waveforms (P-Channel)



Peak Diode Recovery dv/dt Test Circuit & Waveforms (N-Channel)

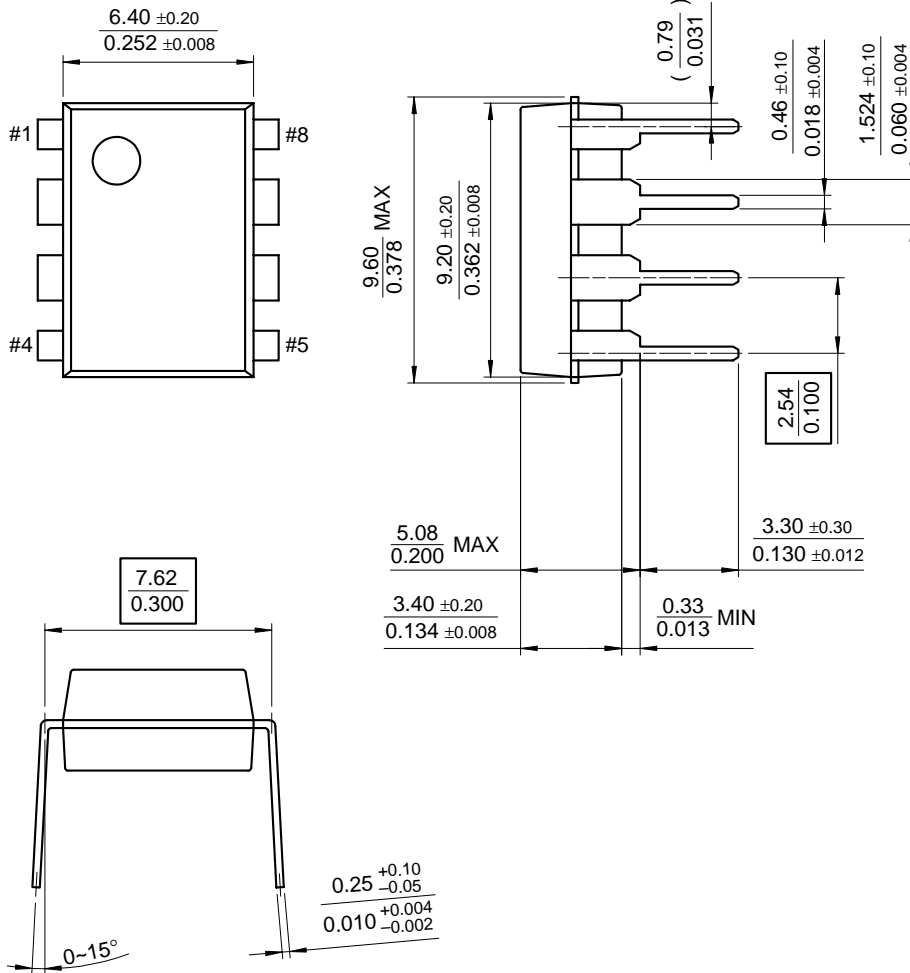


Peak Diode Recovery dv/dt Test Circuit & Waveforms (P-Channel)



Package Dimensions

8-DIP



Dimensions in Millimeters

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.