



# FQB27N25TM\_F085/FQI27N25TU\_F085

## N-Channel MOSFET

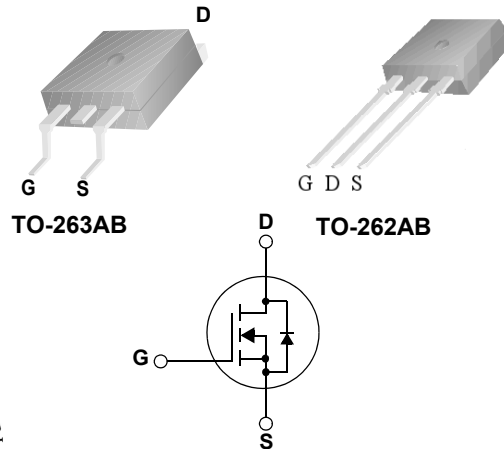
250 V, 25.5 A, 131 mΩ

### Features

- Typ  $R_{DS(on)}$  = 108mΩ at  $V_{GS}$  = 10V,  $I_D$  = 25.5A
- Typ  $Q_{g(tot)}$  = 45nC at  $V_{GS}$  = 10V,  $I_D$  = 27A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

### Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



For current package drawing, please refer to the Fairchild website at [www.fairchildsemi.com/packaging](http://www.fairchildsemi.com/packaging)

### MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DSS}$	Drain to Source Voltage	250	V
$V_{GS}$	Gate to Source Voltage	±30	V
$I_D$	Drain Current - Continuous ( $V_{GS}=10$ ) (Note 1)	$T_C = 25^\circ\text{C}$	25.5
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$	See Figure 4
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	972	mJ
$P_D$	Power Dissipation	417	W
	Derate above $25^\circ\text{C}$	3.3	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 150	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB27N25TM	FQB27N25TM_F085	TO-263AB	330mm	24mm	800 units
FQI27N25TU	FQI27N25TU_F085	TO-262AB	Tube	N/A	50 units

#### Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 4.67\text{mH}$ ,  $I_{AS} = 20.4\text{A}$ ,  $V_{DD} = 100\text{V}$  during inductor charging and  $V_{DD} = 0\text{V}$  during time in avalanche.
- 3:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

FQB27N25TM\_F085/FQI27N25TU\_F085 N-Channel MOSFET

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	250	-	-	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 250\text{V}, T_J = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}(\text{Note } 4)$	-	-	250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 30\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	4.1	5.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 25.5\text{A}, T_J = 25^\circ\text{C}$	-	108	131	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 150^\circ\text{C}(\text{Note } 4)$	-	265	310	$\text{m}\Omega$

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	1800	-	pF
$C_{oss}$	Output Capacitance		-	350	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	45	-	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$	-	0.82	-	$\Omega$
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0 \text{ to } 10\text{V}$	-	45	49	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2\text{V}$				
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 125\text{V}, I_D = 27\text{A}$	-	12	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	23	-	nC

**Switching Characteristics**

$t_{on}$	Turn-On Time	$V_{DD} = 125\text{V}, I_D = 27\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 25\Omega$	-	-	196	ns
$t_{d(on)}$	Turn-On Delay		-	36	-	ns
$t_r$	Rise Time		-	122	-	ns
$t_{d(off)}$	Turn-Off Delay		-	81	-	ns
$t_f$	Fall Time		-	60	-	ns
$t_{off}$	Turn-Off Time		-	-	164	ns

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 25.5\text{A}, V_{GS} = 0\text{V}$	-	-	1.5	V
		$I_{SD} = 12.75\text{A}, V_{GS} = 0\text{V}$	-	-	1.25	V
$t_{rr}$	Reverse--Recovery Time	$I_F = 27\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	205	238	ns
$Q_{rr}$	Reverse--Recovery Charge	$V_{DD} = 200\text{V}$	-	1.8	2.3	nC

**Notes:**

4: The maximum value is specified by design at  $T_J = 150^\circ\text{C}$ . Product is not tested to this condition in production.

### Typical Characteristics

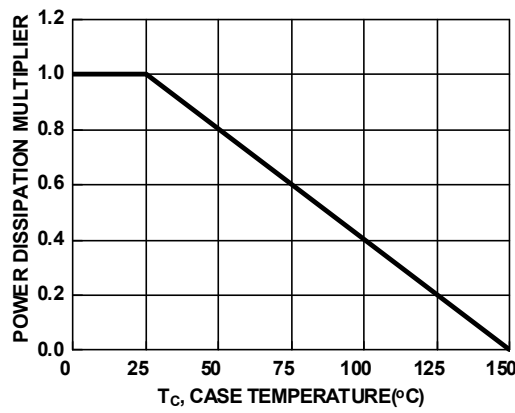


Figure 1. Normalized Power Dissipation vs. Case Temperature

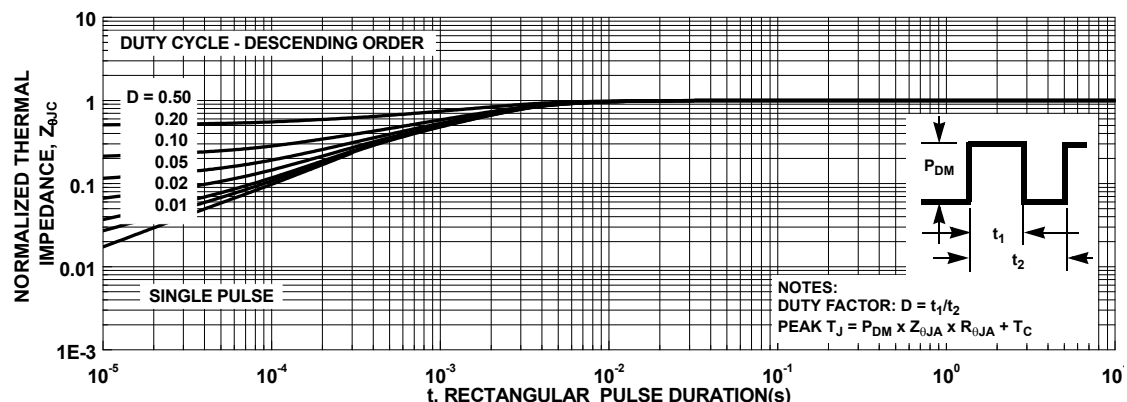


Figure 2. Normalized Maximum Transient Thermal Impedance

### Typical Characteristics

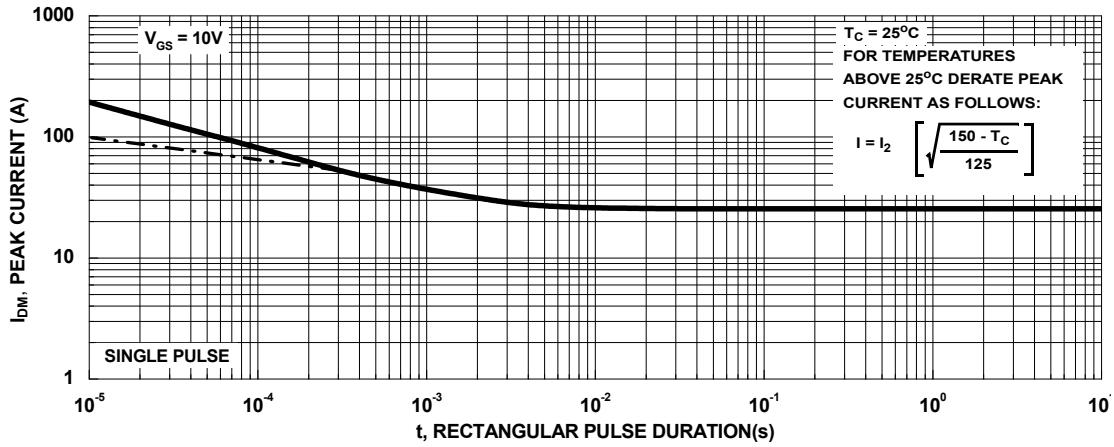


Figure 3. Peak Current Capability

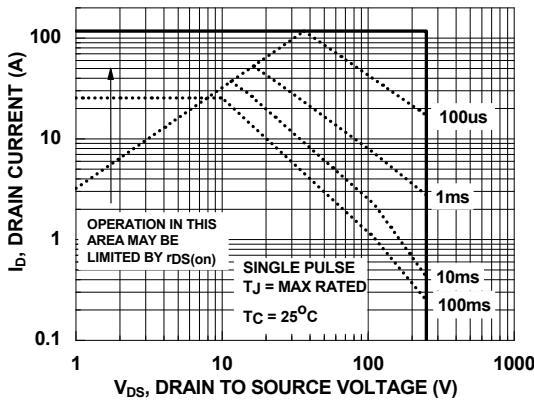
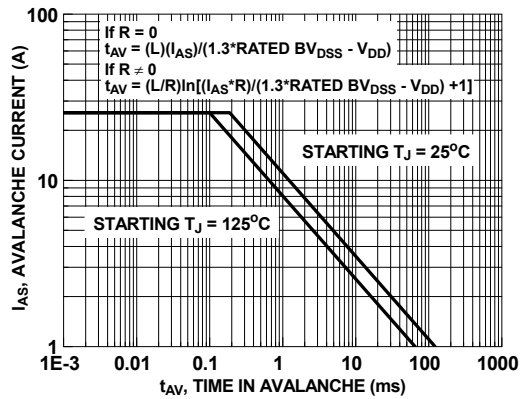


Figure 4. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 5. Unclamped Inductive Switching Capability

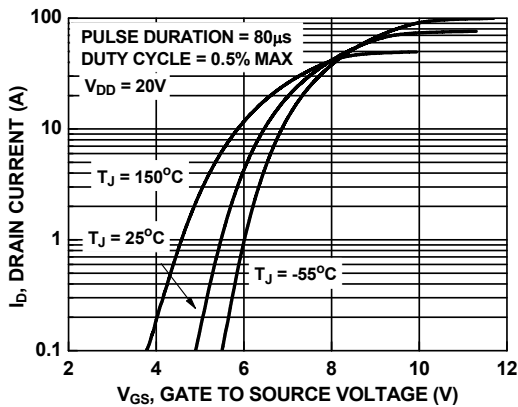


Figure 6. Transfer Characteristics

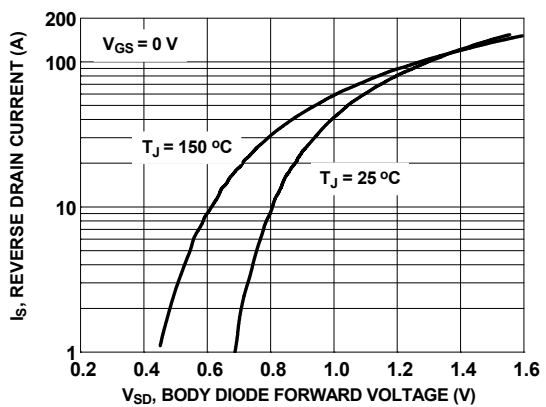


Figure 7. Forward Diode Characteristics

### Typical Characteristics

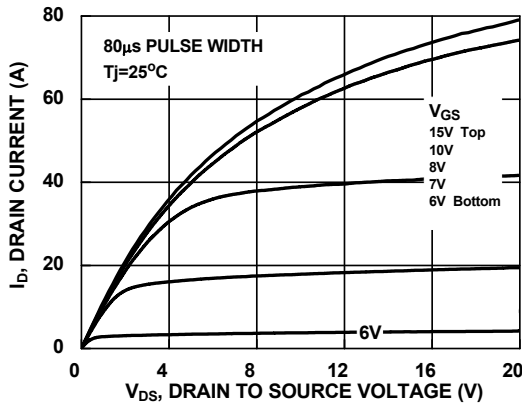


Figure 8. Saturation Characteristics

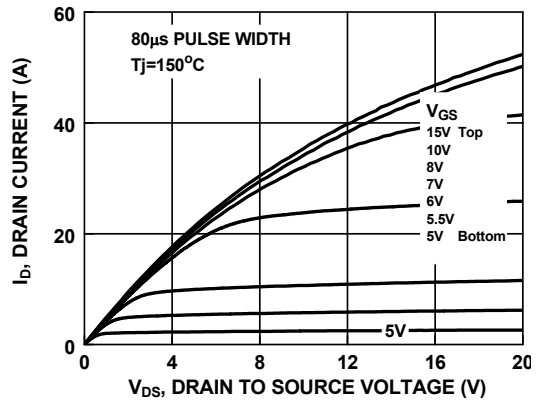


Figure 9. Saturation Characteristics

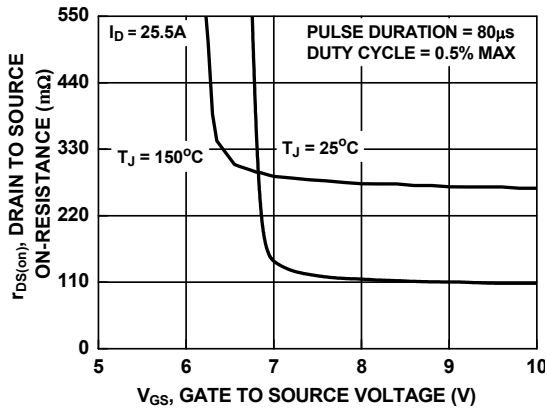


Figure 10.  $R_{DS(on)}$  vs. Gate Voltage

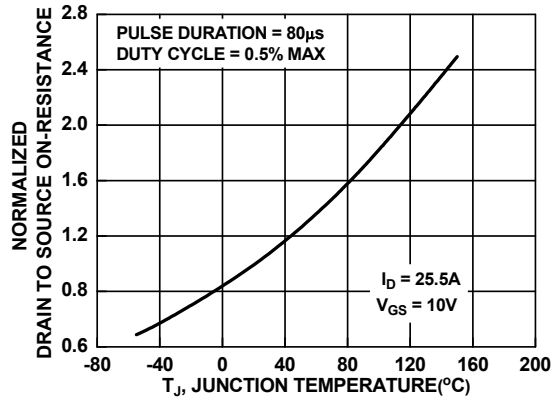


Figure 11. Normalized  $R_{DS(on)}$  vs. Junction Temperature

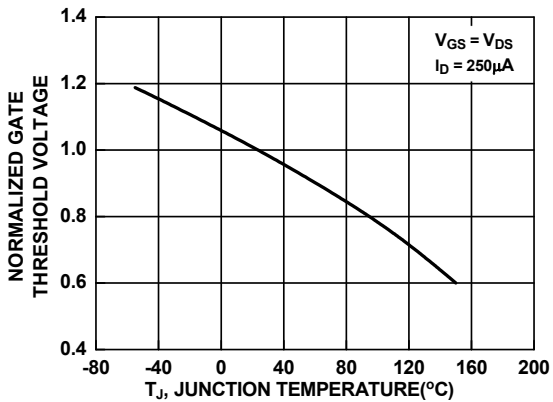


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

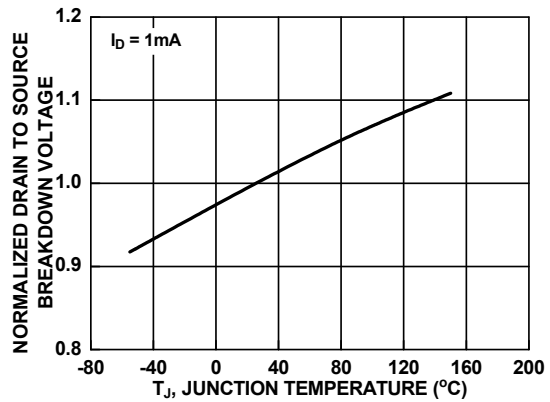


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

## Typical Characteristics

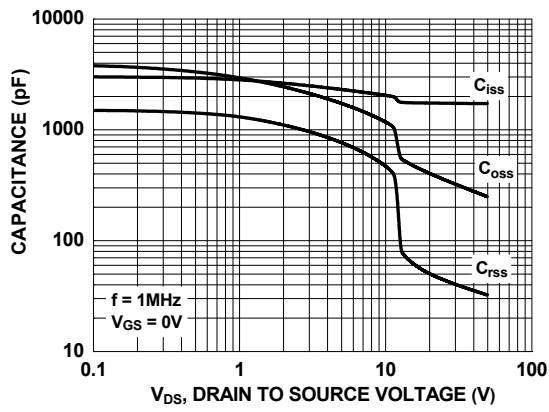


Figure 14. Capacitance vs. Drain to Source Voltage

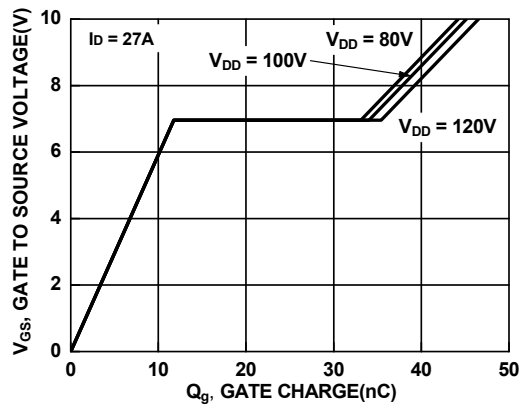







Figure 15. Gate Charge vs. Gate to Source Voltage



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