

FQN1N50C

N-Channel QFET MOSFET

500 V, 0.38 A, 6 Ω

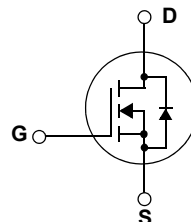
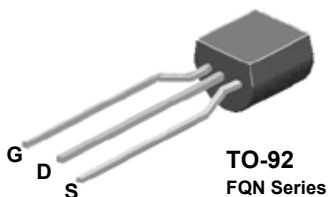


Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 0.38 A, 500 V, $R_{DS(on)} = 6 \Omega$ (Max) @ $V_{GS} = 10 \text{ V}$, $I_D = 0.19 \text{ A}$
- Low Gate Charge (Typ. 4.9 nC)
- Low Crss (Typ. 4.1 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings

Symbol	Parameter	FQN1N50C	Unit
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	0.38
		- Continuous ($T_C = 100^\circ\text{C}$)	0.24
I_{DM}	Drain Current - Pulsed (Note 1)	3.04	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	44.4	mJ
I_{AR}	Avalanche Current (Note 1)	0.38	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.21	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)	0.89	W
	Power Dissipation ($T_L = 25^\circ\text{C}$)	2.08	W
	- Derate above 25°C	0.017	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead (Note 6a)	--	60	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 6b)	--	140	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1N50C	FQN1N50C	TO-92	--	--	2000ea

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	500	--	--	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	--	--	50	μA
		V _{DS} = 400 V, T _C = 125°C	--	--	250	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.19 A	--	4.6	6.0	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 0.19A (Note 4)	--	0.6	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	150	195	pF
C _{oss}	Output Capacitance		--	28	40	pF
C _{rss}	Reverse Transfer Capacitance		--	4.1	--	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 1.0 A, R _G = 25 Ω (Note 4, 5)	--	10	30	ns
t _r	Turn-On Rise Time		--	10	30	ns
t _{d(off)}	Turn-Off Delay Time		--	20	50	ns
t _f	Turn-Off Fall Time		--	15	40	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 1.0 A, V _{GS} = 10 V (Note 4, 5)	--	4.9	6.4	nC
Q _{gs}	Gate-Source Charge		--	0.66	--	nC
Q _{gd}	Gate-Drain Charge		--	2.9	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.38	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	3.04	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.38 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 1.0 A, di _F / dt = 100 A/μs (Note 4)	--	188	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.55	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 80mH, I_{AS} = 1.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 0.38A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature
6. a) Reference point of the R_{θJL} is the drain lead
 b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment
 (R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance. R_{θCA} is determined by the user's board design)

Typical Performance Characteristics

Figure 1. On-Region Characteristics

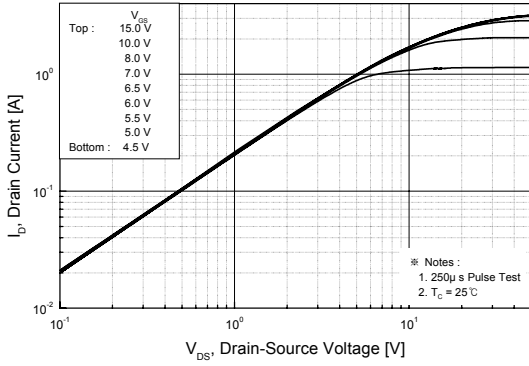


Figure 2. Transfer Characteristics

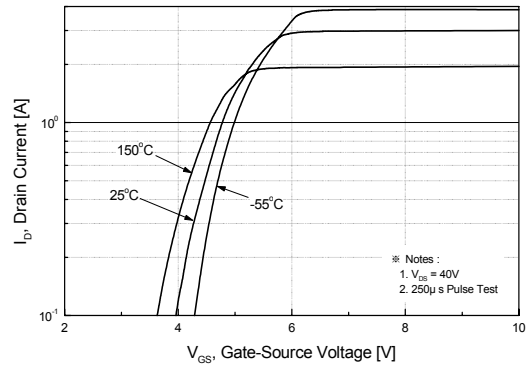


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

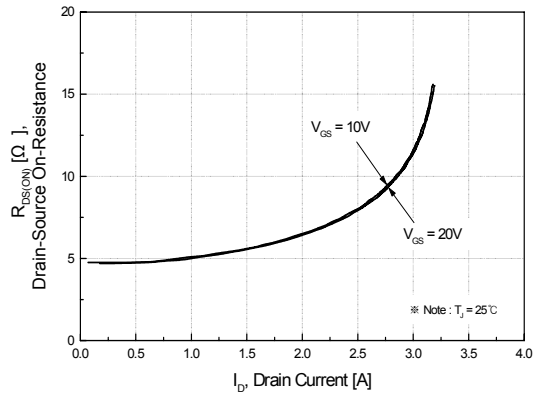


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

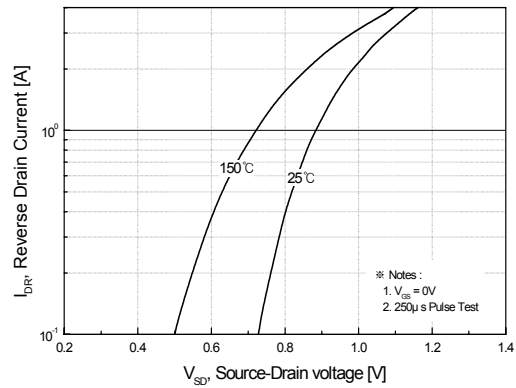


Figure 5. Capacitance Characteristics

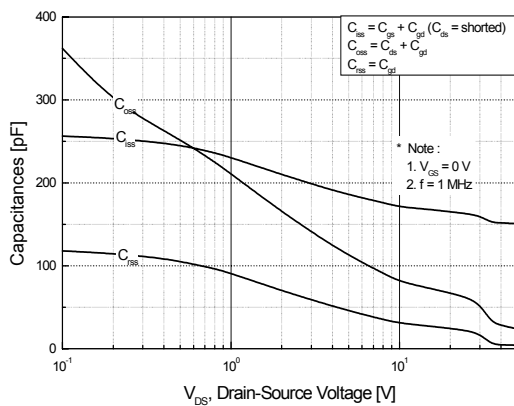
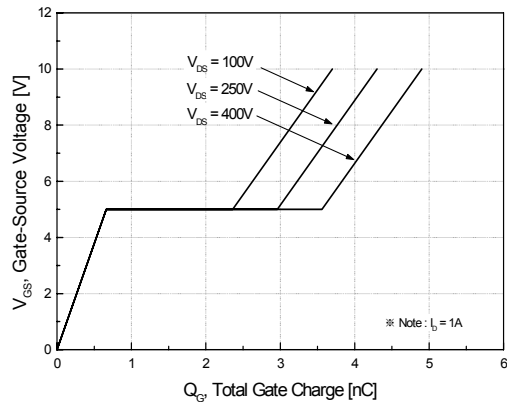


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

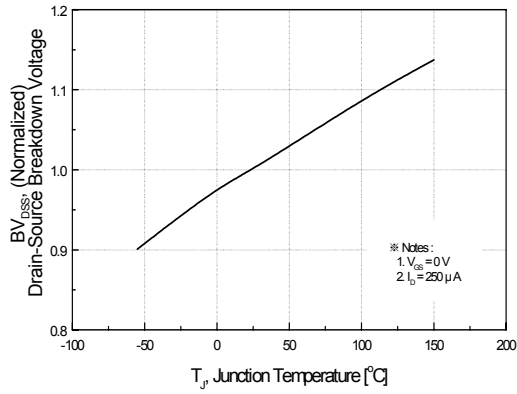


Figure 8. On-Resistance Variation vs. Temperature

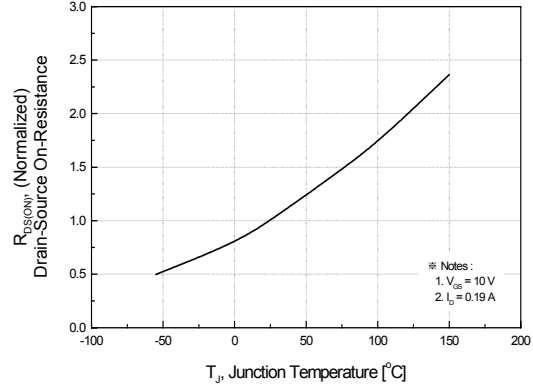


Figure 9. Maximum Safe Operating Area

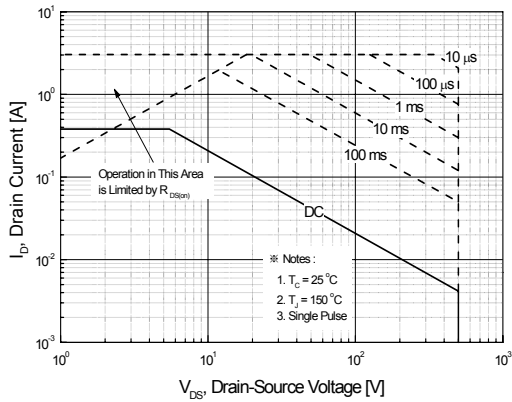


Figure 10. Maximum Drain Current vs. Case Temperature

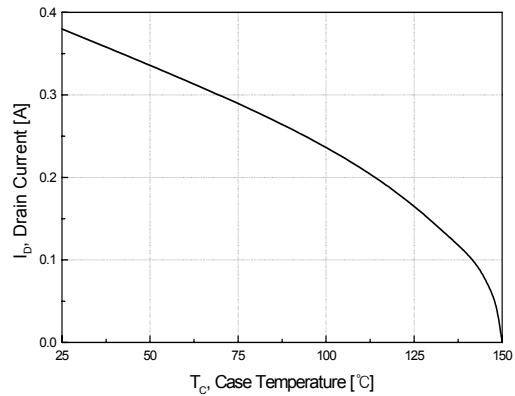
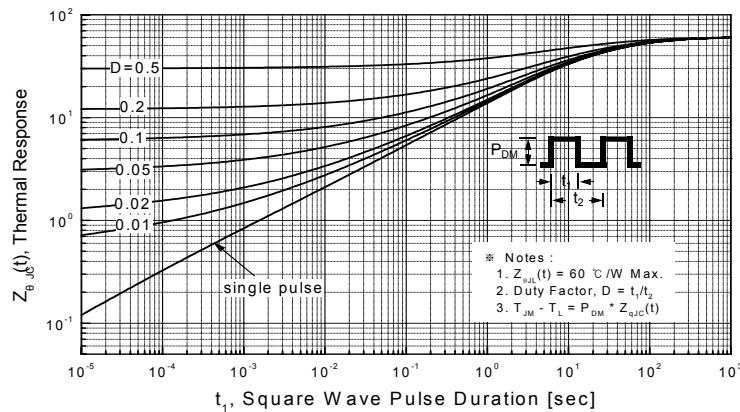
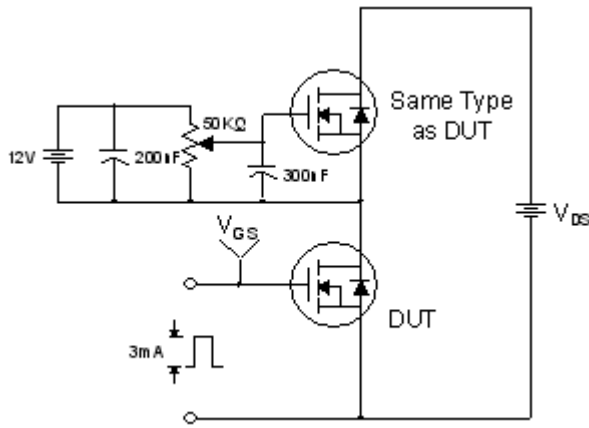


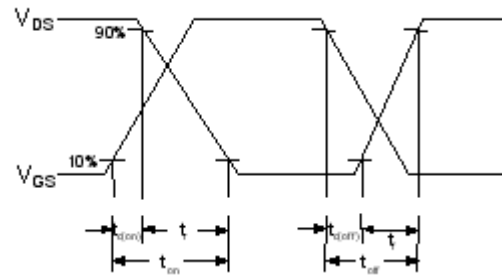
Figure 11. Transient Thermal Response Curve



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

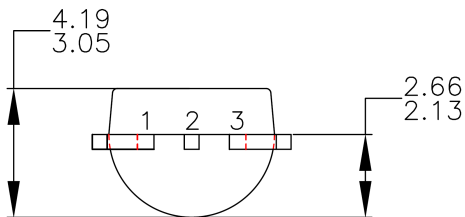
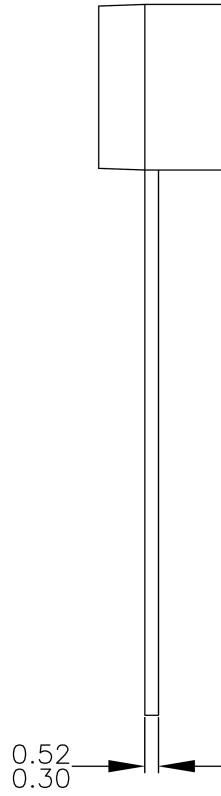
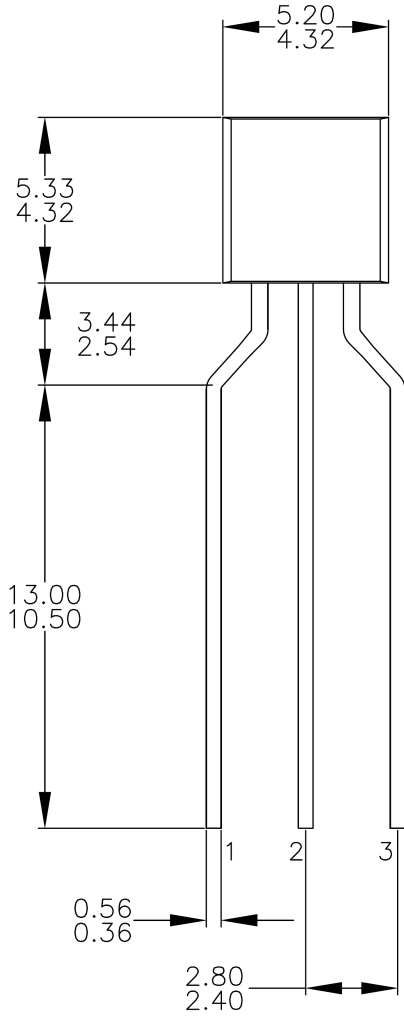


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

- P - BIPOLAR E - EMITTER D - DRAIN
- F - JFET B - BASE S - SOURCE
- M - DMOS C - COLLECTOR G - GATE



- E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03FREV2.

Dimensions in Millimeters



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