FAIRCHILD SEMICONDUCTOR®

March 2013

FQP27P06

P-Channel QFET® MOSFET

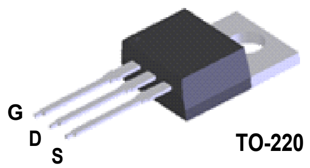
- 60 V, - 27 A, 70 mΩ

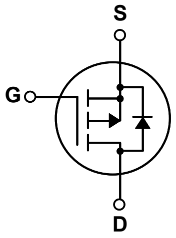
Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- - 27 A, - 60 V, $R_{DS(on)}$ = 70 mΩ (Max.) @ V_{GS} = - 10 V, I_D = - 13.5 A
- Low Gate Charge (Typ. 33 nC)
- Low Crss (Typ. 120 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQP27P06	Unit
V_{DSS}	Drain-Source Voltage		-60	V
I_D	Drain Current	- Continuous (T_C = 25°C)	-27	A
		- Continuous (T_C = 100°C)	-19.1	A
I_{DM}	Drain Current	- Pulsed (Note 1)	-108	A
V_{GSS}	Gate-Source Voltage		± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		560	mJ
I_{AR}	Avalanche Current (Note 1)		-27	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		12	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		-7.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		120	W
		- Derate above 25°C	0.8	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQP27P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.25	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

Elerical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C	--	-0.06	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60 V, V_{GS} = 0 V	--	--	-1	µA
		V_{DS} = -48 V, T_C = 150°C	--	--	-10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -13.5 A	--	0.055	0.07	Ω
g_{FS}	Forward Transconductance	V_{DS} = -30 V, I_D = -13.5 A	--	12.4	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1100	1400	pF
C_{oss}	Output Capacitance		--	510	660	pF
C_{rss}	Reverse Transfer Capacitance		--	120	155	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30 V, I_D = -13.5 A, R_G = 25 Ω (Note 4)	--	18	45	ns
t_r	Turn-On Rise Time		--	185	380	ns
$t_{d(off)}$	Turn-Off Delay Time		--	30	70	ns
t_f	Turn-Off Fall Time		--	90	190	ns
Q_g	Total Gate Charge	V_{DS} = -48 V, I_D = -27 A, V_{GS} = -10 V (Note 4)	--	33	43	nC
Q_{gs}	Gate-Source Charge		--	6.8	--	nC
Q_{gd}	Gate-Drain Charge		--	18	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-27	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-108	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -27 A	--	--	-4.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -27 A, dI_F / dt = 100 A/µs	--	105	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.41	--	µC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 0.9mH, I_{AS} = -27A, V_{DD} = -25V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ -27A, di/dt ≤ 300A/µs, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25°C
4. Essentially independent of operating temperature

Typical Characteristics

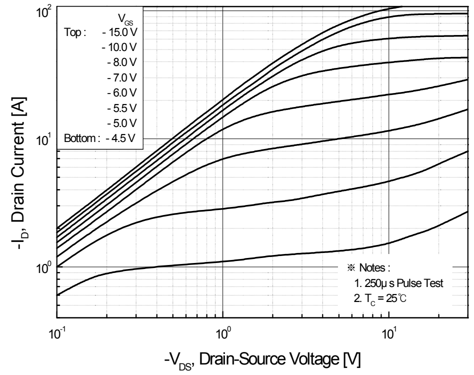


Figure 1. On-Region Characteristics

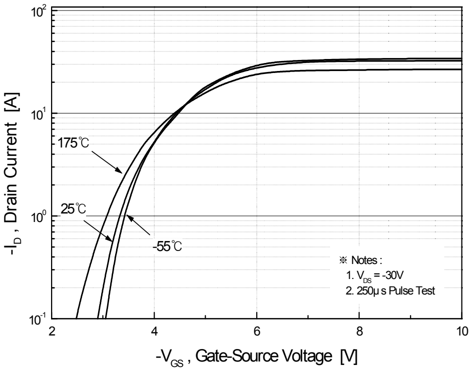


Figure 2. Transfer Characteristics

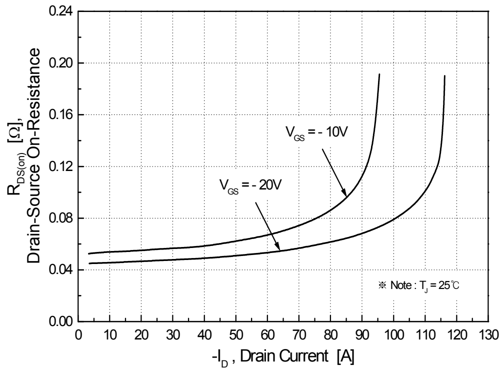


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

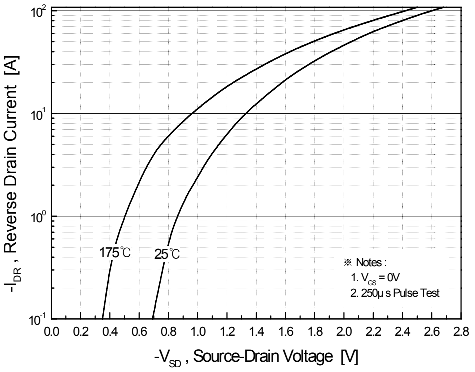


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

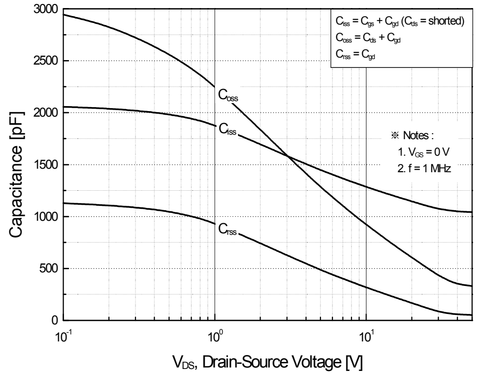


Figure 5. Capacitance Characteristics

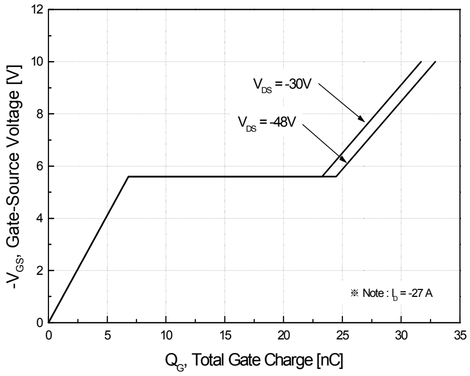


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

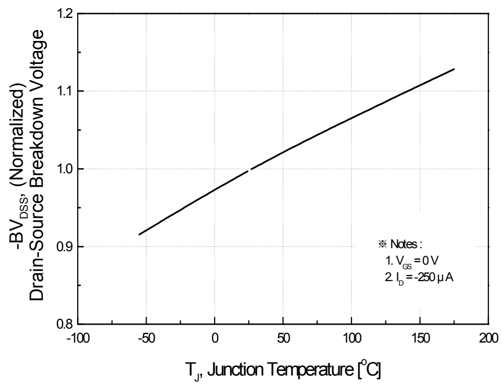


Figure 7. Breakdown Voltage Variation vs. Temperature

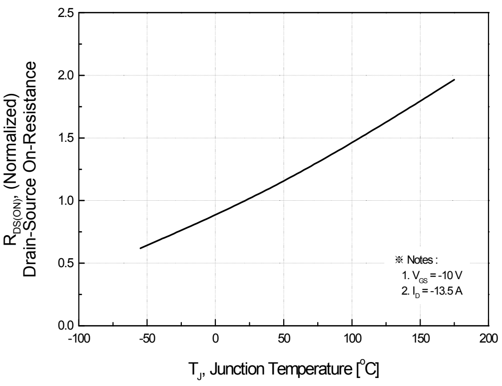


Figure 8. On-Resistance Variation vs. Temperature

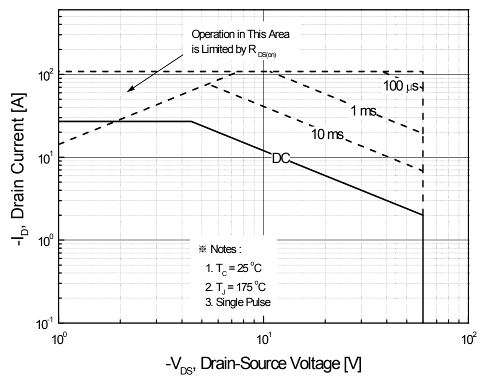


Figure 9. Maximum Safe Operating Area

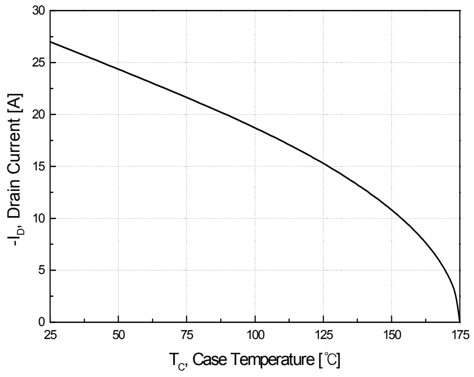


Figure 10. Maximum Drain Current vs. Case Temperature

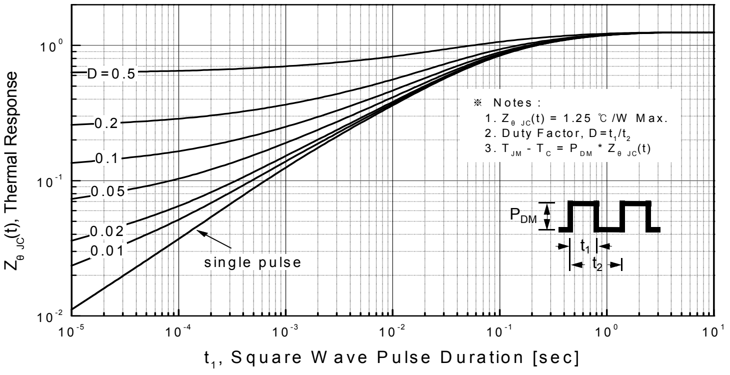
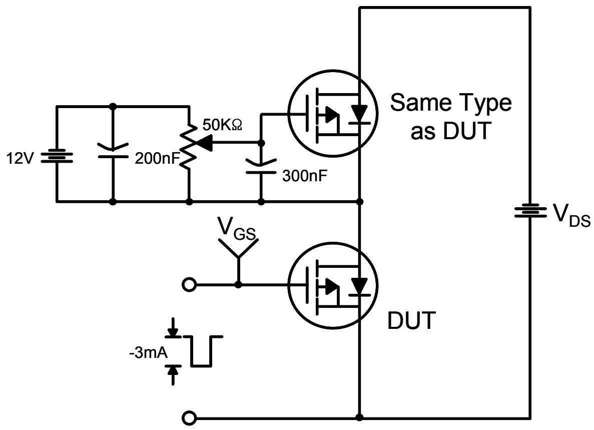
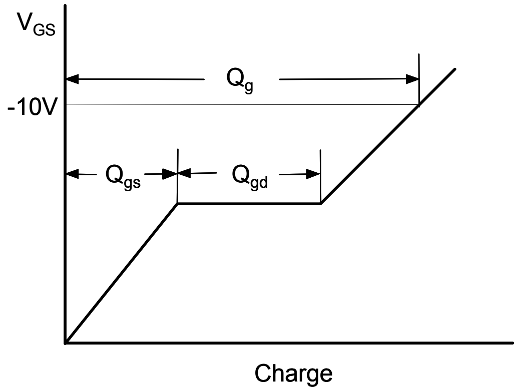


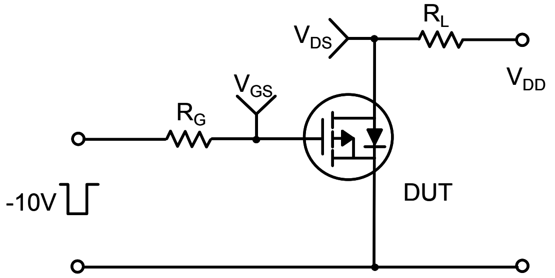
Figure 11. Transient Thermal Response Curve

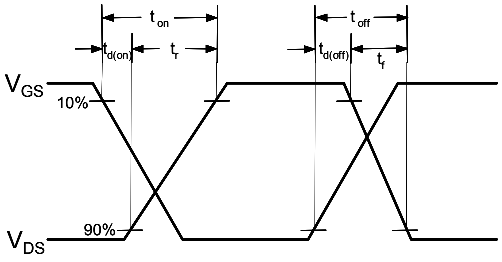
Gate Charge Test Circuit & Waveform



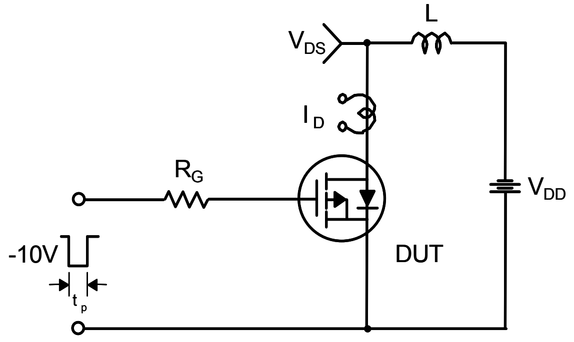


Resistive Switching Test Circuit & Waveforms

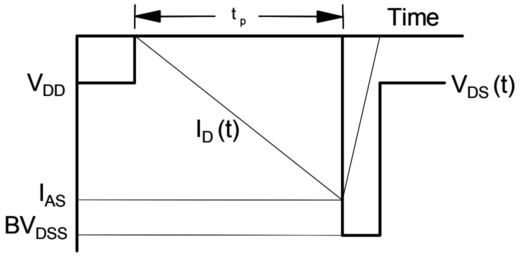




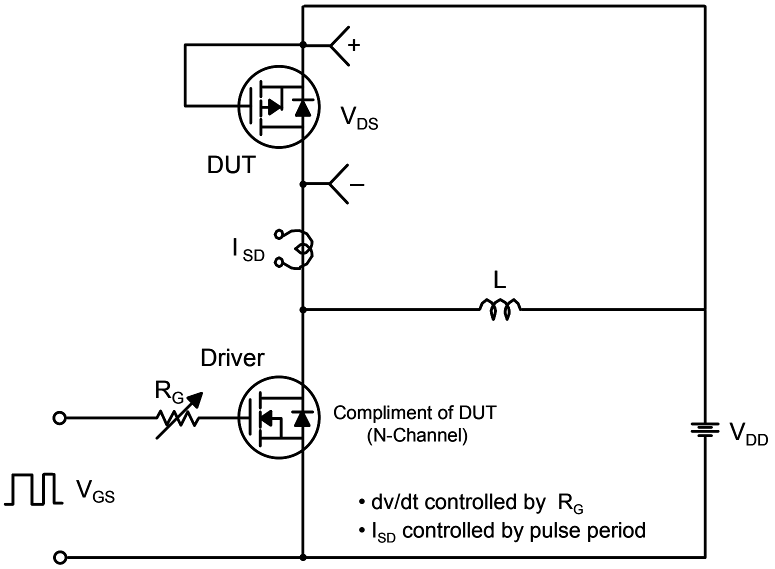
Unclamped Inductive Switching Test Circuit & Waveforms

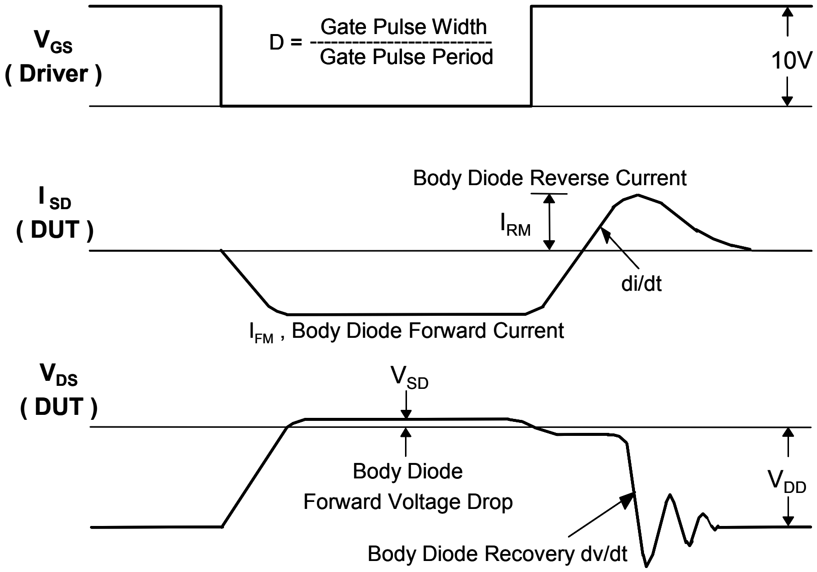


$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



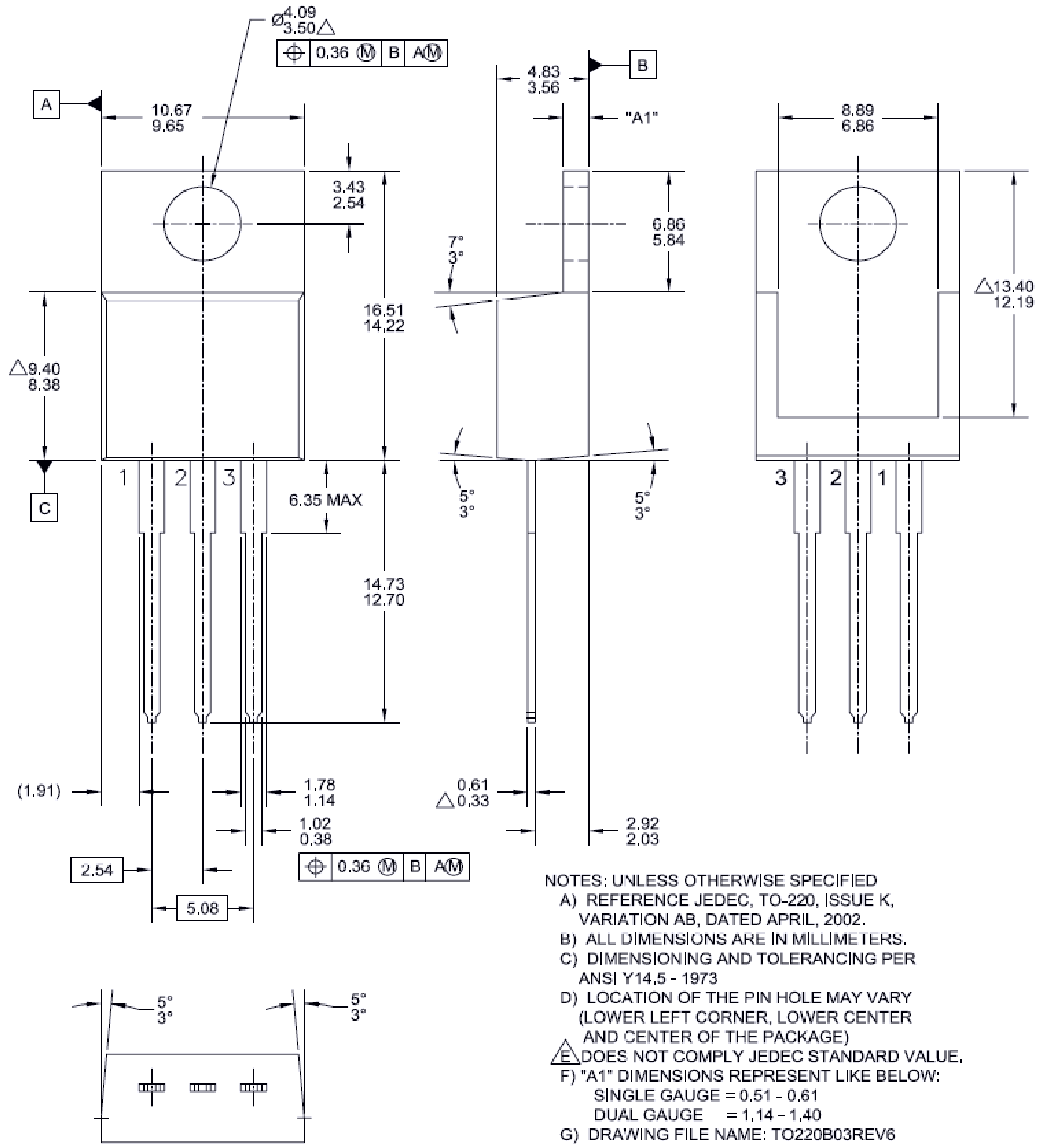
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions

TO-220



NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.14 - 1.40
G) DRAWING FILE NAME: TO220B03REV6

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