

# FQP9N30

## N-Channel QFET<sup>®</sup> MOSFET

300 V, 9.0 A, 450 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 9.0 A, 300 V,  $R_{DS(on)} = 450 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 4.5 \text{ A}$
- Low Gate Charge (Typ. 17 nC)
- Low  $C_{rss}$  (Typ. 16 pF)
- 100% Avalanche Tested

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted.)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	300	V
Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ )	$I_D$	9.0	A
– Continuous ( $T_C = 100^\circ\text{C}$ )		5.7	A
Drain Current – Pulsed (Note 1)	$I_{DM}$	36	A
Gate-Source Voltage	$V_{GSS}$	$\pm 30$	V
Single Pulsed Avalanche Energy (Note 2)	$E_{AS}$	420	mJ
Avalanche Current (Note 1)	$I_{AR}$	9.0	A
Repetitive Avalanche Energy (Note 1)	$E_{AR}$	9.8	mJ
Peak Diode Recovery $dv/dt$ (Note 3)	$dv/dt$	4.5	V/ns
Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	98	W
– Derate above $25^\circ\text{C}$		0.78	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	$T_L$	300	$^\circ\text{C}$

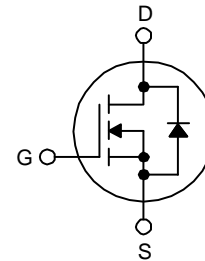
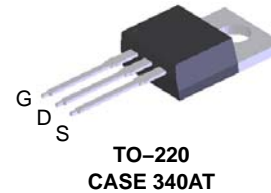
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 8.64 \text{ mH}$ ,  $I_{AS} = 9.0 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $R_G = 25 \Omega$  starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 9.0 \text{ A}$ ,  $di/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .



ON Semiconductor<sup>®</sup>

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### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FQP9N30

## THERMAL CHARACTERISTICS

Symbol	Parameter	FQP9N30	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP9N30	FQP9N30	TO-220	Tube	N/A	N/A	50 units

## ELECTRICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	300	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.28	-	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 300\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 240\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$	-	0.35	0.45	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 4.5\text{ A}$	-	4.9	-	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	570	740	pF
$C_{oss}$	Output Capacitance		-	120	155	pF
$C_{rss}$	Reverse Transfer Capacitance		-	16	20	pF

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 150\text{ V}, I_D = 9.0\text{ A}, R_G = 25\ \Omega$ (Note 4)	-	16	40	ns
$t_r$	Turn-On Rise Time		-	120	250	ns
$t_{d(off)}$	Turn-Off Delay Time		-	27	65	ns
$t_f$	Turn-Off Fall Time		-	48	110	ns
$Q_g$	Total Gate Charge	$V_{DS} = 240\text{ V}, I_D = 9.0\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	17	22	nC
$Q_{gs}$	Gate-Source Charge		-	3.9	-	nC
$Q_{gd}$	Gate-Drain Charge		-	9.2	-	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	-	-	9.0	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	-	-	36	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 9.0\text{ A}$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 9.0\text{ A}, dI_F / dt = 100\text{ A}/\mu\text{s}$	-	170	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	1.4	-	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

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## Typical Characteristics

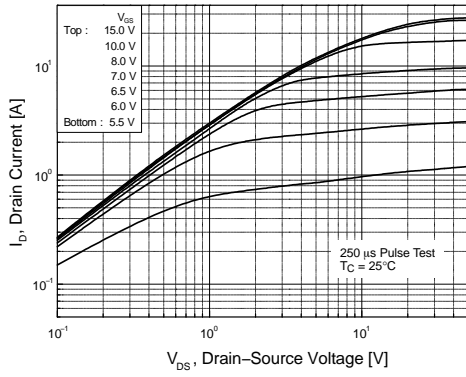


Figure 1. On-Region Characteristics

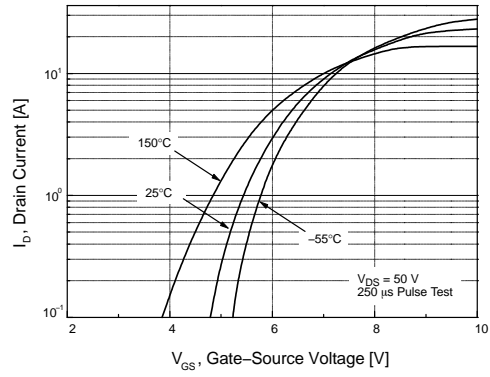


Figure 2. Transfer Characteristics

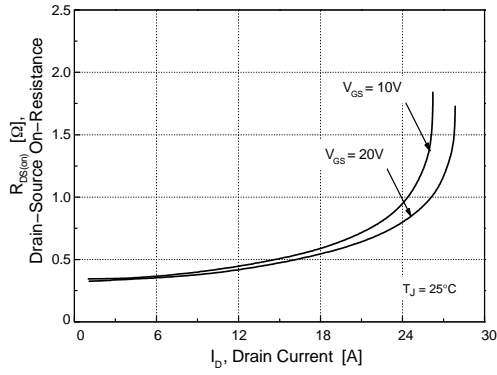


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

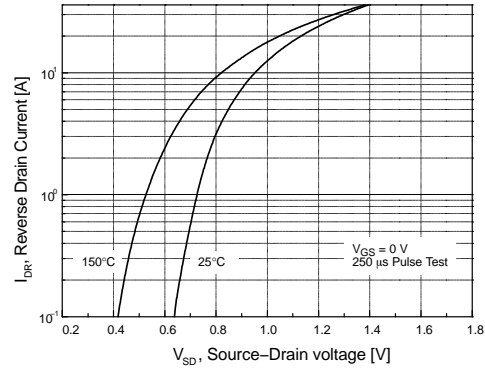


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

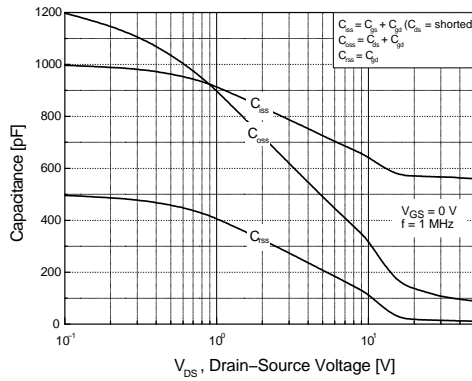


Figure 5. Capacitance Characteristics

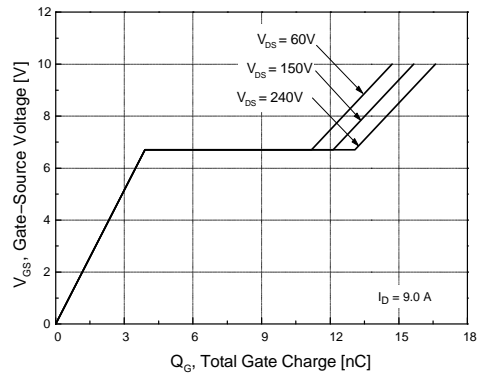


Figure 6. Gate Charge Characteristics

Typical Characteristics

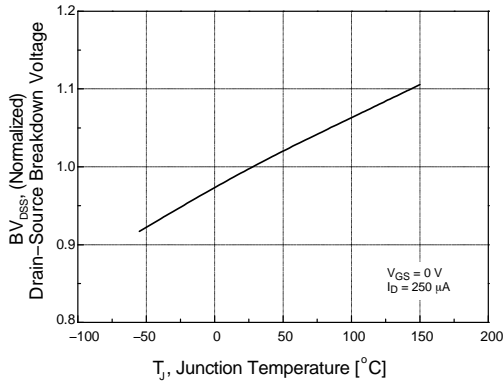


Figure 7. Breakdown Voltage Variation vs. Temperature

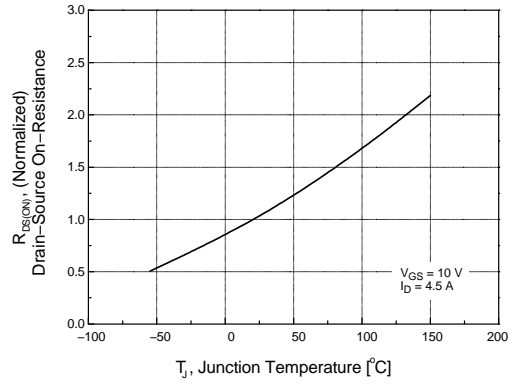


Figure 8. On-Resistance Variation vs. Temperature

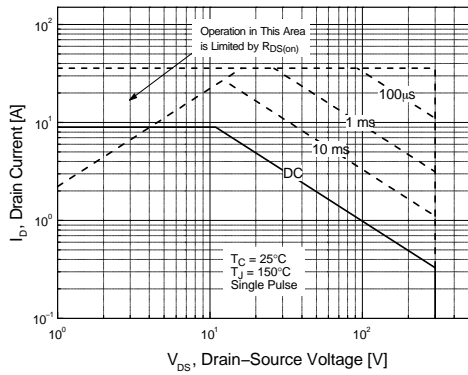


Figure 9. Maximum Safe Operating Area

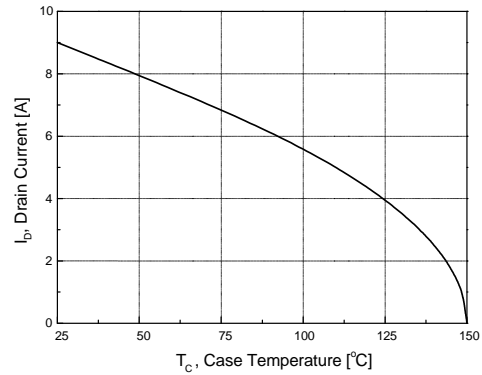


Figure 10. Maximum Drain Current vs. Case Temperature

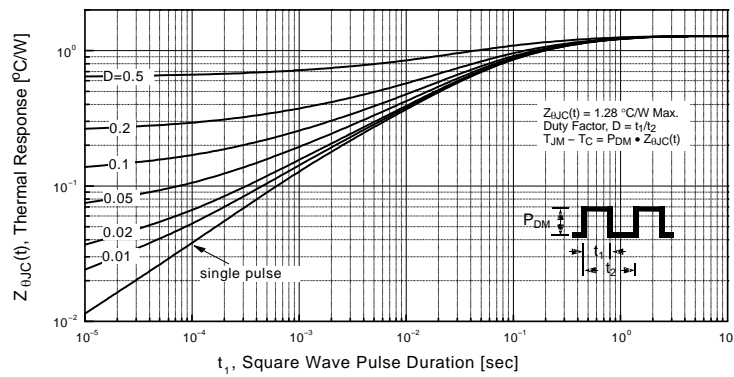


Figure 11. Transient Thermal Response Curve

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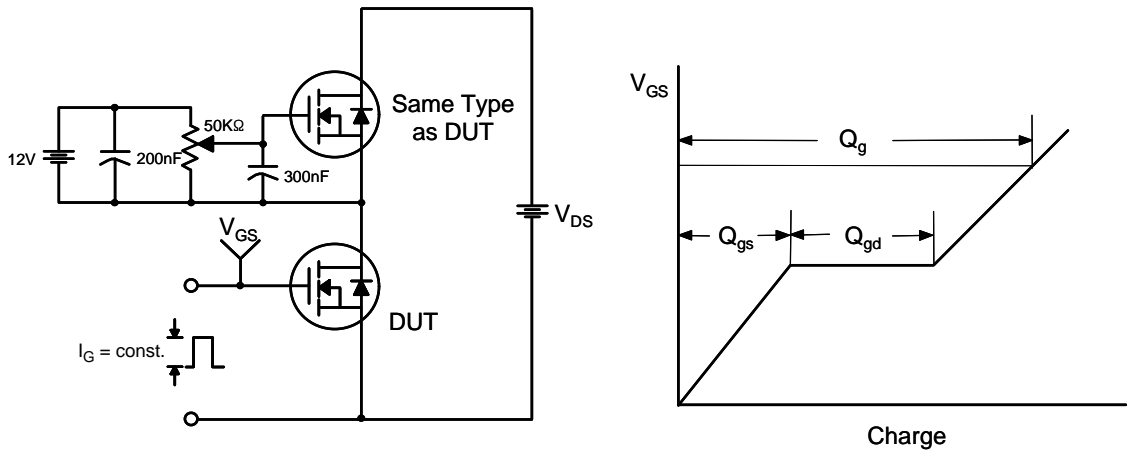


Figure 12. Gate Charge Test Circuit & Waveforms

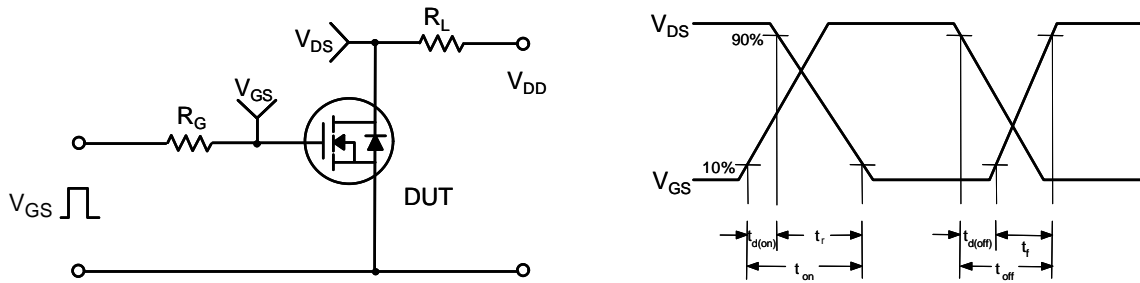


Figure 13. Resistive Switching Test Circuit & Waveforms

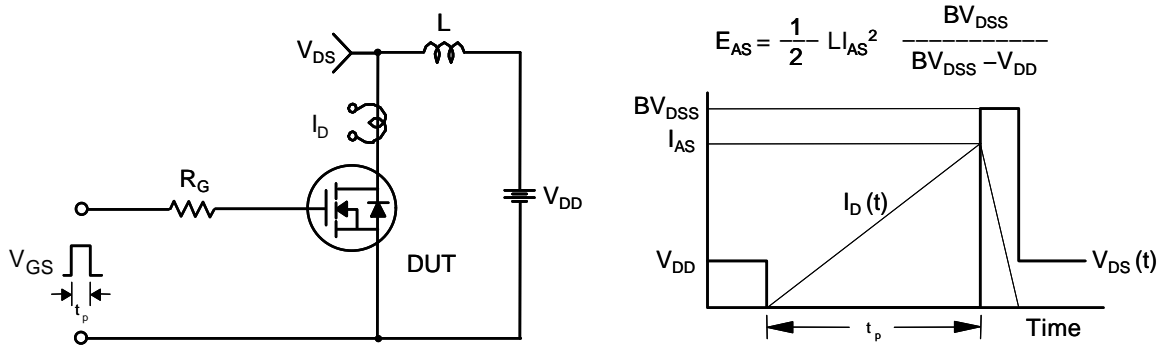


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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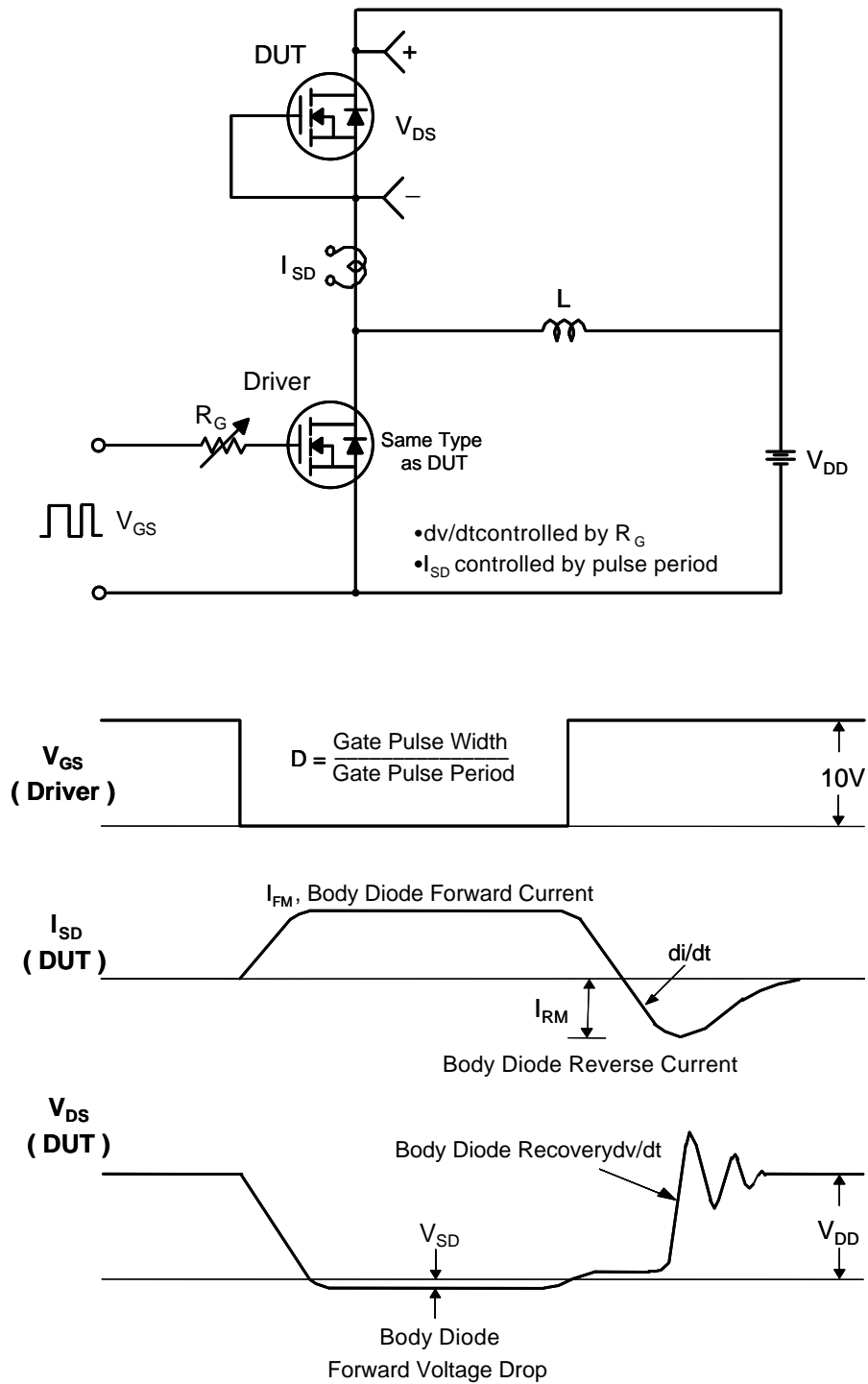
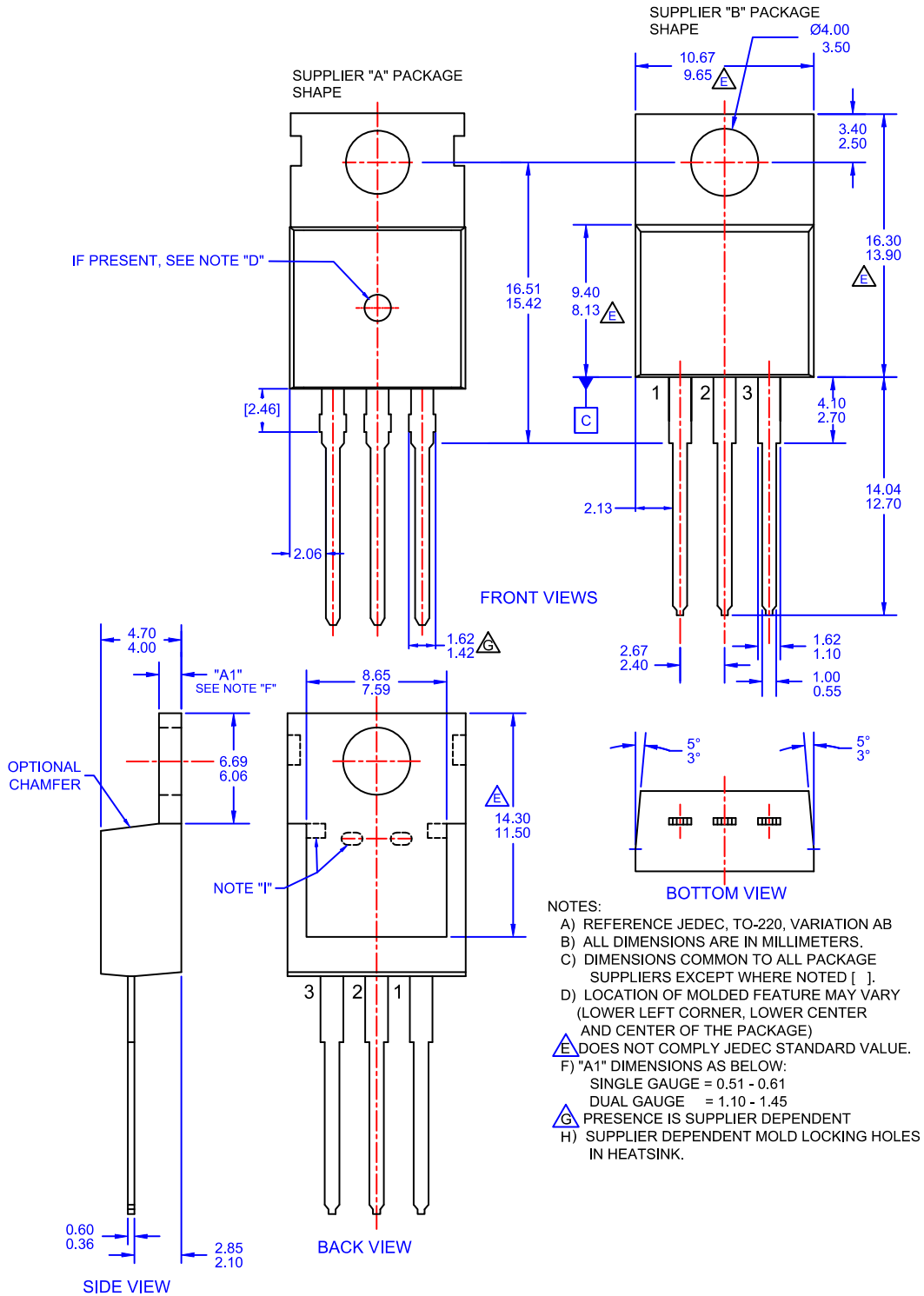


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

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## PACKAGE DIMENSIONS

TO-220-3LD  
CASE 340AT  
ISSUE O



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