

ON Semiconductor®

## FQD5N60C / FQU5N60C

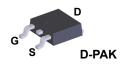
## N-Channel QFET® MOSFET 600 V, 2.8 A, 2.5 Ω

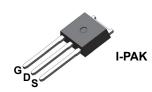
# **Featurés**

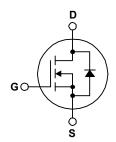
- 2.8 A, 600 V,  $R_{DS(on)}$  = 2.5  $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 1.4 A
- Low Gate Charge (Typ. 15 nC)
- Low Crss (Typ. 6.5 pF)
- · 100% Avalanche Tested
- · RoHS compliant

#### Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.







## **Absolute Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQD5N60CTM / FQU5N60CTU	Unit
V <sub>DSS</sub>	Drain-Source Voltage		600	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		2.8	Α
	- Continuous (T <sub>C</sub> = 100°C)		1.8	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	11.2	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	210	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)		2.8	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		4.9	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
$P_{D}$	Power Dissipation (T <sub>A</sub> = 25°C)*		2.5	W
	Power Dissipation (T <sub>C</sub> = 25°C)		49	W
	- Derate above 25°C		0.39	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FQD5N60CTM / FQU5N60CTU	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.56		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (minimum pad of 2 oz copper), Max.	110	°C/W	
	Thermal Resistance, Junction-to-Ambient (* 1 in² pad of 2 oz copper), Max.	50		

## **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD5N60C	FQD5N60CTM	D-PAK	330 mm	16 mm	2500 units
FQU5N60C	FQU5N60CTU	I-PAK	Tube	N/A	70 units

## $\label{eq:control} \textbf{Electrical Characteristics} \quad \textbf{T}_{C} = 25^{\circ} \text{C unless otherwise noted}.$

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	600			V
$\Delta BV_{DSS}$ / $\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.6		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V			1	μΑ
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C			10	μΑ
$I_{GSSF}$	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.4 A		2.0	2.5	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 1.4 A		4.7		S
Dynami C <sub>iss</sub>	c Characteristics Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		515	670	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		55	72	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 1.0 10.11		6.5	8.5	pF
Switchi	ng Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V = 200 V I = 4.5A		10	30	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD}$ = 300 V, $I_{D}$ = 4.5A, $R_{G}$ = 25 $\Omega$ (Note 4)		42	90	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			38	85	ns
t <sub>f</sub>	Turn-Off Fall Time			46	100	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 4.5A,		15	19	nC
$Q_{gs}$	Gate-Source Charge	V <sub>GS</sub> = 10 V		2.5		nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)		6.6		nC
Drain-S	ource Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2.8	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				11.2	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.8 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = 4.5 \text{ A},$		300		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		2.2		μС

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. L = 18.9mH, I<sub>AS</sub> = 4.5 A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.
- $3.~I_{SD} \leq 4.5 A,~di/dt \leq 200 A/\mu s,~V_{DD} \leq BV_{DSS,}~starting~~T_J = 25^{\circ}C.$
- 4. Essentially independent of operating temperature.

## **Typical Characteristics**

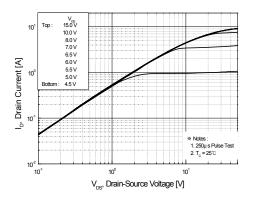


Figure 1. On-Region Characteristics

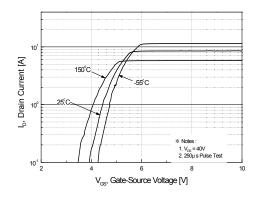


Figure 2. Transfer Characteristics

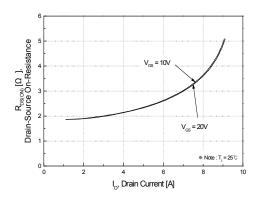


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

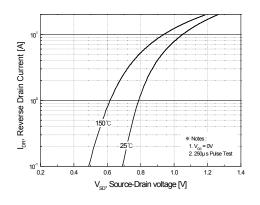


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

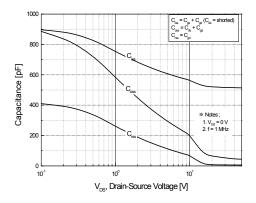


Figure 5. Capacitance Characteristics

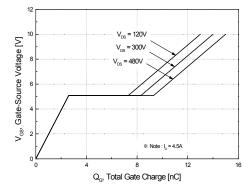
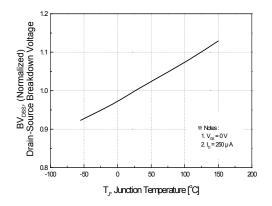


Figure 6. Gate Charge Characteristics

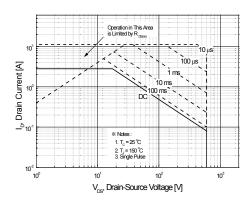
### Typical Characteristics (Continued)



30 25 (parties 20 20 25 (parties 20 25 (parties

Figure 7. Breakdown Voltage Variation vs Temperature





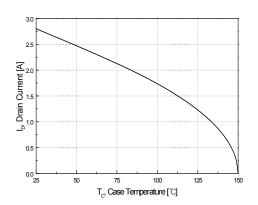


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs Case Temperature

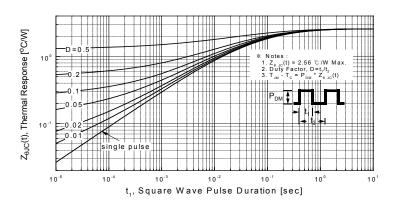


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

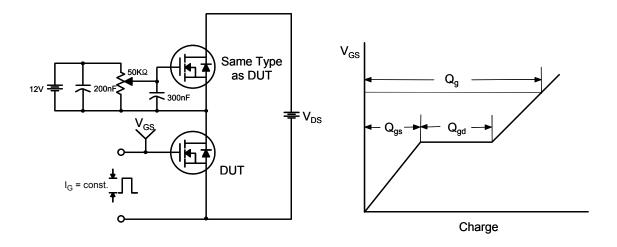


Figure 13. Resistive Switching Test Circuit & Waveforms

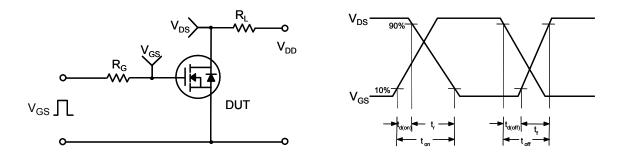
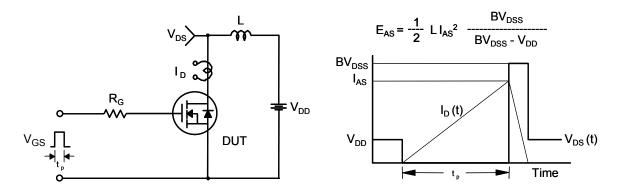


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



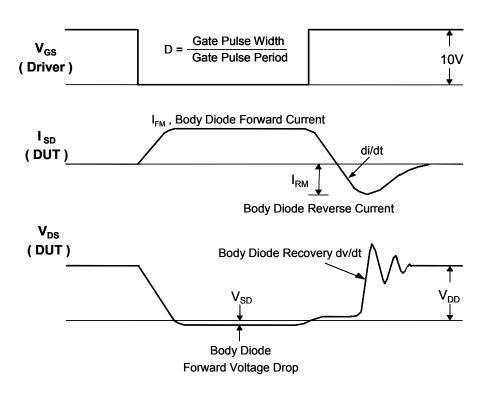
**Ļ** V<sup>DD</sup>

DUT V<sub>DS</sub>
V<sub>DS</sub>
Driver

Same Type as DUT

• dv/dt controlled by R<sub>G</sub>
• I<sub>SD</sub> controlled by pulse period

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



#### **Mechanical Dimensions**

# TO-252 3L (DPAK)

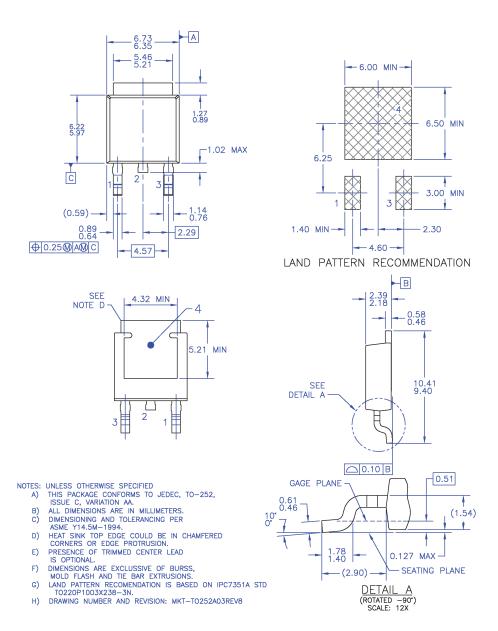


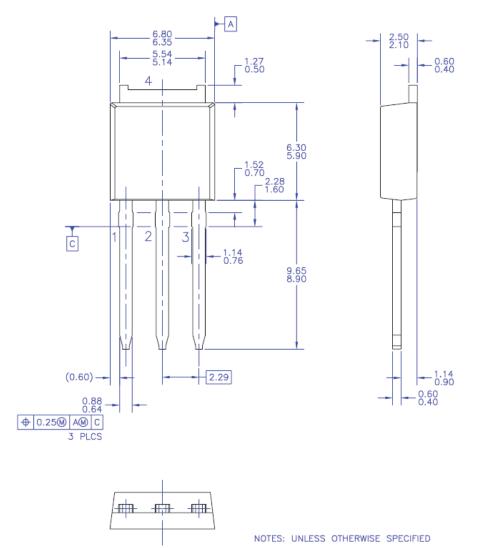
Figure 16. TO252 (D-PAK), Molded, 3 Lead, Option AA&AB

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Dimension in Millimeter

#### **Mechanical Dimensions**

# TO-251 3L (IPAK)



- ALL DIMENSIONS ARE IN MILLIMETERS.
- THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

Figure 17. TO251 (IPAK) Molded 3 Lead

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Dimension in Millimeters

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