FAIRCHILD

SEMICONDUCTOR®

QFET™

FQD6N40C / FQU6N40C

400V N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, electronic lamp ballasts based on half bridge topology.

Features

- 4.5A, 400V, $R_{DS(on)}$ = 1.0 Ω @V_{GS} = 10 V
- Low gate charge (typical 16nC)
- Low Crss (typical 15pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

D-PAK
FQD Series
G S

I-PAK
FQU Series
G D S

D

G

S
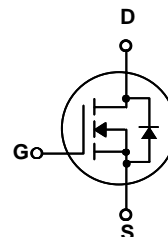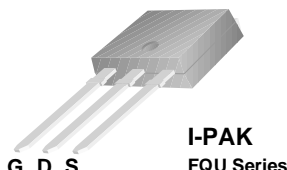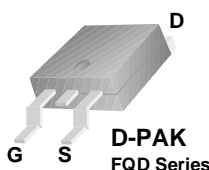
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FQD6N40C / FQU6N40C	Units
V_{DSS}	Drain-Source Voltage		400	V
I_D	Drain Current - Continuous (T_C = 25°C)		4.5	A
	- Continuous (T_C = 100°C)		2.7	A
I_{DM}	Drain Current - Pulsed	(Note 1)	18	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	270	mJ
I_{AR}	Avalanche Current	(Note 1)	4.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)*		2.5	W
	Power Dissipation (T_C = 25°C)		48	W
	- Derate above 25°C		0.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient.*	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient.	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics
$T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA	400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Referenced to 25°C	--	0.54	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 400$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 320$ V, $T_C = 125°C$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 2.25$A	--	0.83	1	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40$ V, $I_D = 2.25$A (Note 4)	--	4.7	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	480	625	pF
C_{oss}	Output Capacitance		--	80	105	pF
C_{rss}	Reverse Transfer Capacitance		--	15	20	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 200$ V, $I_D = 6$A, $R_G = 25$ Ω	--	13	35	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	21	55	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	38	85	ns
Q_g	Total Gate Charge	$V_{DS} = 320$ V, $I_D = 6$A, $V_{GS} = 10$ V	--	16	20	nC
Q_{gs}	Gate-Source Charge		--	2.3	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	8.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	4.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	18	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 4.5$ A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 6$ A, $dI_F / dt = 100$ A/μs (Note 4)	--	230	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.7	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 13.7 mH, $I_{AS} = 6$ A, $V_{DD} = 50$V, $R_G = 25$ Ω, Starting $T_J = 25°C$
3. $I_{SD} \leq 6$A, di/dt ≤ 200A/μs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature
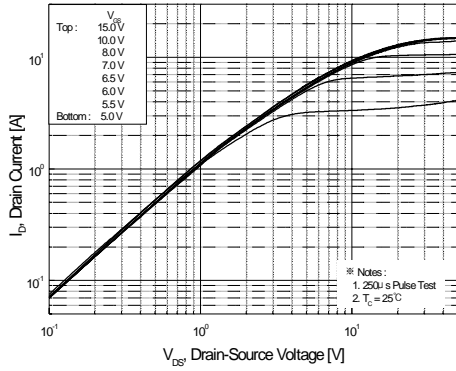
Typical Characteristics

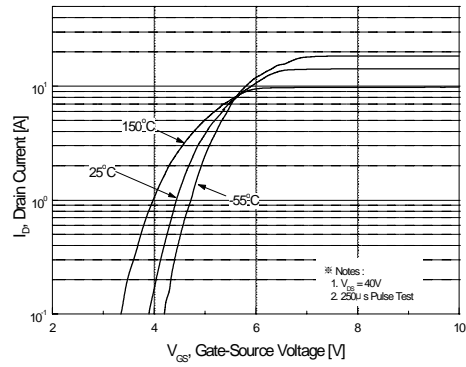**Figure 1. On-Region Characteristics**

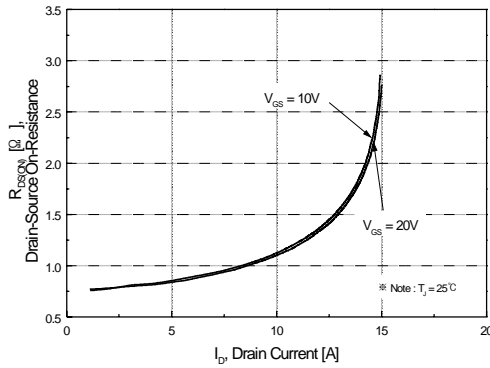**Figure 2. Transfer Characteristics**

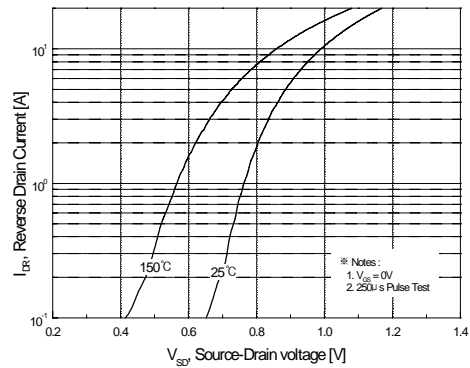**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**

Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature
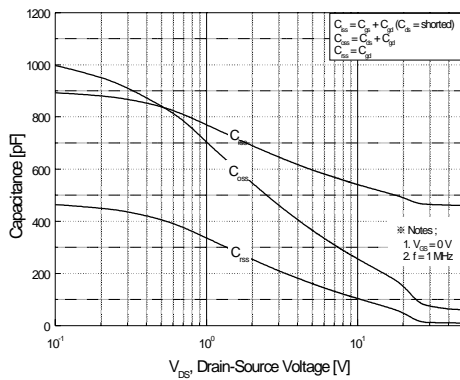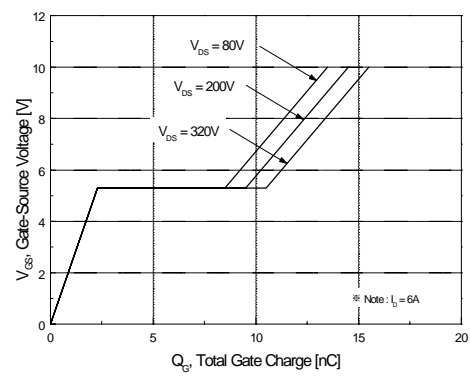

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

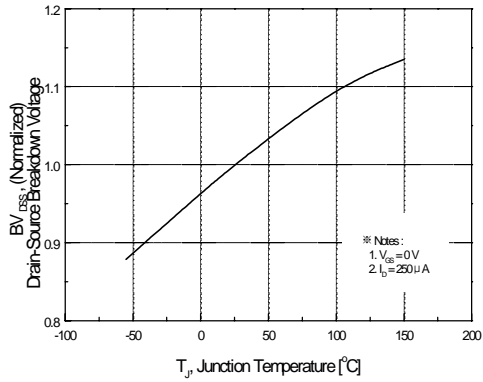## Typical Characteristics (Continued)

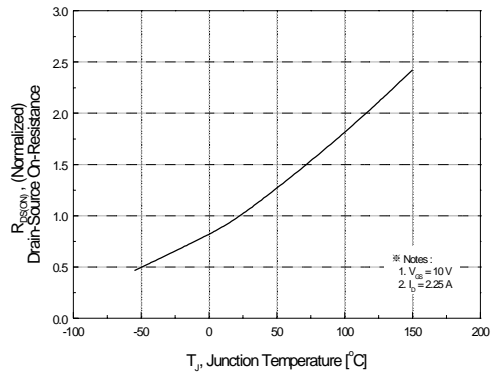**Figure 7. Breakdown Voltage Variation vs Temperature**
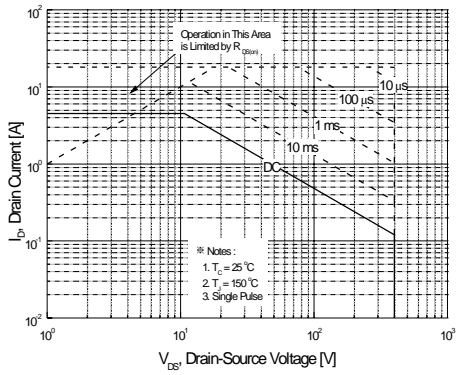

Figure 8. On-Resistance Variation vs Temperature

Figure 9. Maximum Safe Operating Area
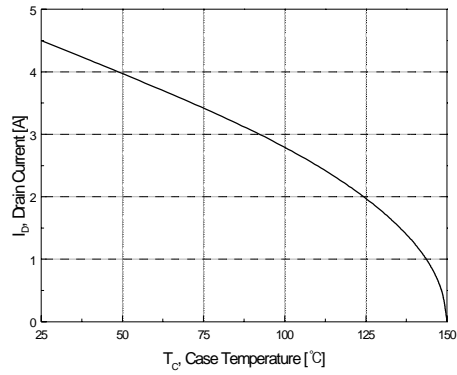
Figure 10. Maximum Drain Current vs Case Temperature
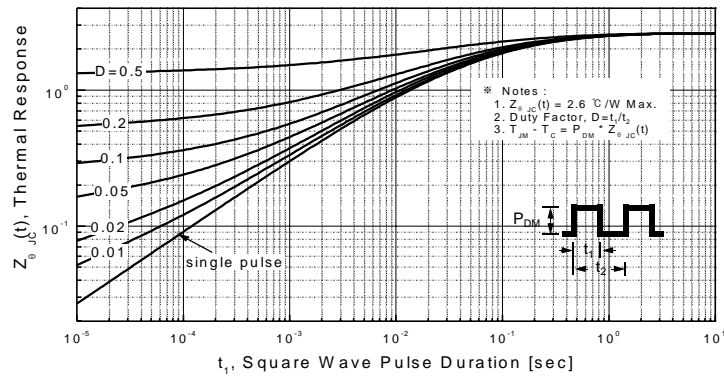
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

12V · 200nF · 50KΩ · 300nF · Same Type as DUT · V_{GS} · DUT · 3mA · V_{DS}

V_{GS} · 10V · Q_g · Q_{gs} · Q_{gd} · Charge

Resistive Switching Test Circuit & Waveforms

V_{DS} · R_L · V_{GS} · R_G · V_{DD} · 10V · DUT

V_{DS} · 90% · V_{GS} · 10% · $t_{d(on)}$ · t_r · $t_{d(off)}$ · t_f · t_{on} · t_{off}

Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS} · L · I_D · R_G · V_{DD} · 10V · t_p · DUT

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS} · I_{AS} · $I_D(t)$ · V_{DD} · $V_{DS}(t)$ · t_p · Time

Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Package Dimensions

D-PAK

Dimensions in Millimeters

Rev. A, October 2003

Package Dimensions (Continued)

I-PAK
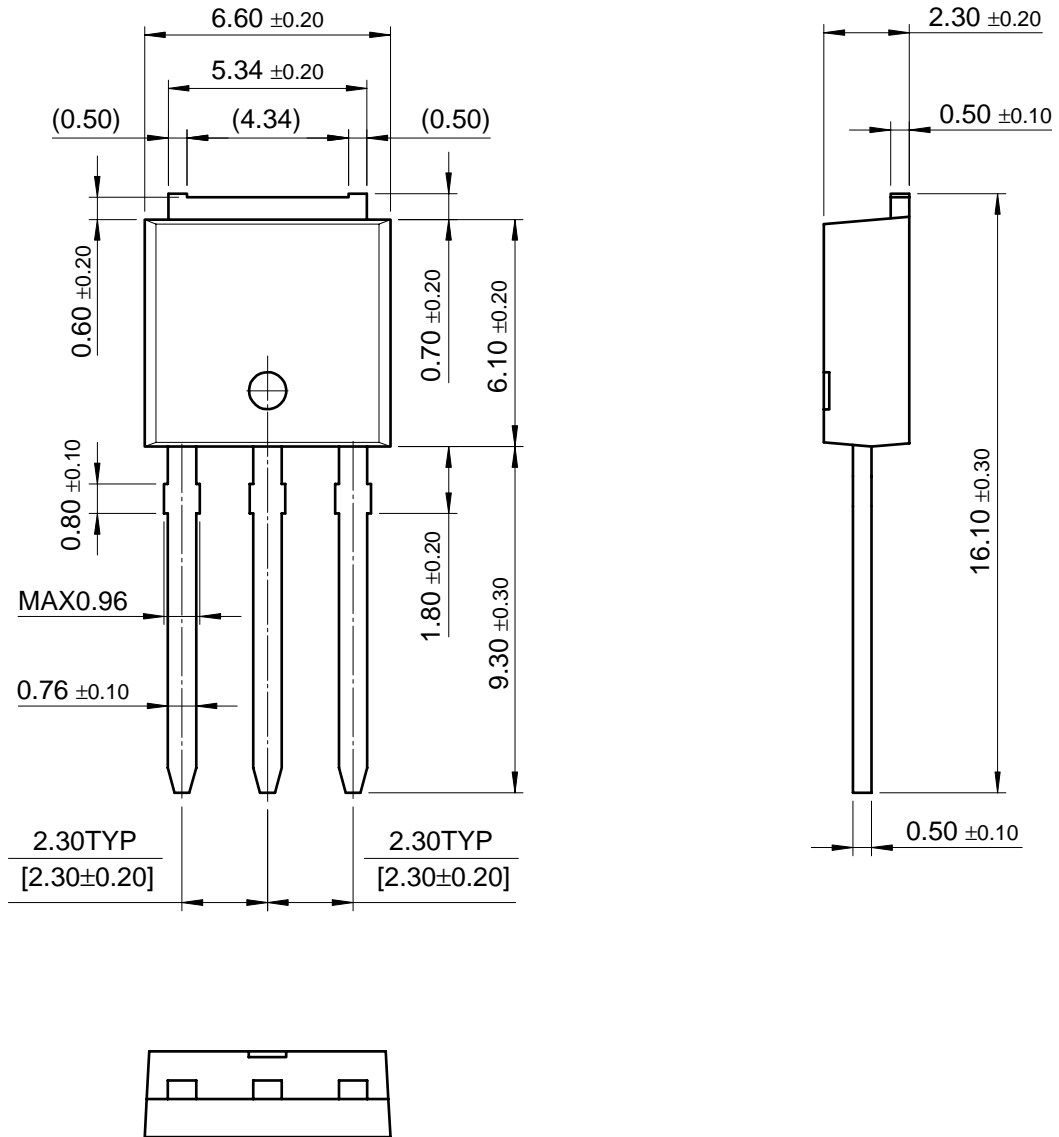
Dimensions in Millimeters

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