

23V, 4A, 500KHz Synchronous Step-Down DC/DC Converter

Description

The FR8018 is a synchronous step-down DC/DC converter that provides wide 4.5V to 23V input voltage range and 4A continuous load current capability. At light load condition, the FR8018 can operate at PSM mode to support high efficiency and reduce power loss.

The FR8018 fault protection includes cycle-by-cycle current limit, UVLO and thermal shutdown. Besides, adjustable soft-start or internal soft-start function prevents inrush current at turn-on. This device uses current mode control scheme which provides fast transient response. Internal compensation function reduces external compensator components and simplifies the design process. In shutdown mode, the supply current is about 1 μ A.

The FR8018 is offered in SOP-8 (Exposed Pad) package and provides good thermal conductance.

Features

- Low $R_{DS(ON)}$ Integrated Power MOSFET
- Internal Compensation Function
- Wide Input Voltage Range: 4.5V to 23V
- Adjustable Output Voltage Down to 0.765V
- 4A Output Current
- Fixed 500kHz Switching Frequency
- External Programmable Soft-Start or Internal 1ms Soft-Start
- PSM (High Efficiency at Light Load)
- Cycle-by-Cycle Current Limit
- Over-Temperature Protection with Auto Recovery
- Under Voltage Lockout
- <1 μ A Shutdown Current
- Hiccup Short Circuit Protection
- FB pin Floating Protection
- SOP-8 Exposed Pad Package
- RoHS Compliant

Applications

- LCD Display, TV
- STB (Set-Top-Box)
- Distributed Power System
- Networking, XDSL Modem

Pin Assignments

SP Package (SOP-8 Exposed Pad)

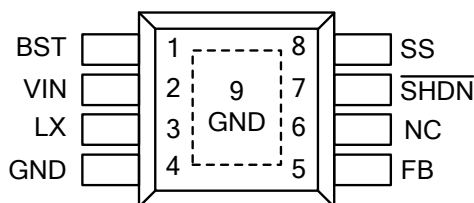
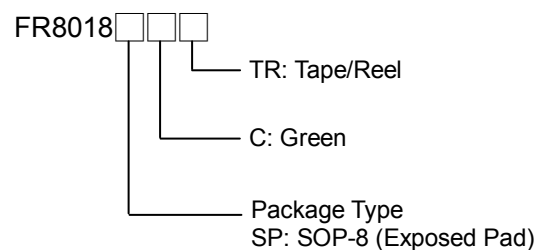


Figure 1. Pin Assignments of FR8018

Ordering Information



Typical Application Circuit

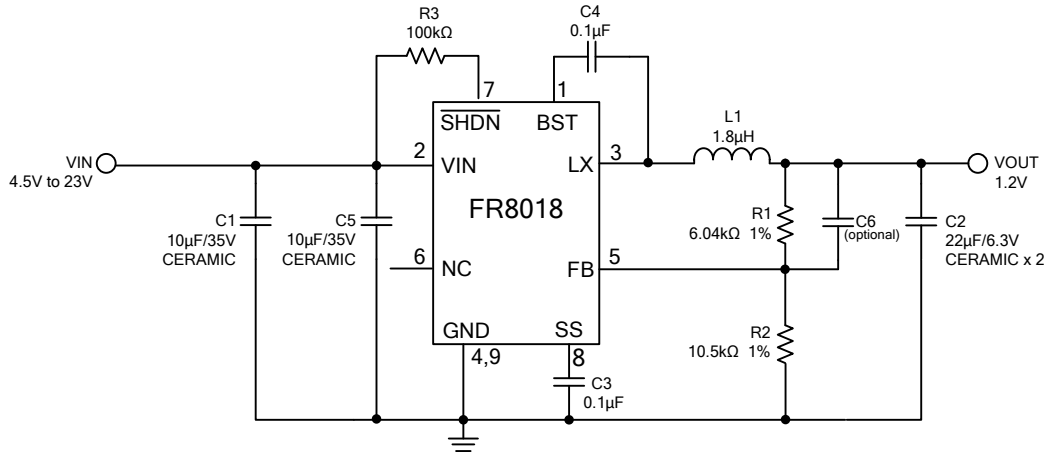


Figure 2. C_{IN}/C_{OUT} use Ceramic Capacitors Application Circuit

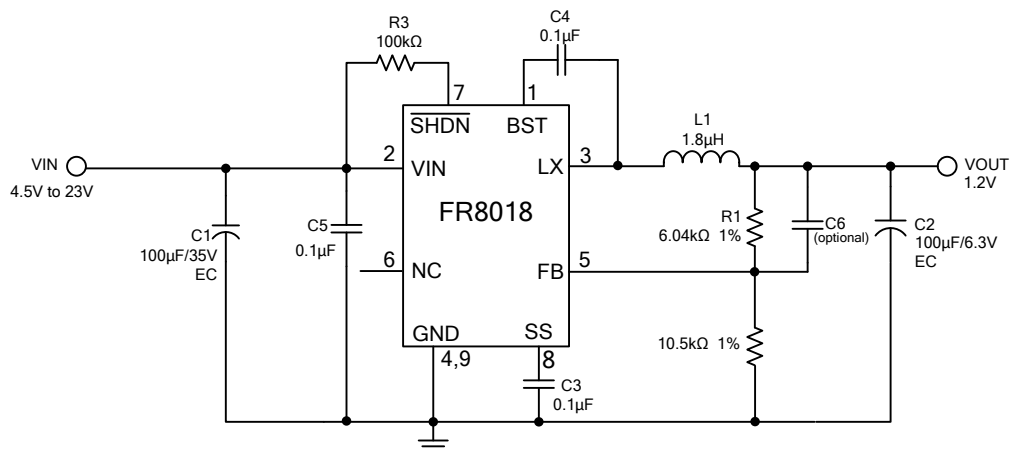


Figure 3. C_{IN}/C_{OUT} use Electrolytic Capacitors Application Circuit

$V_{IN}=12V$, the recommended BOM list is as below.

V_{OUT}	C1	R1	R2	C5	C6	L1	C2
1.2V	10µF MLCC	6.04kΩ	10.5kΩ	10µF MLCC	10pF~1nF	1.8µH	22µF MLCC x2
1.8V	10µF MLCC	14.3kΩ	10.5kΩ	10µF MLCC	10pF~1nF	2.2µH	22µF MLCC x2
2.5V	10µF MLCC	23.7kΩ	10.5kΩ	10µF MLCC	10pF~1nF	3.3µH	22µF MLCC x2
3.3V	10µF MLCC	34.8kΩ	10.5kΩ	10µF MLCC	10pF~1nF	3.3µH	22µF MLCC x2
5V	10µF MLCC	59kΩ	10.5kΩ	10µF MLCC	10pF~1nF	4.7µH	22µF MLCC x2
1.2V	100µF EC	6.04kΩ	10.5kΩ	0.1µF	--	1.8µH	100µF EC
1.8V	100µF EC	14.3kΩ	10.5kΩ	0.1µF	--	2.2µH	100µF EC
2.5V	100µF EC	23.7kΩ	10.5kΩ	0.1µF	--	3.3µH	100µF EC
3.3V	100µF EC	34.8kΩ	10.5kΩ	0.1µF	--	3.3µH	100µF EC
5V	100µF EC	59kΩ	10.5kΩ	0.1µF	--	4.7µH	100µF EC

Table 1. Recommended Component Values

Functional Pin Description

Pin Name	Pin No.	Pin Function
BST	1	High side gate drive boost pin. A capacitance between 10nF~100nF must be connected from this pin to LX. It can boost the gate drive to fully turn on the internal high side NMOS.
VIN	2	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
LX	3	Power switching output. Connect an external inductor to this switching node.
GND	4	Ground pin. Connect this pin to exposed pad.
NC	6	No connection.
FB	5	Feedback input pin. Connect FB and V_{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.765V.
SHDN	7	Enable input pin. Pull high to turn on IC, and pull low to turn off IC. Connect VIN with a 100kΩ resistor for self-startup.
SS	8	Soft-start pin. This pin controls the soft-start period. Connect a capacitor from SS to GND to set the soft start period.
Exposed Pad	9	Ground pin. The exposed pad must be soldered to a large PCB area and connected to GND for maximum power dissipation.

Block Diagram

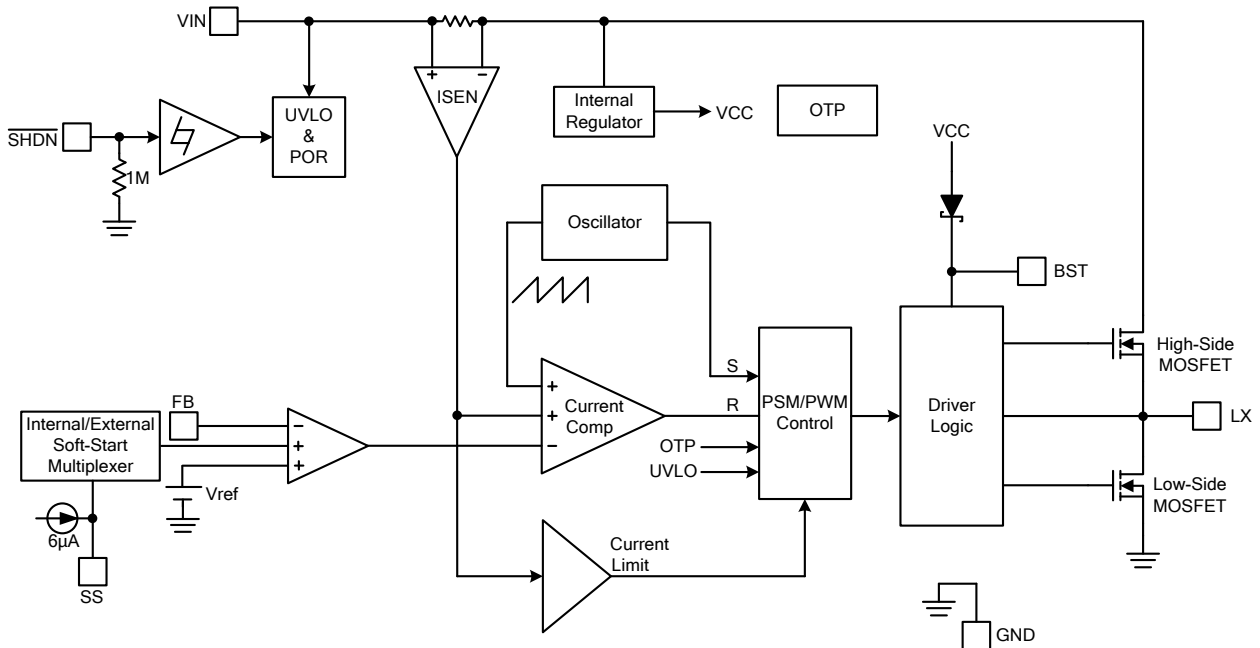


Figure 4. Block Diagram of FR8018

Absolute Maximum Ratings (Note1)

- Supply Voltage V_{IN} ----- -0.3V to +25V
- Enable Voltage V_{SHDN} ----- -0.3V to +25V
- LX Voltage V_{LX} ----- -1V to $V_{IN}+0.3V$
- Dynamic LX Voltage in 15ns Duration----- -6V to $V_{IN}+6V$
- BST Pin Voltage V_{BST} ----- $V_{LX}-0.3V$ to $V_{LX}+6.5V$
- All Other Pins Voltage ----- -0.3V to +6V
- Maximum Junction Temperature (T_J) ----- +150°C
- Storage Temperature (T_S) ----- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ----- +260°C
- Package Thermal Resistance (θ_{JA}) (Note2)
 - SOP-8 (Exposed Pad) ----- 60°C/W
- Package Thermal Resistance (θ_{JC})
 - SOP-8 (Exposed Pad) ----- 15°C/W

Note 1 : Stresses beyond this listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Note 2 : PCB heat sink copper area=10mm².

Recommended Operating Conditions

- Supply Voltage V_{IN} ----- +4.5V to +23V
- Operation Temperature Range ----- -40°C to +85°C

Electrical Characteristics

($V_{IN}=12V$, $T_A=25^{\circ}C$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{IN} Quiescent Current	I_{DDQ}	$V_{\overline{SHDN}}=1.8V$, $V_{FB}=1.0V$		2		mA
V_{IN} Shutdown Supply Current	I_{SD}	$V_{\overline{SHDN}}=0V$		1	10	μA
Feedback Voltage	V_{FB}	$4.5V \leq V_{IN} \leq 23V$	0.753	0.765	0.777	V
High-Side MOSFET $R_{DS(ON)}$ (Note3)	$R_{DS(ON)}$			95		m Ω
Low-Side MOSFET $R_{DS(ON)}$ (Note3)	$R_{DS(ON)}$			55		m Ω
High-Side MOSFET Leakage Current	$I_{LX(leak)}$	$V_{\overline{SHDN}}=0V$, $V_{LX}=0V$			10	μA
High-Side MOSFET Current Limit (Note3)	$I_{LIMIT(HS)}$	Minimum Duty		5.5		A
Oscillation Frequency	F_{OSC}		375	500	625	kHz
Short Circuit Oscillation Frequency	$F_{OSC(short)}$	$V_{FB}=0.2V$		150		kHz
Maximum Duty Cycle	D_{MAX}	$V_{FB}=0.7V$		88		%
Minimum On Time (Note3)	T_{MIN}			100		ns
Input Supply Voltage UVLO Threshold	$V_{UVLO(VTH)}$	V_{IN} Rising		4.2		V
Input Supply Voltage UVLO Threshold Hysteresis	$V_{UVLO(HYS)}$			400		mV
Soft-Start Current	I_{SS}	$V_{SS}=0V$		6		μA
External Soft-Start Period	T_{SS}	$C_{SS}=0.1\mu F$		13		ms
Internal Soft-Start Period	T_{SS}	SS pin floating		1		ms
\overline{SHDN} Input Low Voltage	$V_{\overline{SHDN}(L)}$				0.4	V
\overline{SHDN} Input High Voltage	$V_{\overline{SHDN}(H)}$		2			V
\overline{SHDN} Input Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}=2V$		2		μA
Thermal Shutdown Threshold (Note3)	T_{SD}			165		$^{\circ}C$

Note 3 : Not production tested.

Function Description

The FR8018 is a high efficiency, internal compensation and constant frequency current mode step-down synchronous DC/DC converter. It has integrated high-side (95mΩ, typ) and low-side (55mΩ, typ) power switches, and provides 4A continuous load current. It regulates input voltage from 4.5V to 23V, and down to an output voltage as low as 0.765V.

Control Loop

Under normal operation, the output voltage is sensed by FB pin through a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output is compared to the switch current to control the RS flip-flop. At the beginning of each clock cycle, the high-side NMOS turns on when the oscillator sets the RS flip-flop, and turns off when current comparator resets the RS flip-flop. Then the low-side NMOS will turn on until the clock period ends.

Enable

The FR8018 $\overline{\text{SHDN}}$ pin provides digital control to turn on/off the regulator. When the voltage of $\overline{\text{SHDN}}$ exceeds the threshold voltage, the regulator will start the soft start function. If the $\overline{\text{SHDN}}$ pin voltage is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μA. For auto start-up operation, connect $\overline{\text{SHDN}}$ to VIN through a 100KΩ resistor.

Soft-Start

The FR8018 employs internal and programmable external soft-start functions to reduce input inrush current during start up. When SS pin doesn't connect to C_{SS} capacitor, the internal soft-start time will be 1ms. When SS pin connects to C_{SS} capacitor, the C_{SS} capacitor will be charged by a 6μA current. The equation for the soft-start time is shown as below:

$$T_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \times V_{FB}}{I_{SS}(\mu\text{A})}$$

The V_{FB} voltage is 0.765V and the I_{SS} current is 6μA. If a 0.1μF capacitor is connected from SS pin to GND, the soft-start time will be 13ms.

Under Voltage Lockout

When the FR8018 is power on, the internal circuits will be held inactive until V_{IN} voltage exceeds the UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the UVLO threshold voltage. The hysteresis of the UVLO comparator is 400mV (typ).

Short Circuit Protection

The FR8018 provides short circuit protection function to prevent the device damage from short condition. When the short condition occurs and the feedback voltage drops lower than 0.4V, the oscillator frequency will be reduced to 150kHz and hiccup mode will be triggered to prevent the inductor current increasing beyond the current limit. Once the short condition is removed, the frequency will return to normal.

Over Current Protection

The FR8018 over current protection function is implemented using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

Over Temperature Protection

The FR8018 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteresis of the over temperature protection is 60°C (typ).

Internal Compensation Function

The stability of the feedback circuit is controlled by internal compensation circuits. This internal compensation function is optimized for most applications and this function can reduce external R, C components.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.765V. Thus the output voltage is:

$$V_{OUT} = 0.765V \times \left(1 + \frac{R1}{R2}\right)$$

Table 2 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
5V	59k Ω	10.5k Ω
3.3V	34.8k Ω	10.5k Ω
2.5V	23.7k Ω	10.5k Ω
1.8V	14.3k Ω	10.5k Ω
1.2V	6.04k Ω	10.5k Ω

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

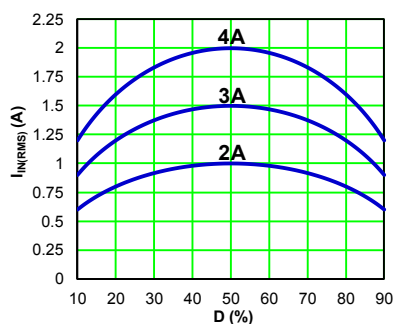
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1-D)}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at $D=0.5$ and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



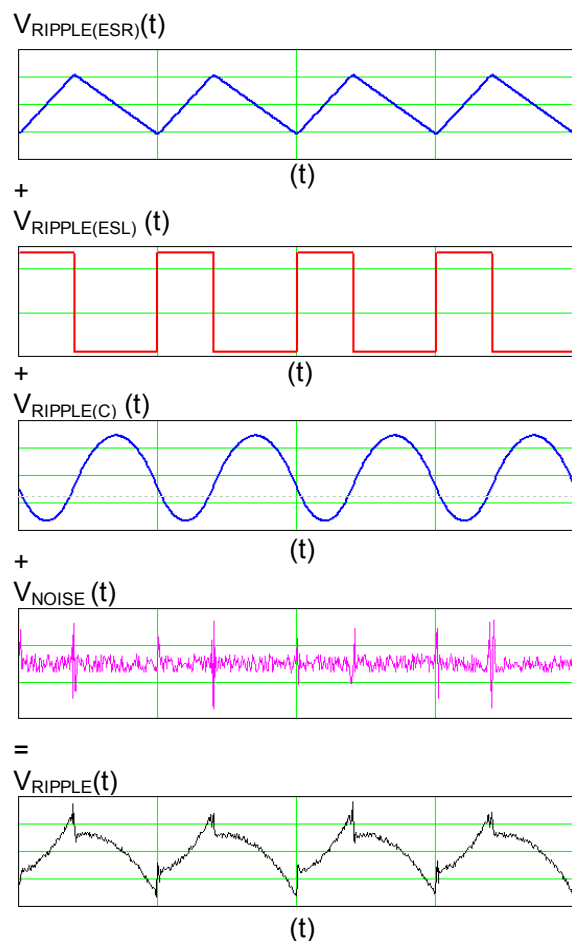
A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1 μ F ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t) = V_{RIPPLE(C)}(t) + V_{RIPPLE(ESR)}(t) + V_{RIPPLE(ESL)}(t) + V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.



Application Information (Continued)

$$V_{\text{RIPPLE(ESR)}} = \frac{V_{\text{OUT}}}{F_{\text{OSC}} \times L} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \times \text{ESR}$$

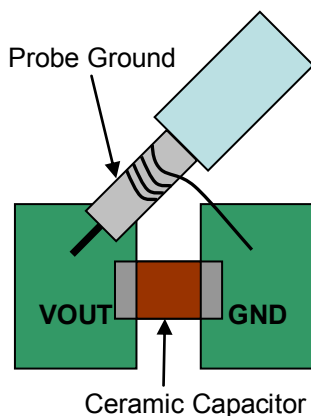
$$V_{\text{RIPPLE(ESL)}} = \frac{\text{ESL}}{L + \text{ESL}} \times V_{\text{IN}}$$

$$V_{\text{RIPPLE(C)}} = \frac{V_{\text{OUT}}}{8 \times F_{\text{OSC}}^2 \times L \times C_{\text{OUT}}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Remove the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminates noise.



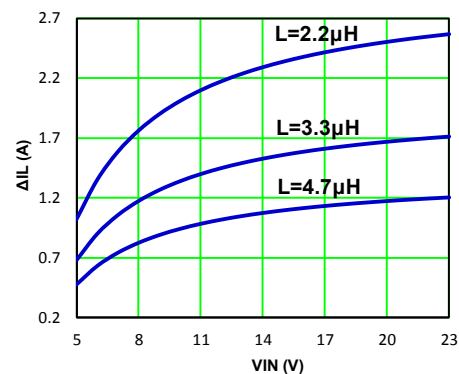
Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L = \frac{V_{\text{OUT}}}{F_{\text{OSC}} \times L} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right)$$

The following diagram is an example to graphically represent ΔI_L equation.



$V_{\text{OUT}}=3.3\text{V}$, $F_{\text{OSC}}=500\text{KHz}$

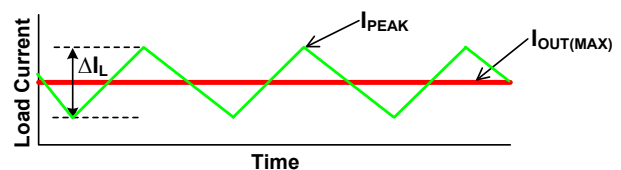
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L = 0.3 \times I_{\text{OUT(MAX)}}$$

$$L = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN}} \times F_{\text{OSC}} \times \Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the FR8018 high-side MOSFET current limit. The peak inductor current is shown as below:

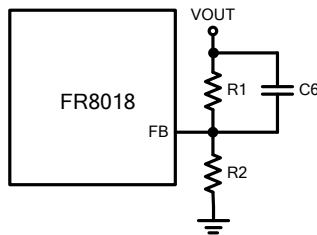
$$I_{\text{PEAK}} = I_{\text{OUT(MAX)}} + \frac{\Delta I_L}{2}$$



Application Information (Continued)

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C6 in the feedback network is recommended to improve transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C6 can be calculated with the following equation:

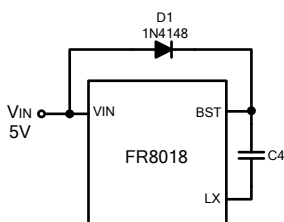
$$C6 = \frac{1}{2\pi \times F_{CROSS}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region. In general, the feedforward capacitor range is between 10pF to 1nF.

External Diode Selection

For 5V input application, it is recommended to add an external bootstrap diode. This helps improving the efficiency. The boost diode can be a low cost one such as 1N4148.



PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.

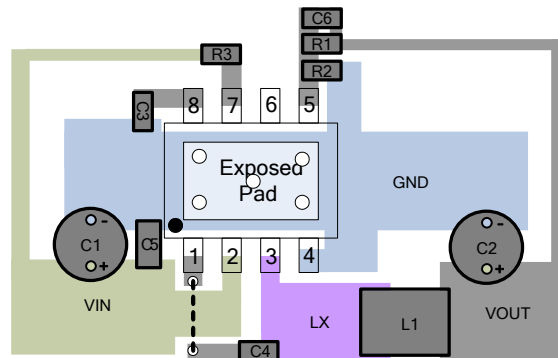
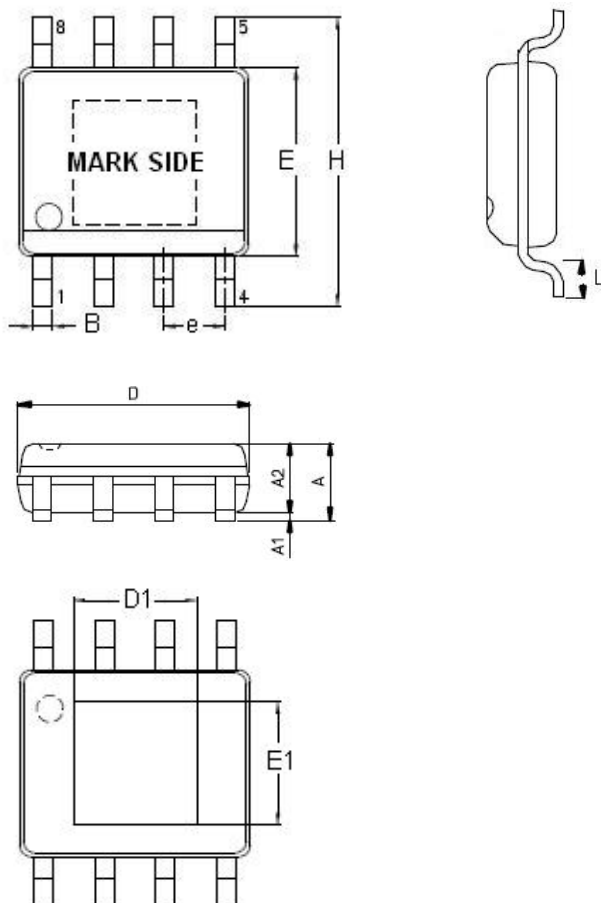


Figure 5. Recommended PCB Layout Diagram

Outline Information

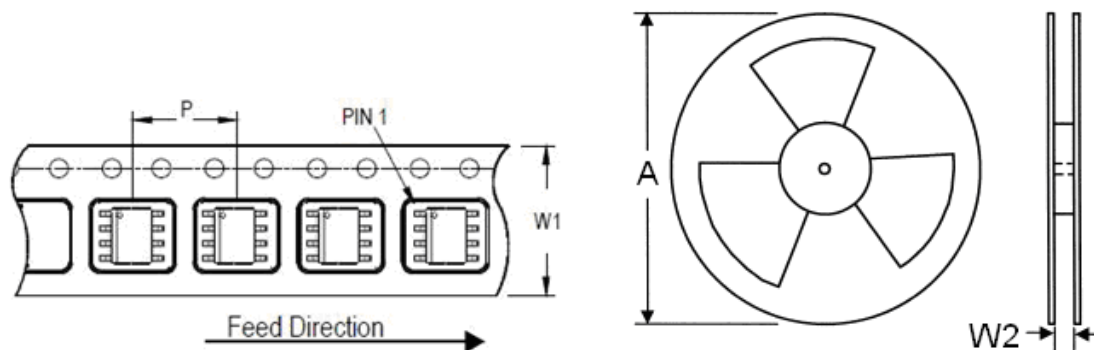
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	3.04	3.50
E	3.80	4.00
E1	2.15	2.41
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note : Followed From JEDEC MO-012-E.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

Life Support Policy

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