

June 1998

### Features

- 4A, 250V, RDS(on) = 0.700Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current
  - 4.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 1E13 Neutrons/cm<sup>2</sup>
  - Usable to 1E14 Neutrons/cm<sup>2</sup>

### Description

The Intersil Corporation has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P-Channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm<sup>2</sup> for 500V product to 1E14n/cm<sup>2</sup> for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n<sup>0</sup>) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

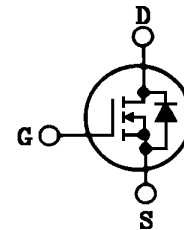
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Intersil High-Reliability Marketing group for any desired deviations from the data sheet.

### Package

TO-205AF



### Symbol



### Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

	FRL234D, R, H	UNITS
Drain-Source Voltage . . . . .	VDS	250 V
Drain-Gate Voltage (RGS = 20kΩ) . . . . .	VDGR	250 V
Continuous Drain Current		
TC = +25°C . . . . .	ID	4 A
TC = +100°C . . . . .	ID	2 A
Pulsed Drain Current . . . . .	IDM	12 A
Gate-Source Voltage . . . . .	VGS	±20 V
Maximum Power Dissipation		
TC = +25°C . . . . .	PT	25 W
TC = +100°C . . . . .	PT	10 W
Derated Above +25°C . . . . .		0.20 W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure) . . . . .	ILM	12 A
Continuous Source Current (Body Diode) . . . . .	IS	4 A
Pulsed Source Current (Body Diode) . . . . .	ISM	12 A
Operating And Storage Temperature . . . . .	TJC, TSTG	-55 to +150 °C
Lead Temperature (During Soldering)		
Distance > 0.063 in. (1.6mm) From Case, 10s Max. . . . .	TL	300 °C

# FRL234D, FRL234R, FRL234H

## Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	250	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1	VDS = 250V, VGS = 0	-	1	mA
	IDSS2	VDS = 200V, VGS = 0	-	0.025	
	IDSS3	VDS = 200V, VGS = 0, TC = +125°C	-	0.25	
Rated Avalanche Current	IAR	Time = 20μs	-	12	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 4A	-	2.94	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 2A	-	0.70	Ω
Turn-On Delay Time	td(on)	VDD = 125V, ID = 4A Pulse Width = 3μs Period = 300μs, Rg = 25Ω 0 ≤ VGS ≤ 10 (See Test Circuit)	-	35	ns
Rise Time	tr		-	85	
Turn-Off Delay Time	td(off)		-	195	
Fall Time	tf		-	75	
Gate-Charge Threshold	QG(th)	VDD = 125V, ID = 4A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		15	62	
Gate-Charge Total	QGM		30	120	
Plateau Voltage	VGP		3	12	V
Gate-Charge Source	QGS		3	12	nc
Gate-Charge Drain	QGD		7	30	
Diode Forward Voltage	VSD	ID = 4A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 4A; di/dt = 100A/μs	-	800	ns
Junction-To-Case	Rθjc		-	5.0	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	175	

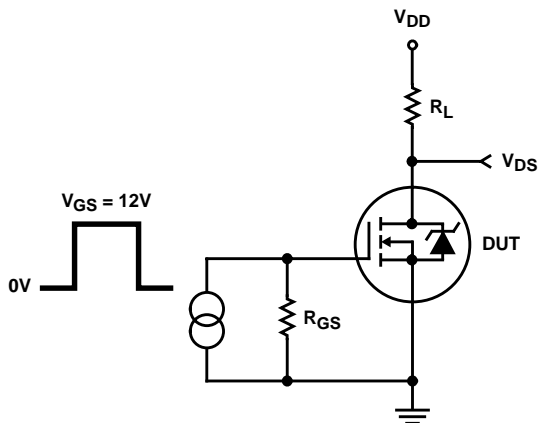


FIGURE 1. RESISTIVE SWITCHING TEST CIRCUIT

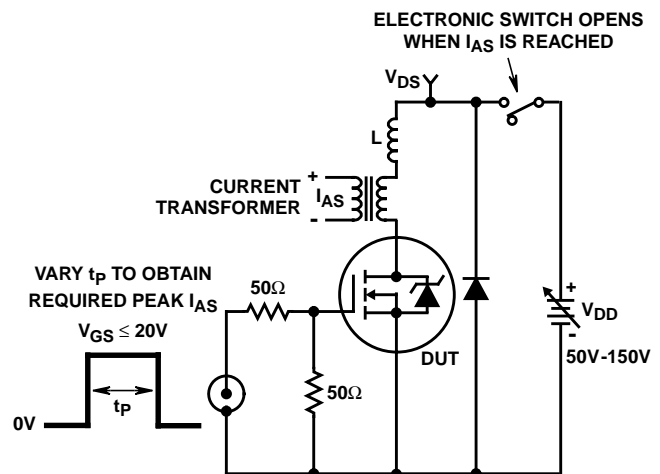


FIGURE 2. UNCLAMPED ENERGY TEST CIRCUIT

## FRL234D, FRL234R, FRL234H

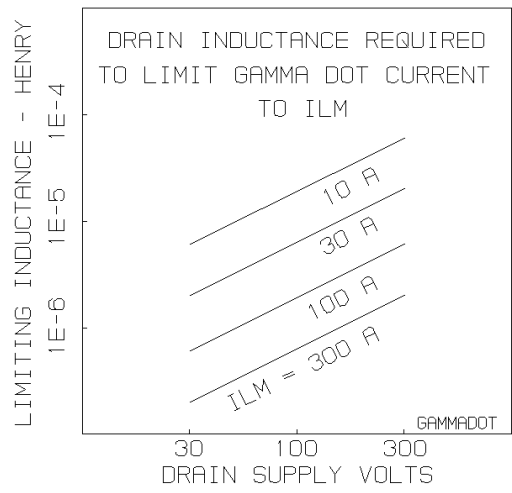
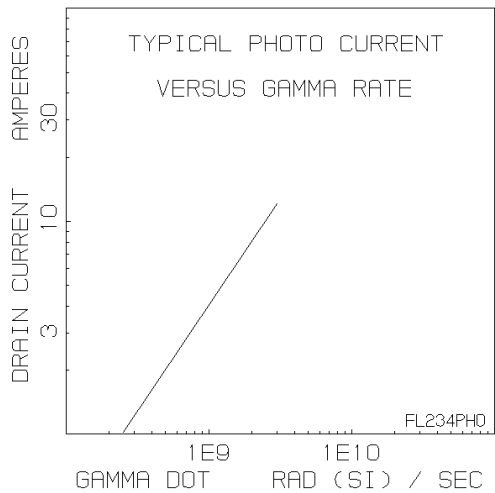
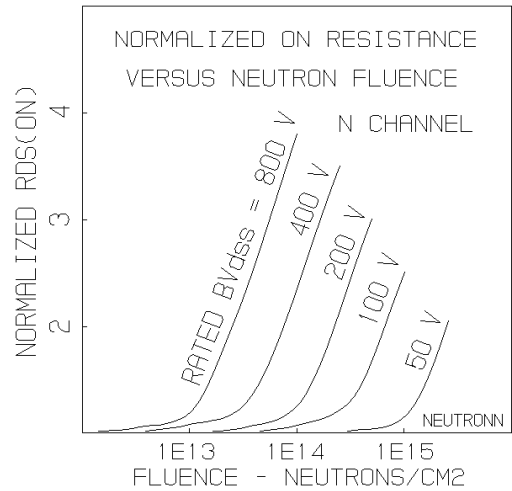
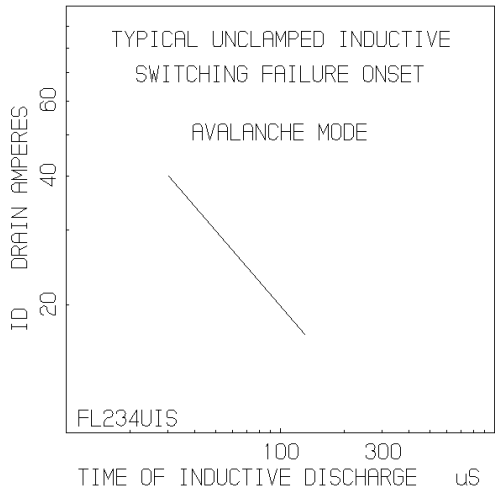
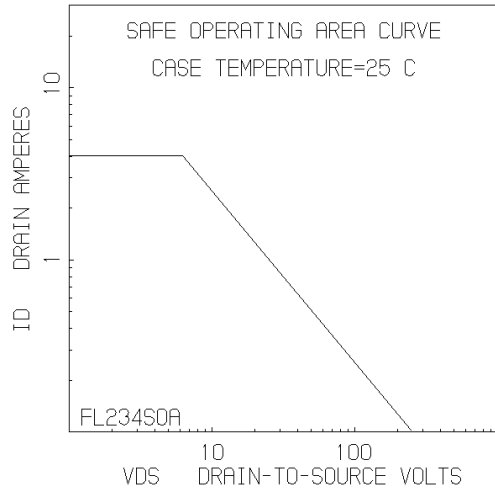
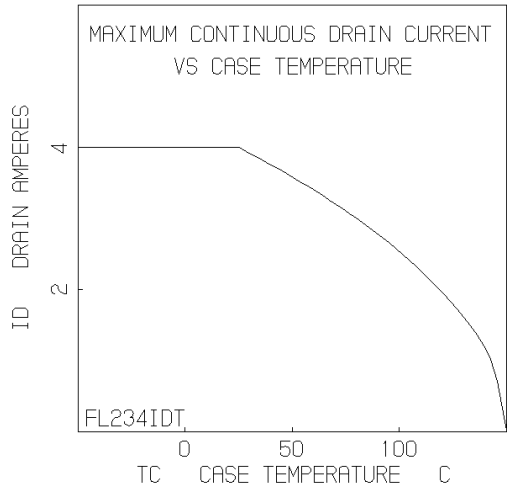
### Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS	
				MIN	MAX		
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	FRL234D, R	VGS = 0, ID = 1mA	250	-	V
	(Note 5, 6)	BVDSS	FRL234H	VGS = 0, ID = 1mA	238	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	FRL234D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	FRL234H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	FRL234D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	FRL234H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	FRL234D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	FRL234H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	FRL234D, R	VGS = 0, VDS = 200V	-	25	μA
	(Note 5, 6)	IDSS	FRL234H	VGS = 0, VDS = 200V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	FRL234D, R	VGS = 10V, ID = 4A	-	2.94	V
	(Note 1, 5, 6)	VDS(on)	FRL234H	VGS = 16V, ID = 4A	-	4.20	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	FRL234D, R	VGS = 10V, ID = 2A	-	0.700	Ω
	(Note 1, 5, 6)	RDS(on)	FRL234H	VGS = 14V, ID = 2A	-	1.0	Ω

**NOTES:**

1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 1/19/90 on TA 17633 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, Intersil Application note AN-8831, Oct. 1988

**Typical Performance Characteristics**



**Rad Hard Data Packages - Intersil Power Transistors**

**TXV Equivalent**

**1. Rad Hard TXV Equivalent - Standard Data Package**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
- F. Group C - Attributes Data Sheet
- G. Group D - Attributes Data Sheet

**2. Rad Hard TXV Equivalent - Optional Data Package**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
  - Precondition Lot Traveler
  - Pre and Post Burn-In Read and Record Data
- D. Group A - Attributes Data Sheet
  - Group A Lot Traveler
- E. Group B - Attributes Data Sheet
  - Group B Lot Traveler
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
  - Bond Strength Data (Subgroup B3)
  - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
- F. Group C - Attributes Data Sheet
  - Group C Lot Traveler
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
  - Bond Strength Data (Subgroup C6)
- G. Group D - Attributes Data Sheet
  - Group D Lot Traveler
  - Pre and Post RAD Read and Record Data

- E. Preconditioning Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data

- F. Group A - Attributes Data Sheet
- G. Group B - Attributes Data Sheet
- H. Group C - Attributes Data Sheet
- I. Group D - Attributes Data Sheet

**2. Rad Hard Max. "S" Equivalent - Optional Data Package**

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
  - X-Ray and X-Ray Report
- F. Group A - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Subgroups A2, A3, A4, A5 and A7 Data
- G. Group B - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Subgroups B1, B3, B4, B5 and B6 Data
- H. Group C - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Subgroups C1, C2, C3 and C6 Data
- I. Group D - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Pre and Post Radiation Data

**Class S - Equivalents**

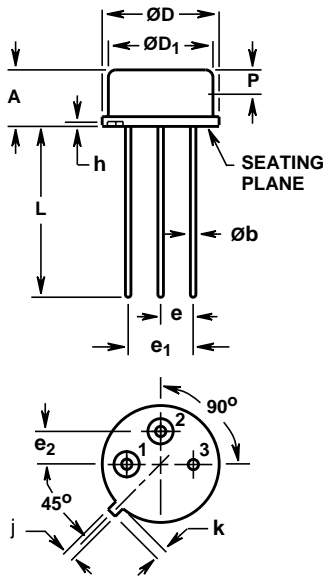
**1. Rad Hard "S" Equivalent - Standard Data Package**

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report

# FRL234D, FRL234R, FRL234H

## TO-205AF

### 3 LEAD JEDEC TO-205AF HERMETIC METAL CAN PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.160	0.180	4.07	4.57	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
ØD <sub>1</sub>	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e <sub>1</sub>	0.190	0.210	4.83	5.33	4
e <sub>2</sub>	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.560	12.70	14.22	3
P	0.075	-	1.91	-	5

#### NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AF outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inches (0.254mm).
6. Lead no. 3 butt welded to stem base.
7. Controlling dimension: Inch.
8. Revision 3 dated 6-94.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

### Sales Office Headquarters

#### NORTH AMERICA

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (407) 724-7000  
FAX: (407) 724-7240

#### EUROPE

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

#### ASIA

Intersil (Taiwan) Ltd.  
Taiwan Limited  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029