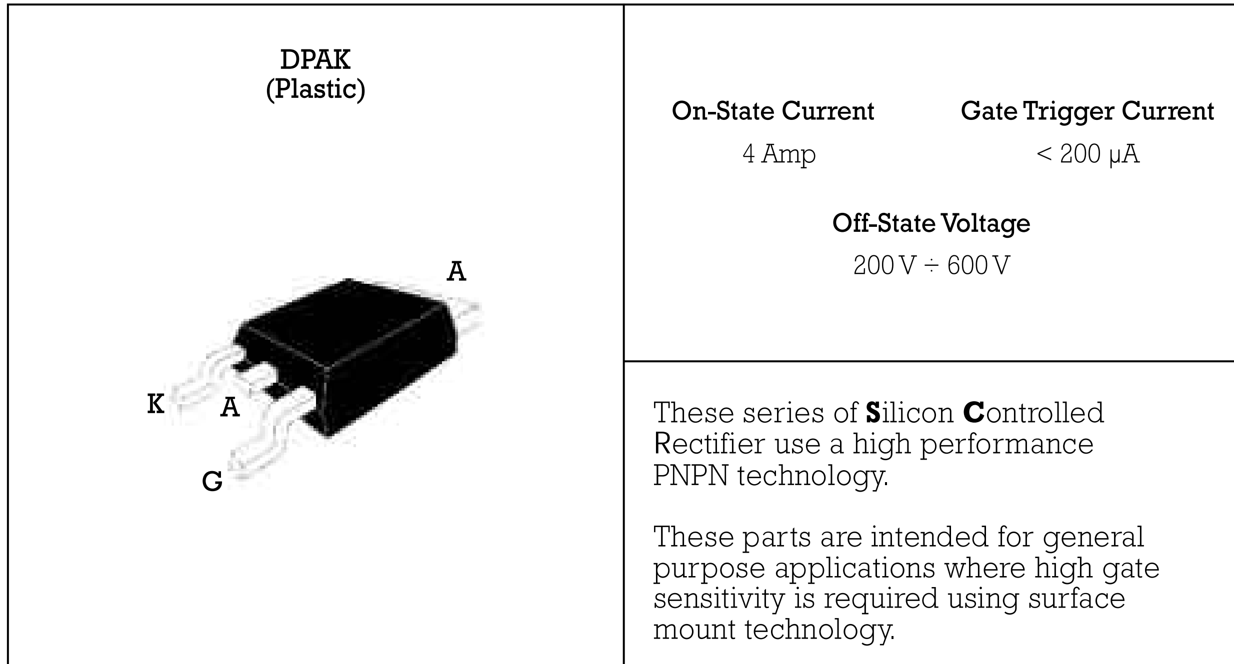
FAGOR

FS04...D

SURFACE MOUNT SCR



On-State Current
4 Amp

Gate Trigger Current
< 200 μA

Off-State Voltage
200 V ÷ 600 V

These series of **S**ilicon **C**ontrolled Rectifier use a high performance PNPN technology.

These parts are intended for general purpose applications where high gate sensitivity is required using surface mount technology.

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, T_C = 115 °C	4		A
$I_{T(AV)}$	Average On-State Current	Half Cycle, =180°, T_C = 115 °C	2.5		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	33		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz	30		A
I^2t	Fusing Current	t = 10 ms, Half Cycle	4.5		A^2s
V_{GRM}	Peak Reverse Gate Voltage	I_{GR} = 10μA	8		V
I_{GM}	Peak Gate Current	20 μs max.		1.2	A
P_{GM}	Peak Gate Dissipation	20 μs max.		3	W
$P_{G(AV)}$	Gate Dissipation	20 ms max.		0.2	W
T_j	Operating Temperature		-40	+125	°C
T_{stg}	Storage Temperature		-40	+150	°C
T_{sld}	Soldering Temperature	10s max		260	°C

SYMBOL	PARAMETER	CONDITIONS	VOLTAGE			Unit
			B	D	M	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	R_{GK} = 1 K	200	400	600	V

SURFACE MOUNT SCR

Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS		SENSITIVITY 01	04	02	03	Unit
I_{GT}	Gate Trigger Current	V_D = 12 V_{DC} , R_L = 33 . T_j = 25 °C	MIN	1	15		20	μA
			MAX	20	50	200	200	
I_{DRM} / I_{RRM}	Off-State Leakage Current	V_D = V_{DRM} , R_{GK} = 220 , V_R = V_{RRM} , | T_j = 125 °C	MAX	1				mA
		| T_j = 25 °C	MAX	5				μA
V_{TM}	On-state Voltage	at I_T = 8 Amp, tp = 380 μs, T_j = 25 °C	MAX	1.6				V
V_{GT}	Gate Trigger Voltage	V_D = 12 V_{DC} , R_L = 33 , T_j = 25 °C	MAX	0.8				V
V_{GD}	Gate Non Trigger Voltage	V_D =V_{DRM}, R_L = 3.3 K , R_{GK} = 220 T_j = 125 °C	MIN	0.1				V
I_H	Holding Current	I_T = 50 mA , R_{GK} = 1K , T_j = 25 °C	MAX	5				mA
I_L	Latching Current	I_G = 1 mA , R_{GK} = 1K , T_j = 25 °C	MAX	6				mA
dv / dt	Critical Rate of Voltage Rise	V_D = 0.67 x V_{DRM} , R_{GK} = 220 , T_j = 125 °C	MIN	10	10	5	10	V/μs
di / dt	Critical Rate of Current Rise	I_G = 2 x I_{GT} Tr 100 ns, F = 60 Hz, T_j = 125 °C	MIN	50				A/μs
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC			3				°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Amb (S=0.5 cm^2)			70				°C/W

PART NUMBER INFORMATION

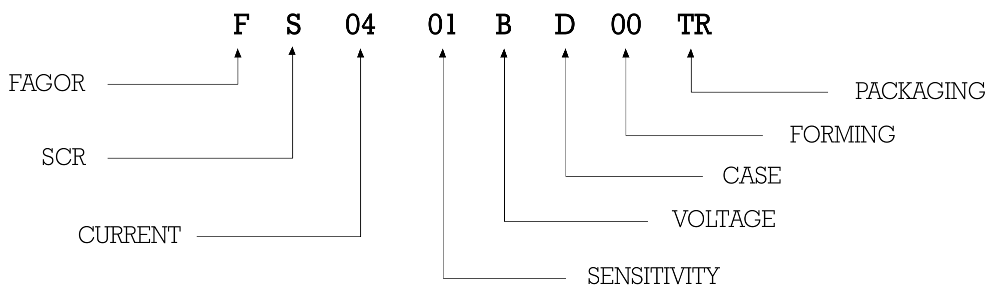


Fig. 1: Maximum average power dissipation versus average on-state current

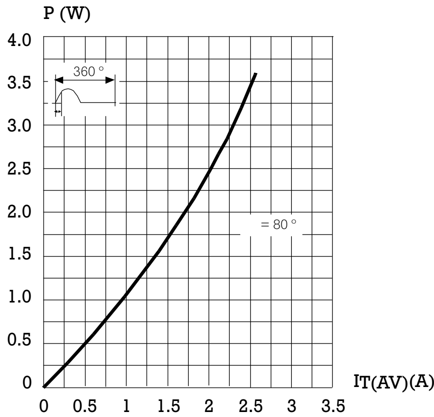


Fig. 2: Correlation between maximum average power dissipation and maximum allowable temperatures (Tamb and T case) for different thermal resistances heatsink+contact.

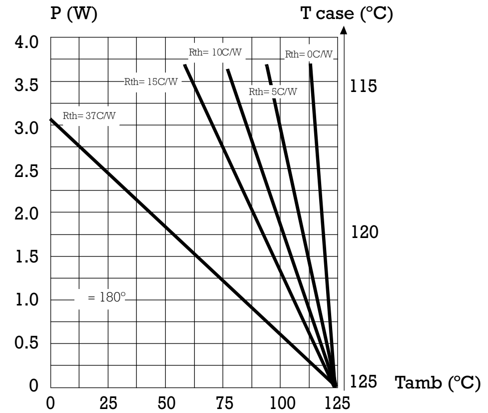


Fig. 3: Average and DC on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout)

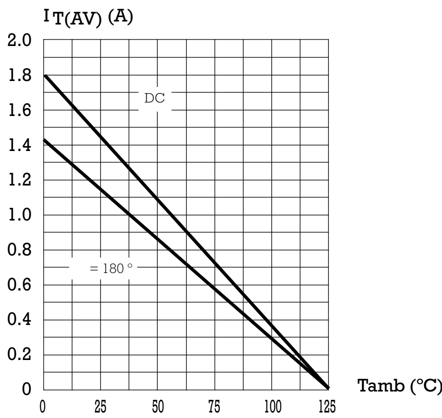


Fig. 4-1: Relative variation of thermal impedance junction to case versus pulse duration.

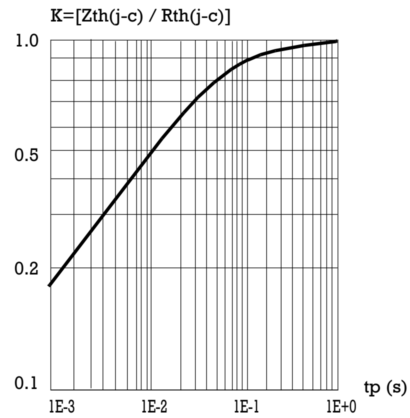


Fig. 4-2: Relative variation of thermal impedance junction to ambient versus pulse duration. (recommended pad layout)

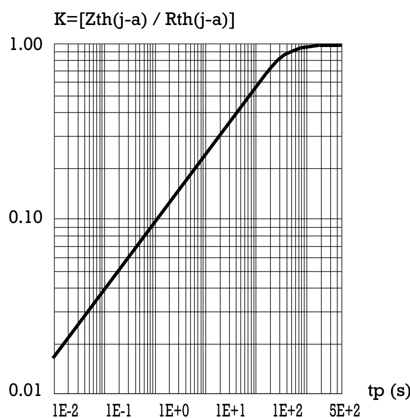
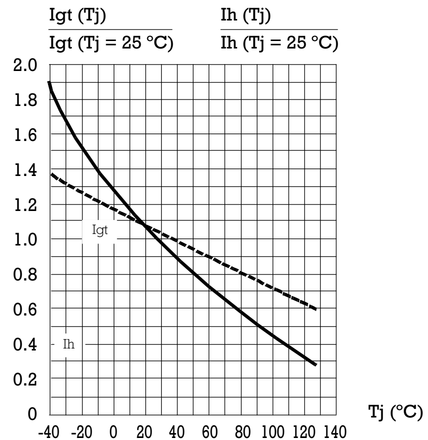


Fig. 5: Relative variation of gate trigger current and holding current versus junction temperature.



SURFACE MOUNT SCR

Fig. 6: Non repetitive surge peak on-state current versus number of cycles.

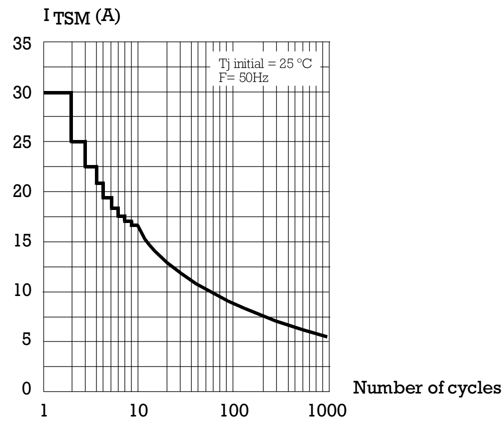


Fig. 7: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp <10 ms, and corresponding value of I^2t.

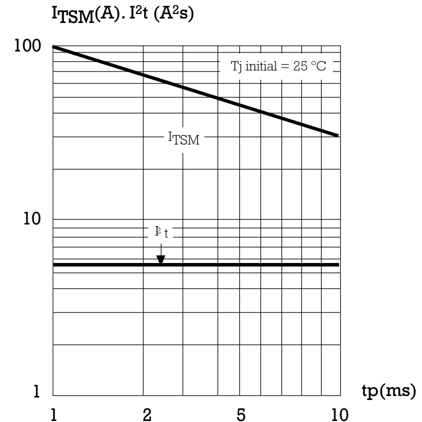


Fig. 8: On-state characteristics (maximum values).

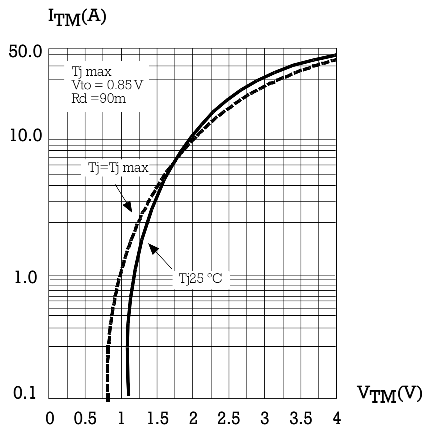


Fig. 9: Thermal resistance junction to ambient versus copper surface under tab (Epoxy printed circuit board FR4, copper thickness: 35µm).

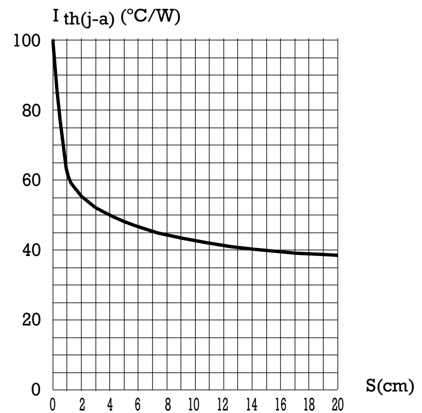
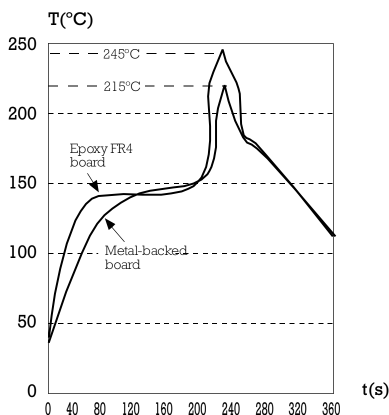


Fig. 10: Typical reflow soldering heat profile, either for mounting on FR4 or metal-backed boards.



PACKAGE MECHANICAL DATA DPAK TO 252-AA

REF.	DIMENSIONS		
	Milimeters		
	Min.	Nominal	Max.
A	2.18	2.3±0.18	2.39
A1	0	0.12	0.127
b	0.64	0.75±0.1	0.89
c	0.46		0.61
c1	0.46		0.56
c2		0.8±0.013	
D	5.97	6.1±0.1	6.22
D1	5.21		5.52
E	6.35	6.58±0.14	6.73
E1	5.20	5.36±0.1	5.46
e		2.28BSC	
H	9.40	9.90±0.15	10.41
L	1.40		1.78
L1	2.55	2.6±0.05	2.74
L2	0.46	0.5±0.013	0.58
L3	0.89	1.20±0.05	1.27
L4	0.64	0.83±0.1	1.02

Marking: type number
Weight: 0.2 g

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