FS1610
Advanced Power Management Controller

Leading the Digital Power Revolution ™

GENERAL DESCRIPTION

FyreStorm's FS1610 Advanced Power Management Controller utilizes proprietary digital technology to provide a fully programmable power subsystem solution for sophisticated mobile devices such as digital still cameras, feature-phones, smart-phones, PDAs and hand-held computers. Compared to traditional implementations, an FS1610 based solution reduces PCB area, and its digital technology, which allows full programmability, results in faster design cycles, allowing quicker time-to-market for the end product. It reduces glue logic by interfacing seamlessly to processors such as Intel's PXA family, Freescale Semiconductor's MX families, Samsung's ARM9-based family and AMD's Au1200 family.

The FS1610 provides eight highly efficient switch-mode converters (three buck converters, one White LED driver, three boost converters and one buck-boost converter) and has integrated drivers that directly drive external MOSFETs. A patented digital control algorithm reduces capacitor and inductor size and cost, reduces quiescent current and improves conversion efficiency. Additionally, the FS1610 provides three low-power LDO regulators with internal pass FETs, a Real-Time-Clock with a programmable alarm and a Watchdog Timer.

Start-up configuration of the device is stored in an internal EEPROM that can be programmed by the user, and can then be managed by the host processor via the device's I^2C or UART serial port. Load activation and shedding profiles can also be specified in the EEPROM and by the host. The FS1610 is also capable of stand-alone operation using the parameters loaded from the EEPROM at start-up.

The FS1610 is provided in a space-efficient, 8 x 8 FBGA package.

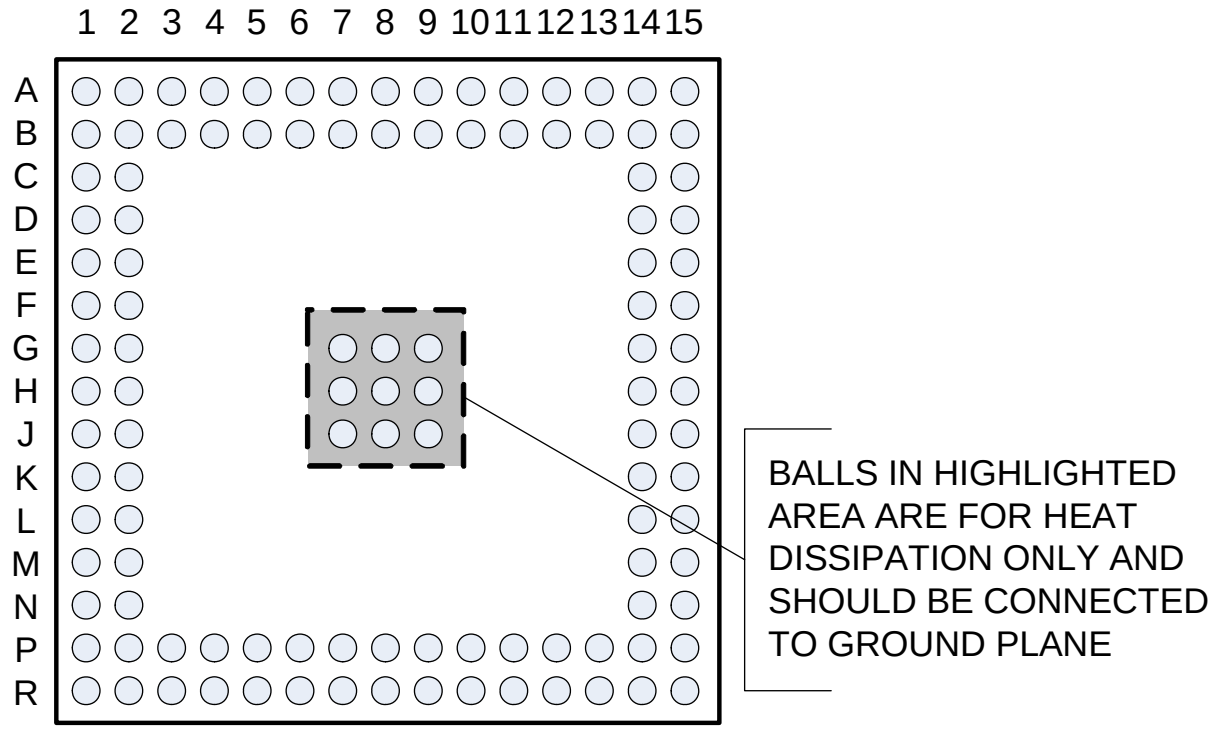
APPLICATIONS

- **Feature phones and smart phones**
- **Portable media players and MP3 players**
- **PDAs and hand-held computers**
- **Digital still cameras and camcorders**
- **Other portable electronics equipment**

KEY FEATURES

- **Eight switching converters**
  - Three buck (step-down) converters
    - Two converters available in Low Power mode for high efficiency at low load currents
  - Three boost (step-up) converters
  - One buck-boost (step-up) converter for negative output voltage
  - One constant current boost White LED driver
  - High efficiency (typically 90%+) from 5% to 100% of programmed maximum current in active mode
  - Converters drive external MOSFET(s) directly
- **Switching converters feature all-digital loop control technology**
  - Real-time analysis provides optimal power system control and operation
  - Precise supply-to-supply matching and tracking
  - Programmable power-up and -down slew rates
  - Programmable load connection and shedding
  - Reduced component count yields smaller size and lower cost
- **Three LDOs**
- **Input voltage range: 2.8 to 5.5 Volts**
- **Battery backup switching support**
- **Dynamic programming for all buck and LDO power rails**
- **Power-up supply characteristics can be modified without hardware changes by reprogramming the device's EEPROM**
  - Fast and simple design with FyreStorm's Web-based Design Center
- **Capable of stand-alone operation using the parameters loaded from the EEPROM at start-up**
  - No serial interface with host required
  - Utilize device pins for status/control
- **Integrated system support**
  - Real time clock with alarm and Watchdog timer
  - Programmable host controller interrupt output
  - Power Good and Power-on-Reset outputs
- **Remote management via I^2C or UART interface to host processor**
- **Operates from a low-cost 32.768 KHz crystal or external clock input**
  - Provides buffered 32 KHz output to the system
- **Low power consumption**
  - 50 µA in shutdown mode with RTC enabled
- **128 bytes user data space in EEPROM**
- **8 x 8 mm FBGA package with 0.5 mm ball pitch**

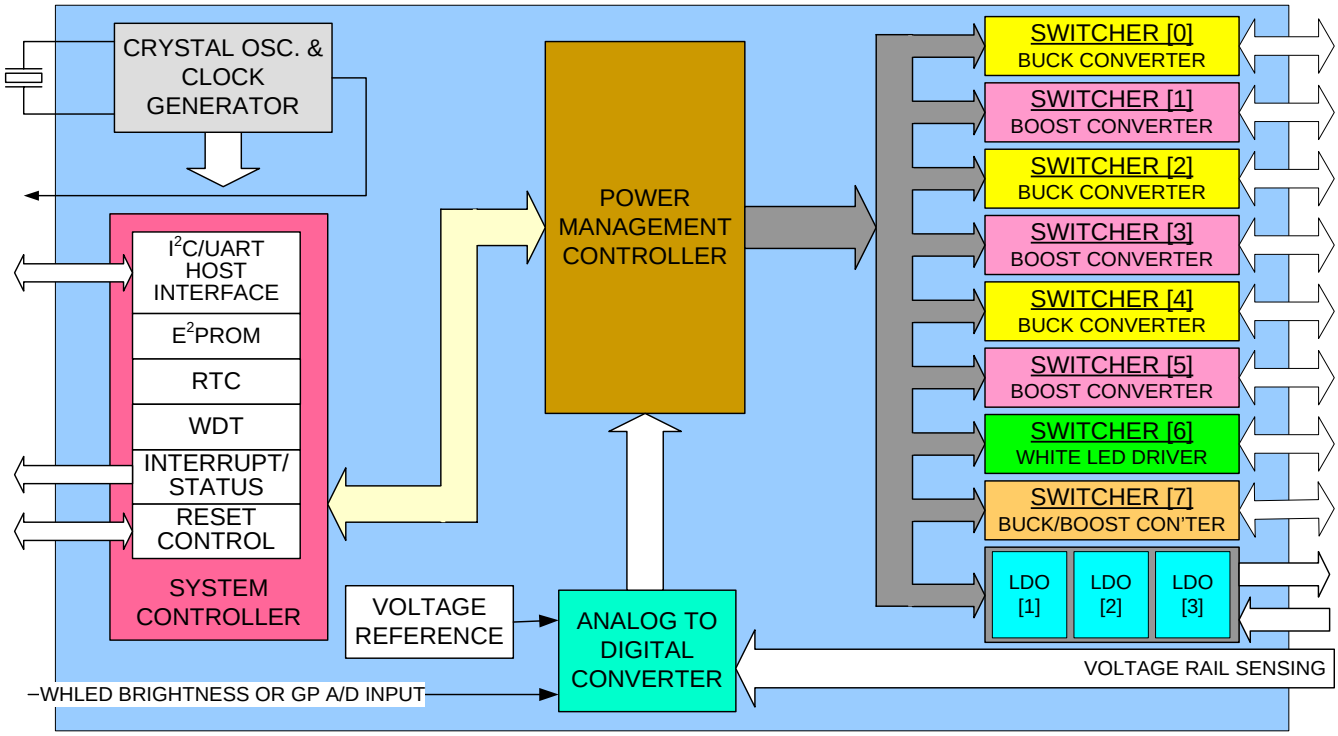
FS1610 PIN CONFIGURATION



FS1610 Pin Configuration – Top View, Looking Through Package

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	PWREN[1]	B7	BATBU	F1	LDO[1]	L2	HSENB[7]	P11	nEXTON
A2	X1	B8	VBAT	F2	GNDLDO[1]	L14	HSD[2]	P12	V_EEPROM
A3	X2	B9	MFP[2]	F14	VRET[3]	L15	VIN[2]	P13	ADPTR_DET
A4	CLKOUT	B10	POK	F15	LSD[3]	M1	HSENA[7]	P14	LSD[0]
A5	ADPTR_IN	B11	PWREN[2]	G1	VINLDO[1]	M2	LSEN[7]	P15	VRET[0]
A6	VIN	B12	PWREN[3]	G2	N/C	M14	LSD[2]	R1	DNC
A7	GND	B13	DVSS	G14	VIN[31]	M15	VRET[2]	R2	HSEN[4]
A8	VMAIN	B14	HSD[7]	G15	LSD[1]	N1	HSEN[6]	R3	N/C
A9	MFP[5]	B15	VRET[7]	H1	AVDD	N2	LSEN[6]	R4	HSEN[3]
A10	nRSTO	C1	VINLDO[3]	H2	AVSS	N14	HSD[0]	R5	HSEN[2]
A11	DVDD	C2	N/C	H14	N/C	N15	VIN[0]	R6	HSEN[1]
A12	BLCTL_D	C14	VRET[6]	H15	VRET[1]	P1	HSEN[5]	R7	HSEN[0]
A13	MFP[1]	C15	LSD[6]	J1	VINSENH	P2	LSEN[5]	R8	SDDIS[3]
A14	MFP[4]	D1	LDO[2]	J2	VINSENL	P3	LSEN[4]	R9	SDDIS[6]
A15	MFP[3]	D2	GNDLDO[2]	J14	HSD[4]	P4	LSEN[3]	R10	nRSTI
B1	LDO[3]	D14	VIN[7]	J15	VIN[4]	P5	LSEN[2]	R11	nDB
B2	GNDLDO[3]	D15	VIN[65]	K1	BLCTL_A	P6	LSEN[1]	R12	EE_SDA
B3	RTCVDD	E1	VINLDO[2]	K2	DAS_BYP1	P7	LSEN[0]	R13	EE_SCL
B4	RTCVSS	E2	VBIAS_LDO2	K14	LSD[4]	P8	SDDIS[1]	R14	TEST[2]
B5	DBOUT	E14	VRET[5]	K15	VRET[4]	P9	SDDIS[5]	R15	TEST[1]
B6	SW[2]IN	E15	LSD[5]	L1	DAS_BYP2	P10	nIRSTO		

FS1610 BLOCK DIAGRAM



CONVENTIONS

Unless otherwise noted, a positive logic (active High) convention is assumed throughout this document, whereby a positive voltage (V_{IH}) causes assertion of an input signal and indicates an asserted output signal. An 'n' preceding the signal name, e.g., nINTR, indicates that the input or output signal is asserted in a Low state (V_{IL}). Whenever a signal is separated into numbered bits, e.g., D[7], D[6], ..., D[0], the family of bits may also be shown collectively, e.g., as D[7:0].

The designation 0xNNNN indicates a number expressed in hexadecimal notation (N = 0, 1, 2, . . . , 9, A, . . , E, F). The designation 0bXXXX indicates a number expressed in binary notation (X = 0, 1).

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Parameter	Min	Max	Unit
Input voltage, all analog and power input pins except ADPTR_IN	– 0.3	+ 6	V
Input voltage, ADPTR_IN pin	– 0.3	+ 6	V
Input voltage, all digital input and output pins	– 0.3	+ 4.0	V
Input voltage, HSEN[7:0], LSEN[7:0]	– 0.3	+ 6	V
Continuous current, pins LSD[0], HSD[0], LSD[2], HSD[2], LSD[4], HSD[4]	- 25	25	mA
Continuous current, pins LSD[1], LSD[3], LSD[5], LSD[6], HSD[7]	- 25	25	mA
Continuous power dissipation		0.7	W
Junction temperature		+ 125	°C
Operating ambient temperature range	– 20	+ 85	°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Electrical Parameters - General

T_A = – 20°C to 85°C unless otherwise noted. Typical values are at T_A = +25°C and VIN = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INP}	Input voltage: VMAIN, VIN, VIN[0], VIN[2], VIN[4], VIN[7], VIN[31], VIN[65], VBIAS_LDO2 [4]		2.8		5.5	V
	Input voltage VINLDO[3, 1]		1.8		VIN	
	Input voltage VINLDO[2]		1.8		VBIAS_LDO2	
	Input voltage ADPTR_IN		0		5.8	
	Input voltage V_EEPROM	Not connected for normal operation	1.8	2.5	3.3	
V_{BU}	Input voltage, BATBU		2.75		5.5	V
$V_{SW[2]IN}$	Input voltage, SW[2]IN		0		VIN	V
	Operating Current VMAIN				2	µA
	Operating current BATBU	SHUTDOWN state, CLKOUT disabled, I_{VBAT} = 0		50		µA
	Operating current VIN	LOWPOWER – SW[2, 0] enabled, no loads		150		µA
		SHUTDOWN		5		µA
		READY		4		mA
t_{READY}	SHUTDOWN to READY state delay [3]				200	ms
t_{RSTI}	nRSTI input debounce time [2, 3]	nRSTI de-asserted		100		ms
t_{EXTON}	nEXTON input debounce time [2, 3]	nEXTON asserted or de-asserted		100		ms
t_{RSTO}	nRSTO timer period (programmable in EEPROM) [3]		0		65,535	ms
t_{IRSTO}	nIRSTO timer period [3]	nRSTI asserted		65		ms
V_{DBTH}	Dead battery threshold programming range [1]		2.70	3.10	3.30	V
	Dead Battery detect threshold programming resolution			50		mV
	Dead Battery detect threshold accuracy	VMAIN decreasing	-2		2	%
V_{DBHYS}	Dead Battery detect comparator hysteresis	VMAIN increasing	<tbd>	150		mV
V_{LBTH}	Low battery threshold programming range		0		5.5	V
	Low Battery detect threshold programming resolution	ACTIVE		1.34		mV
		LOWPOWER		85		
	Low Battery detect threshold accuracy		-0.5		0.5	%
V_{DBOH}	DBOUT output-High voltage	I_O = 100 µA	VIN – 0.1			V
V_{DBOL}	DBOUT output-Low voltage	I_O = -100 µA			0.1	V
	ADPTR_IN detect threshold voltage	ADPTR_IN increasing	VMAIN		VMAIN + 0.2	V
	ADPTR_IN detect comparator hysteresis	ADPTR_IN decreasing	<tbd>	150		mV
T_{ADPT}	ADPTR_IN detect debounce time [2, 3]	ADPTR_IN asserted		100		ms
	Thermal Sensor Accuracy	Junction temperature	-10		10	ºC
T_{TAL}	Thermal alarm threshold (based on thermal sensor accuracy)	Temperature rising		105		ºC
		Temperature falling		95		ºC
T_{TSD}	Thermal shutdown threshold (based on thermal sensor accuracy)			115		ºC
Logic Level Signals						
	Output-Low voltage: All digital outputs	I_{OL} = -4 mA			0.4	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Output-High voltage: All digital outputs, unless otherwise specified	When configured as active outputs, I_{OH} = 4 mA	2.0		2.4	V
		When configured as open-drain output			3.75	V
	Output-High voltage: CLKOUT	I_{OH} = 1 mA, C_O = 50 pF	2.0		2.4	V
V_{IH}	Input-High voltage: All digital inputs		1.6		3.75	V
V_{IL}	Input-Low voltage: All digital inputs				0.4	V
	Input leakage current: All digital inputs except nRSTI and nEXTON	Input voltage = 3.6 V	– 1		+ 1	µA
		Input voltage = 0 V	– 1		+ 1	µA
	Output-High leakage current: All open-drain outputs	Output voltage = 3.6 V			0.2	µA
	Input leakage current: nRSTI and nEXTON	Input voltage = 2.5 V	– 1		+ 1	µA
		Input voltage = 0 V	62	125	150	µA

1. V_{DBTH} is set to a default value of 3.10 V during the internal power-on-reset cycle. It may then be changed by data in the EEPROM.
2. Debounce interval is measured from the last bounce detected.
3. Based on 32.768 KHz crystal frequency
4. VIN, VIN[0], VIN[2], VIN[4], VIN[7], VIN[31], VIN[65] must be at the same voltage

Electrical Parameters – LDO Regulators

VIN = 3.0 V – 5.5 V, T_A = – 20°C to 85°C unless otherwise noted. Typical values are at T_A = +25°C and VIN = 3.6V. C_{OUT} = 0.47 µF unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO[1], LDO[3]						
	Output voltage programming range		0.9		3.3	V
	Output voltage programming resolution			50		mV
	Initial voltage accuracy	I_{OUT} = 0	- 0.5		0.5	%
	Output voltage change under load	I_{OUT} = 0 to 60 mA, C_{OUT} = 2.2 µF, X5R		- 35	- 50	mV
	Dropout voltage	I_{OUT} = 60 mA		200	<tbd>	mV
	Maximum output current [1]		60			mA
	Quiescent current, VINLDO[x]	No load			1	µA
	Quiescent current, VIN	Enabled, no load		45	tbd	µA
		LDO disabled			1	µA
V_{PG}	POK threshold	Rising		95		%
		Falling		90		%
t_{FLT}	POK response time to out of regulation programming range		1		255	ms
	External output capacitor	R_{ESR} < 50 mΩ L_{ESL} < 3 nH 1 Mhz < f < 50 MHz	470	1000	2200	nF
	PSRR	f =10 KHz, I_{OUT} = 60 mA	40			db
		f =100 KHz, I_{OUT} = 60 mA	30			db
LDO[2]						
	Output voltage programming range		0.9		3.3	V
	Output voltage programming resolution			50		mV
	Initial voltage accuracy	I_{OUT} = 0	- 0.5		0.5	%
	Output voltage change under load	I_{OUT} = 0 to 60 mA, C_{OUT} = 2.2 µF, X5R		- 35	- 50	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Dropout voltage	I_{OUT} = 60 mA		200	<tbd>	mV
	Maximum output current [1]		60			mA
	Noise	VBIAS_LDO2 = 3.3V 10 Hz < f < 100 KHz		20	<tbd>	µV RMS
	Quiescent current, VINLDO[2]	No load			1	µA
	Quiescent current, VBIAS_LDO2	Enabled, no load		45	tbd	µA
		LDO disabled			1	µA
V_{PG}	POK threshold	Rising		95		%
		Falling		90		%
t_{FLT}	POK response time to out of regulation programming range		1		255	ms
	External output capacitor	R_{ESR} < 50 mΩ L_{ESL} < 3 nH 1 Mhz < f < 50 MHz	470	1000	2200	nF
	PSRR	f =10 KHz, I_{OUT} = 60 mA	40			db
		f =100 KHz, I_{OUT} = 60 mA	30			db

1. The aggregate internal power dissipation for all LDOs combined must not exceed 500 mW.

Electrical Parameters – Switching Regulators

VIN = 3.0 V – 5.5 V, T_A = – 20°C to 85°C unless otherwise noted. Typical values are at T_A = +25°C and VIN = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Constant Current Boost Regulator: SW[6]						
I_{LED}	Maximum output current		30			mA
	Output current programming resolution			1.0		mA
	Output current accuracy	I_{LED} = 20 mA	<tbd>	±8	<tbd>	%
	Number of series LEDs	V_{LED} = 4.1V max.	2		10	Units
	Over-voltage protection threshold accuracy		– 5		5	%
	LSD[6] RDS_{ON}	Output current = 25 mA		4.8	6.3	Ohm
		Output current = – 25 mA		2.4	3.1	Ohm
	Input leakage current: HSEN[6], LSEN[6]			±1	<tbd>	µA
	Output-Low voltage, SDDIS[6] output	I_{OL} = 0.1 mA			5	mV
f_{SW6}	Switching frequency				8 x f_{CLK}	Hz
	Incremental operating current, VIN	SW[6] enabled, I_{LED} = 30 mA		2		mA
	Incremental supply current at VIN[65]	SW[6] enabled, I_{LED} = 30 mA		100		µA
	BLCTL_D input PWM frequency			100	500	Hz
	Output sequencing turn-off threshold	Output is disabled	VIN			V
I_{PG}	POK threshold		90			%
	POK response time to out of regulation programming range		1		255	ms
Synchronous Buck Regulators: SW[0], SW[2], SW[4]						
	Output voltage programming range		0.85		3.3	V
	Output voltage programming resolution			5		mV
	Output voltage accuracy	I_{OUT} = 0 to 300 mA, includes line and load regulation	– 2.5		0.5	%
	DVM voltage step size (EEPROM configurable)		5		300	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	DVM voltage step time (EEPROM configurable)		$T_{CLK}/4$		31 x $T_{CLK}/4$	µs
f_{SW0}	Switching frequency				$16f_{CLK}$	KHz
	Incremental operating current at VIN pin	SW[x] enabled, static load, ACTIVE mode		1		mA
	Supply current at VIN[x] pin	SW[x] enabled, switching at maximum f_{SW0}		200		µA
	Input leakage current: HSEN[4, 2, 0], LSEN[4, 2, 0]			±1	<tbd>	µA
	Output impedance: HSD[4, 2, 0]	Output current = 25 mA		2.4	3.1	Ohm
		Output current = – 25 mA		4.8	6.3	Ohm
	Output impedance: LSD[4, 2, 0]	Output current = 25 mA		4.8	6.3	Ohm
		Output current = – 25 mA		2.4	3.1	Ohm
	Current limit as percentage of programmed output		<tbd>		<tbd>	%
V_{PG}	POK threshold		97.5			%
	POK response time to out of regulation programming range		1		255	ms
	Output sequencing turn-off threshold (EEPROM programmable)	Output is disabled		500		mV
Boost Regulators: SW[1], SW[3], SW[5], Buck-Boost Regulator SW[7]						
	Output voltage programming range SW[5, 3, 1]		VIN		25.0	V
	Output voltage programming range SW[7]		-1.0		-20.0	V
	Output Voltage Accuracy	Output current 0 - 30 mA	-0.5		0.5	%
	Output voltage programming resolution	Of programmed range			0.1	%
	Output impedance: LSD[5, 3, 1]	Output current = 25 mA		4.8	6.3	Ohm
		Output current = – 25 mA		2.4	3.1	Ohm
	Output impedance: HSD[7]	Output current = 25 mA		2.4	3.1	Ohm
		Output current = – 25 mA		4.8	6.3	Ohm
	Input leakage current: HSEN[A7, B7, 5, 3, 1], LSEN[7, 5, 3, 1]			±1	<tbd>	µA
	Output-Low voltage: SDDIS[5, 3, 1] outputs	I_{OL} = 0.1 mA			5	mV
	Switching frequency				$8f_{CLK}$	KHz
	Incremental operating current at VIN pin (SW[5,3,1])	Rail enabled, static load		350		µA
	Incremental operating current at VIN pin (SW[7])	Rail enabled, static load		500		µA
	Incremental supply current at VIN[xy] pin	Rail enabled, switching at maximum f_{SW}		50		µA
	Current-limit as percentage of programmed output			150		%
V_{PG}	POK threshold			97.5		%
	POK response time to out of regulation programming range		1		255	ms
	Output sequencing turn-off threshold	Output is disabled	VIN			V

Electrical Parameters – BLCTL_A Input

VIN = 3.0 V – 5.5 V, T_A = – 20°C to 85°C unless otherwise noted. Typical values are at T_A = +25°C and VIN = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Input voltage		0		VIN	V
	Measurement data quantization (Range is EEPROM programmable)	Range: 0 – 1.375 V		<tbd>		mV
		Range: 0 – 2.75 V		<tbd>		
		Range: 0 – 5.5 V		<tbd>		
	Measurement data accuracy		- 0.5		0.5	%

Electrical Parameters – VBAT Switch [1]

VIN = 3.0 V – 5.5 V, T_A = – 20°C to 85°C unless otherwise noted. Typical values are at T_A = +25°C and VIN = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Output voltage, VBAT	SW[2] on and in regulation		$V_{SW[2]IN}$		V
		SW[2] off or out of regulation		V_{BATBU}		V
	VBAT switch voltage drop	I_{OUT} = 20 mA, V_{BATBU} and V_{SW2IN} = 3.0 V		100	200	mV
	VBAT output current				30	mA

1. 'VBAT Switch' is the internal SPDT switch that connects BATBU or SW[2]IN to the VBAT output.

AC Electrical Parameters

VINA = VIND = 3.0 V – 5.5 V, T_A = – 20°C to 85°C unless otherwise noted. Typical values are at T_A = +25°C and VINA = VIND = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I^2C Serial Interface Timing						
	Clock frequency		0		400	KHz
	Bus-free time between START and STOP		1.3			µs
	SCL low Period		1.3			µs
	SCL high Period		1.0			µs
	SDA hold Time		0			µs
	SDA setup Time		100			ns
	STOP condition setup time		1.0			µs
	Repeated START condition setup time		1.0			µs
Real-Time-Clock Timing						
	Granularity		1			s
	Span				10	years
	Alarm Setting Accuracy		0		1	s
	Alarm latency	Alarm triggered to nINTR output asserted			200	ms
Watch-dog Timer Timing						
	Interval range		0.05		32	s
	Granularity		5			ms
	Latency	Alarm triggered to nINTR output asserted			5	ms
	Watchdog reset input pulse width		100			ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal Oscillator Input						
f_{CLK}	Crystal Frequency [1]		30	32.768	32.8	KHz
T_{CLK}	Clock period		30.488	30.158	33.333	µs
	V_{IH}, X1 input		1.6	2.0	2.8	V
	V_{IL}, X1 input		-0.3	0.4	0.6	V
	Input leakage, X1			0.1	1	µA
	External Capacitance, X1 and X2			18		pF
	Stabilization time				1	s

1. For accurate timekeeping with the RTC and WDT, a crystal frequency of 32.768 KHz ± 100 ppm should be used.

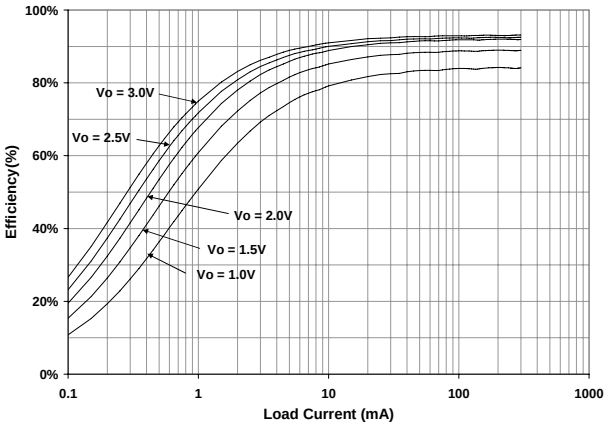


Figure 1. Typical Buck Converter Efficiency, Normal Mode, Vin = 3.9V

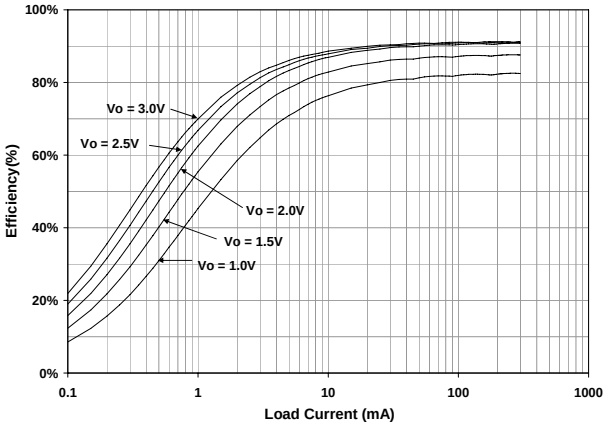


Figure 2. Typical Buck Converter Efficiency, Normal Mode, Vin = 5.0V

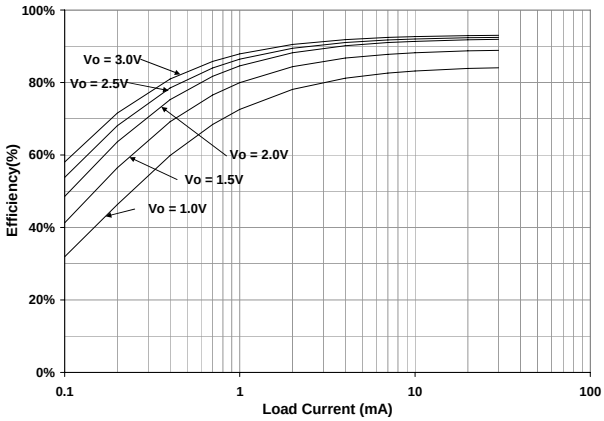


Figure 3. Typical Buck Converter Efficiency, Low Power Mode, Vin = 3.9V

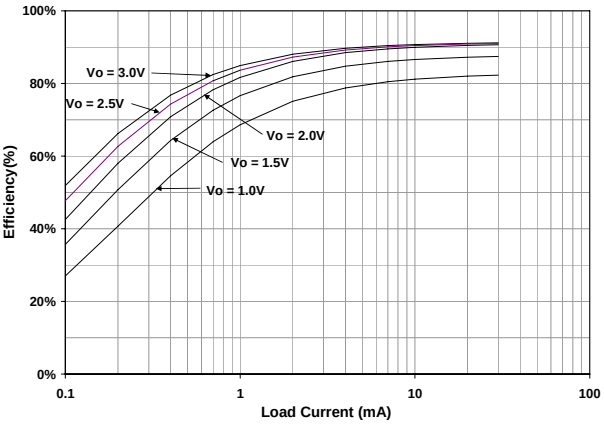


Figure 4. Typical Buck Converter Efficiency, Low Power Mode, VIN = 5.0V

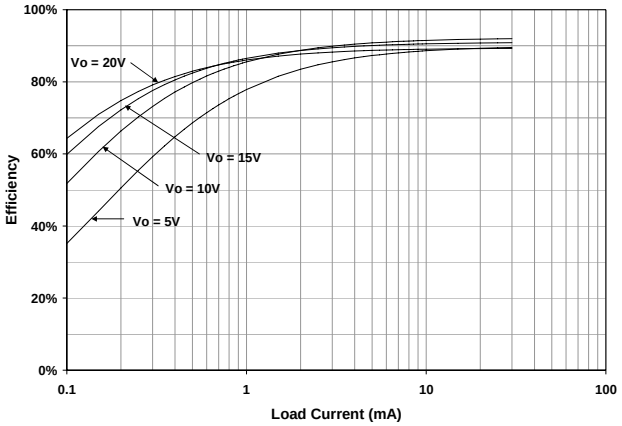


Figure 5. Typical Boost Converter Efficiency, VIN = 3.9V

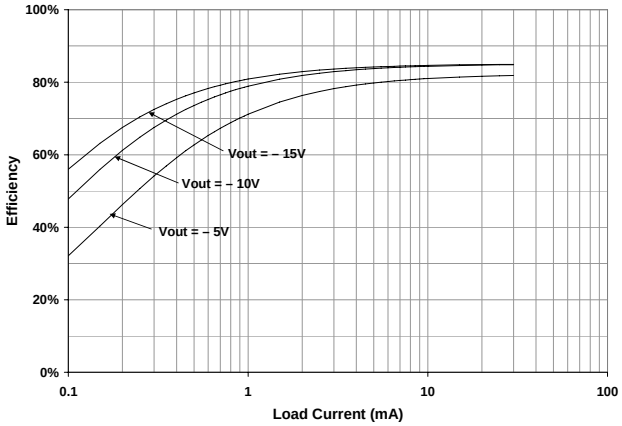


Figure 7. Typical Buck-Boost Converter Efficiency, VIN = 3.9V

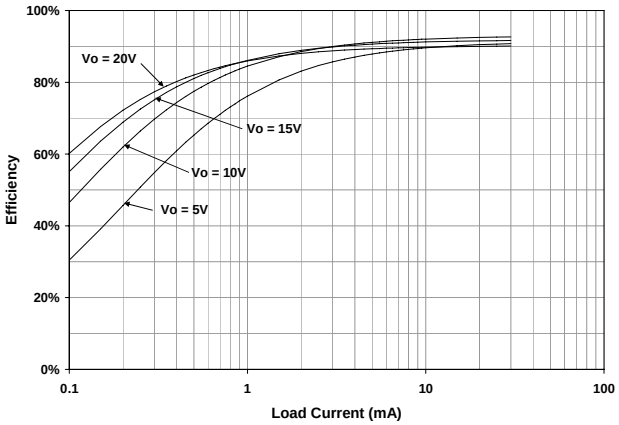


Figure 6. Typical Boost Converter Efficiency, Vin = 5.0V

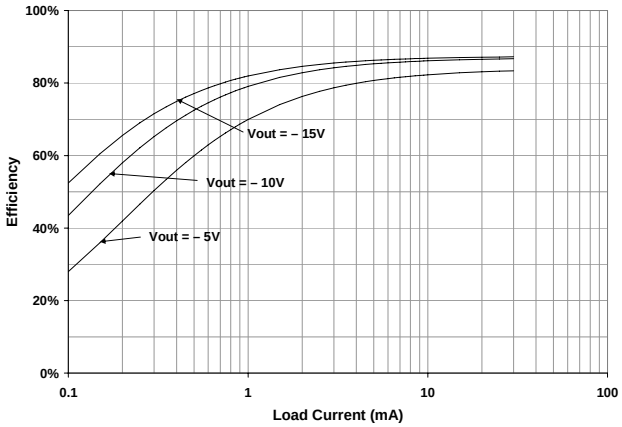


Figure 8. Typical Buck-Boost Converter Efficiency, VIN = 5.0V

PIN DESCRIPTIONS

Pin No.	Type [1]	Name	Description [2]
A2	I	X1	**Crystal or External 32KHz Clock Input.** **Note:** A clock is required for device operation, even if the RTC and/or Watchdog are not used.
A3	O_A	X2	**Crystal Output.**
A4	O	CLKOUT	**32 KHz Output.** Configurable buffered output of the crystal oscillator.
A10	O	nRSTO	**Power-On Reset Output.** nRSTO is asserted during the internal power-on-reset period of the FS1610. See COLD START POWER-ON SEQUENCE. It can be programmed to be asserted during an out-of-regulation condition on any supply or upon an nRSTI event. Refer to Table 1 if not used.
P10	O	nIRSTO	**Intel Power-On Reset Output.** nIRSTO is asserted for t_{IRSTO} during initial power-up. See COLD START POWER-ON SEQUENCE. Connect to nRESET of Intel PXA27x processors. It is also asserted upon an nRSTI active event, if the WDT expires and when the chip transitions to SHUTDOWN state. Refer to Table 1 if not used.
R10	I	nRSTI	**Manual Reset Input.** If this input is asserted, nRSTO and nIRSTO are asserted. These outputs remain asserted until t_{RSTO} and t_{IRSTO}, respectively, after nRSTI is deasserted and the de-bounce interval, t_{RSTI}, is completed. No power rails are modified. An internal pull-up resistor is provided. If driven from logic, it must be driven from an open drain output to prevent reverse leakage current.

Pin No.	Type [1]	Name	Description [2]
B10	O	POK	**Power OK Output.** POK is asserted when all the rails specified in the EEPROM to be monitored by this status signal are above their regulation thresholds. Refer to Table 1 if not used.
P11	I	nEXTON	**External Power On Input**. An internal de-bounce filter and a pull-up resistor are provided. If driven from logic, it must be driven from an open drain output to prevent reverse leakage current.
A5	I_A	ADPTR_IN	**AC Adapter Present.** An input at the specified level indicates that an AC adapter is present.
P13	O	nADPTR_DET	**Adapter Detected Output.** Indicates that presence of an AC adapter has been detected via the ADPTR_IN input. Refer to Table 1 if not used.
B12 B11 A1	I	PWREN[3] PWREN[2] PWREN[1] (Note 3)	**Power Enable [3:1].** Power on/off control for any group of rails can be mapped to be controlled by PWREN[1] or PWREN[2] or PWREN[3]. A low-high transition enables the voltage rail group, a high-low transition disables the group. Once enabled or disabled, a pre-programmed sequencing defined in the configuration EEPROM is activated. (Note 3 does NOT apply to PWREN[1])
A13	I	MFP[1] (Note 3)	**nLOPWR: Low Power Mode Enable Input**. Activates the device's LOWPOWER operating mode. See Low Power Mode.
B9	I/O	MFP[2] (Note 3)	**(Standalone Mode) – nLB: Low Battery Detect Output.** This pin is asserted whenever VIN goes below the low-battery detect threshold. **(I^2C Serial Mode) – SCL: I^2C Clock Input.** **(UART Serial mode) – EXTPEN2: External Power Enable Output.** This output is asserted (HIGH) at the conclusion of the internal power-up boot process, before turning on any power rails, and is de-asserted when the FS1610 transitions to SHUTDOWN state, after all FS1610 power rails are turned off.
A15	I/O	MFP[3] (Note 3)	**(Standalone and I^2C Serial Modes) – PWREN[4]/WDRST/ EXTPEN3: Power Enable 4 Input or Watchdog Timer Reset Input or External Power Enable Output.** The function of this pin is selected via the EEPROM. If configured as PWREN[4], a group of power rails can be mapped via the EEPROM to be enabled/disabled via this input. See **PWREN[3:1**] for additional information. If configured as WDRST, any transition on this input will reset the Watchdog Timer and restart the programmed time-out interval. If configured as External Power Enable, the output is asserted (HIGH) at the conclusion of the internal power-up boot process, before turning on any power rails, and is de-asserted when the FS1610 transitions to SHUTDOWN state, after all FS1610 power rails are turned off. **(UART Serial mode) – TxD: Serial data output.**
A14	I/O	MFP[4] (Note 3)	**(Standalone Mode) – SD: Shutdown Input.** When asserted, the FS1610 disables all power enable groups (PWREN[5:0]) simultaneously. The sequence of disabling the individual rails within each power enable group is as specified in the EEPROM. Any rails that were enabled by serial commands and are not members of a power enable group are also disabled after all power enable groups have been disabled. **(UART and I^2C Serial Modes) – nINTR: Interrupt Output.** This pin is the output for all internally generated interrupts. A read to the FS1610 via the serial bus provides the status of the interrupt. The interrupts include RTC alarm and Low-battery detect. See HSI User Manual for additional information.
A9	I/O	MFP[5] (Note 3)	**(Standalone Mode) – PWREN[5] [2]: Power Enable 5 input.** A group of power rails can be mapped via the EEPROM to be enabled/disabled via this input. See **PWREN[3:1**] for additional information. **(I^2C Serial Mode) – SDA: I^2C Data Input/Output.** **(UART Serial mode) – RxD: Serial Data Input.**
B7	P	BATBU	**Backup battery input.** A voltage must be present on BATBU in order for the device to operate. Connect a bypass capacitor from this pin to RTCVSS.

Pin No.	Type [1]	Name	Description [2]
B8	P	VBAT	**"Keep Alive" Supply output.** VBAT is the first supply to be active and the last to power-off. It is compliant with the Intel PXA27x specifications. VBAT = VINSW[2] if SW[2] is enabled and within regulation VBAT = BATBU if SW[2] is disabled or out of regulation See COLD START POWER-ON SEQUENCE for additional information.
R11	O	nDB	**Dead Battery Output.** This pin is asserted when VMAIN is below the 'dead battery' threshold and an AC adapter is not present. This pin typically connects to the 'Battery Fault' host processor input. Refer to Table 1 if not used.
B5	O_A	DBOUT	**Disconnect Battery Output, active-high.** This output is asserted when a DB threshold is detected at VMAIN (unless in ACTIVE mode) or if the presence of an AC adapter is detected at ADPTR_IN. It is meant to connect to an external P-channel FET switch to disconnect the main battery.
A8	I_A	VMAIN	**Main Battery Comparator Input.** Used to directly monitor the main battery for a dead-battery condition. See Figure 21.
A6	P	VIN	**Power Supply Input.** Main power supply input
J1	I_A	VINSENH	**Main Supply Input Sense.**
J2	I_A	VINSENL	**Main Supply Return Sense.**
A7	P	GND	**Main Supply Return.**
G1	P	VINLDO[1]	**LDO[1] Supply Input.**
F2	P	GNDLDO[1]	**LDO[1] Supply Return.**
F1	P	LDO[1]	**LDO[1] Output.**
E1	P	VINLDO[2]	**LDO[2] Supply Input.**
D2	P	GNDLDO[2]	**LDO[2] Supply Return.**
D1	P	LDO[2]	**LDO[2] Output.**
E2	I_A	VBIAS_LDO2	**LDO[2] Bias Supply.** Connect to VINLDO[2] or higher voltage.
C1	P	VINLDO[3]	**LDO[3] Supply Input.**
B2	P	GNDLDO[3]	**LDO[3] Supply Return.**
B1	P	LDO[3]	**LDO[3] Output.**
N15	P	VIN[0]	**Supply Input, Switcher 0.** Connect a bypass capacitor between this pin and VRET[0].
P15	P	VRET[0]	**Supply Return, Switcher 0.**
N14	O_A	HSD[0]	**High-Side Drive Switcher 0.**
P14	O_A	LSD[0]	**Low-Side Drive Switcher 0.** When SW[0] is turned off, the low-side driver will discharge the output capacitance at a rate programmable via the configuration EEPROM.
R7	I_A	HSEN[0]	**Output Voltage High-Side Sense, Switcher 0.**
P7	I_A	LSEN[0]	**Output Voltage Low-Side Sense, Switcher 0.**
H15	P	VRET[1]	**Supply Return, Switcher 1.**
G15	O_A	LSD[1]	**Low-Side Drive Switcher 1.**
R6	I_A	HSEN[1]	**Output Voltage High-Side Sense, Switcher 1.**
P6	I_A	LSEN[1]	**Output Voltage Low-Side Sense, Switcher 1.**
P8	O_A	SDDIS[1]	**Shutdown Disconnect 1.** This output is used to reduce leakage current via the resistor divider on the output of SW[1]. SDDIS[1] turns on prior to the output ramping up when SW[1] is enabled and turns off (high-impedance) after the output goes below VIN when SW[1] is disabled.
L15	P	VIN[2]	**Supply Input, Switcher 2.** Connect a bypass capacitor between this pin and VRET[2].
M15	P	VRET[2]	**Supply Return, Switcher 2.**
L14	O_A	HSD[2]	**High-side Drive Switcher 2.**

Pin No.	Type [1]	Name	Description [2]
M14	O_A	LSD[2]	**Low-side Drive Switcher 2.** When SW[2] is turned off, the low-side driver will discharge the output capacitance at a rate programmable via the configuration EEPROM.
R5	I_A	HSEN[2]	**Output Voltage High-Side Sense, Switcher 2.**
P5	I_A	LSEN[2]	**Output Voltage Low-Side Sense, Switcher 2.**
B6	P	SW[2]IN	**Input Voltage for internal VBAT switch connection.** Typically connected to the output of SW[2].
G14	P	VIN[31]	**Supply Input, Switcher 3 and Switcher 1.** Connect a bypass capacitor between this pin and VRET[3].
F14	P	VRET[3]	**Supply Return, Switcher 3.**
F15	O_A	LSD[3]	**Low-Side Drive Switcher 3.**
R4	I_A	HSEN[3]	**Output Voltage High-Side Sense, Switcher 3.**
P4	I_A	LSEN[3]	**Output Voltage Low-Side Sense, Switcher 3.**
R8	O_A	SDDIS[3]	**Shutdown Disconnect 3.** This output is used to reduce leakage current via the resistor divider on the output of SW[3]. SDDIS[3] turns on prior to the output ramping up when SW[3] is enabled and turns off (high-impedance) after the output goes below VIN when SW[3] is disabled.
J15	P	VIN[4]	**Supply Input, Switcher 4.** Connect a bypass capacitor between this pin and VRET[4].
K15	P	VRET[4]	**Supply return, Switcher 4.**
J14	O_A	HSD[4]	**High-Side Drive Switcher 4.**
K14	O_A	LSD[4]	**Low-Side Drive Switcher 4.** When SW[4] is turned off, the low-side driver will discharge the output capacitance at a rate programmable via the configuration EEPROM.
R2	I_A	HSEN[4]	**Output Voltage High-Side Sense, Switcher 4.**
P3	I_A	LSEN[4]	**Output Voltage Low-Side Sense, Switcher 4.**
E14	P	VRET[5]	**Supply Return, Switcher 5.**
E15	O_A	LSD[5]	**Low-Side Drive Switcher 5.**
P1	I_A	HSEN[5]	**Output Voltage High-Side Sense, Switcher 5.**
P2	I_A	LSEN[5]	**Output Voltage Low-Side Sense, Switcher 5.**
P9	O_A	SDDIS[5]	**Shutdown Disconnect 5.** This output is used to reduce leakage current via the resistor divider on the output of SW[5]. SDDIS turns on prior to the output ramping up when SW[5] is enabled and turns off (high-impedance) after the output goes below VIN when SW[5] is disabled.
D15	P	VIN[65]	**Supply Input, Switcher 6 and Switcher 5.** Connect a bypass capacitor between this pin and VRET[6].
C14	P	VRET[6]	**Supply Return, Switcher 6.**
C15	O_A	LSD[6]	**Low-Side Drive Switcher 6.**
N1	I_A	HSEN[6]	**Output Voltage High-Side Sense, Switcher 6.**
N2	I_A	LSEN[6]	**Output Voltage Low-Side Sense, Switcher 6.**
R9	O_A	SDDIS[6]	**Shutoff Disconnect.** This output is used to reduce leakage current via the resistor divider on the output of SW[6]. SDDIS[6] turns on prior to the output ramping up when SW[6] is enabled and turns off (high-impedance) after the output goes below VIN when SW[6] is disabled.
K1	I_A	BLCTL_A	**Analog Backlight Brightness Control or General Purpose Input.** An EEPROM option enables the constant-current output of SW[6] to be controlled via an analog control signal applied to this input. The voltage-current relationship is programmed in the EEPROM. The voltage at this input can be read by a serial command. Leave unconnected if not used.
A12	I	BLCTL_D	**PWM Backlight Brightness Control Input.** The constant-current output of SW[6] can be controlled via a digital PWM control signal applied to this input. The PWM signal frequency must be between 100 Hz and 500 Hz. Leave unconnected if not used.

Pin No.	Type [1]	Name	Description [2]
D14	P	VIN[7]	**Supply Input, Switcher 7.** Connect a bypass capacitor between this pin and VRET[7].
B15	P	VRET[7]	**Supply Return, Switcher 7.**
B14	O_A	HSD[7]	**High-Side Drive Switcher 7.**
M1	I_A	HSENA[7]	**Output Voltage High-Side Sense A, Switcher 7.**
L2	I_A	HSENB[7]	**Output Voltage High-Side Sense B, Switcher 7.**
M2	I_A	LSEN[7]	**Output Voltage Low-Side Sense, Switcher 7.**
K2	I_A	DAS_BYP1	**Internal Reference Voltage Bypass 1.** Connect a 2 KΩ resistor between this pin and AVSS.
L1	I_A	DAS_BYP2	**Internal Reference Voltage Bypass 2.** Connect an 0.01 µF bypass capacitor between this pin and AVSS.
A11	P	DVDD	**Bypass Capacitor for Internal Regulator for Digital Circuits.** Connect a 2.2 µF X5R bypass capacitor between this pin and DVSS.
B13	P	DVSS	**Digital Ground.**
B3	P	RTCVDD	**Internal RTC Supply.** Connect an 0.1 µF X5R (or better) bypass capacitor between this pin and RTCVSS.
B4	P	RTCVSS	**Digital Ground for Internal RTC Supply.**
H1	P	AVDD	**Bypass Capacitor for Internal Regulator for Analog Circuits.** Connect a 2.2 µF X5R bypass capacitor between this pin and AVSS.
H2	P	AVSS	**Analog Ground.**
R15	I	TEST[1]	**Test Input 1.** For FyreStorm use only. Connect to ground for normal operation.
R14	I	TEST[2]	**Test Input 2.** For FyreStorm use only. Connect to ground for normal operation.
P12	P	V_EEPROM	**Supply for Internal EEPROM –** Connect the specified voltage during programming of the internal EEPROM. Do not connect during normal operation.
R12	I/O	EE_SDA	**EEPROM I^2C Data Input/Output, active-high.** Used for EEPROM programming only. Leave unconnected for normal operation.
R13	I	EE_SCL	**EEPROM I^2C Clock input, active-high.** Used for EEPROM programming only. Leave unconnected for normal operation.
C2, G2, H14, R3	--	N/C	**No Internal Connection.** These ball pads may be used for routing.
R1	--	DNC	**Do Not Connect.** Make no connection to these balls.

1. I = digital input, O = digital output, P = power input or output, I_A = analog input, O_A = analog output.
2. See Table 1 for asserted state for digital inputs and outputs and digital output driver type.
3. While in SHUTDOWN state, these pins are not powered and resemble 'floating' open drain outputs to the system. When the device enters READY state, they are configured as inputs with input pull-down resistors. The chip stays in this configuration until the end of Boot (~100 mS) or when SW[2] goes into regulation, depending upon EEPROM configuration option, at which time they are configured as specified. See COLD START POWER-ON SEQUENCE and Table 1.

Table 1. Digital I/O Configuration Options

Pin Name	I or O	Serial Mode	Function	Options		Default		Comments
				Polarity	Active/OD/AOD/PD (2)	Polarity	Active/OD/AOD (2)	
CLKOUT	O	ANY	CLKOUT	--	ACT	--	ACT	
nRSTO	O	ANY	nRSTO	Y	OD/AOD	Active L	OD	Set to OD and connect to ground if not used.
nIRSTO	O	ANY	nIRSTO	N	OD/AOD	Active L	OD	Set to OD and connect to ground if not used.
nRSTI	I	ANY	nRSTI	N	--	Active L	--	
POK	O	ANY	POK	Y	OD/AOD	Active H	OD	Set to OD and connect to ground if not used.
nEXTON	I	ANY	nEXTON	N	--	Active L	--	
nADPTR_DET	O	ANY	nADPTR_DET	Y	OD/AOD	Active L	OD	Set to OD and connect to ground if not used.
PWREN[1]	I	ANY	PWREN[1]	N	--	Active H, Note 1	--	
PWREN[2]	I	ANY	PWREN[2]	Y	--	Active H, Note 1	--	
PWREN[3]	I	ANY	PWREN[3]	Y	--	Active H, Note 1	--	
EE_SDA	I/O	ANY	EE_SDA	N	OD	--	OD	
EE_SCL	O	ANY	EE_SCL	N	OD	--	OD	
nDB	O	ANY	nDB	N	OD/AOD	Active L	OD	Set to OD and connect to ground if not used.
BLCTL_D	I	ANY	BLCTL_D	N	--	Active H	--	Leave floating if not used
MFP[1]	I	I2C	nLOPWR	Y	PD	Active L, Note 1	--	Select input pulldown option if not used
	I	UART	nLOPWR	Y	PD	Active L, Note 1	--	Select input pulldown option if not used
	I	S'ALONE	nLOPWR	Y	PD	Active L, Note 1	--	Select input pulldown option if not used
MFP[2]	I/O	I2C	SCL	N	ACT/OD/AOD	Active H	OD	
	O	UART	EXTPEN2	N	ACT/OD	Active H	ACT	
	O	S'ALONE	nLB	Y	ACT/OD/AOD	Active L	OD	Set to output type ACT if not used
MFP[3]	I	I2C	PWREN[4]/WDRST	Y	PD	Active H, Note 1	--	Configure as an input and select input pulldown option if not used
	O	I2C	EXTPEN3	N	ACT/OD	Active H	ACT	
	O	UART	TxD	N	ACT/OD/AOD	--	ACT	
	O	S'ALONE	EXTPEN3	N	ACT/OD	Active H	ACT	Configure as an input and select input pulldown option if not used
	I	S'ALONE	PWREN[4]/WDRST	Y	PD	Active H, Note 1	--	
MFP[4]	O	I2C	nINTR	Y	ACT/OD/AOD	Active L	OD	
	O	UART	nINTR	Y	ACT/OD/AOD	Active L	OD	
	I	S'ALONE	SD	Y	PD	Active H, Note 1	--	Select input pulldown option if not used
MFP[5]	I/O	I2C	SDA	N	ACT/OD/AOD	--	OD	
	I	UART	RxD	N	PD	--	--	Select input pulldown option if not used
	I	S'ALONE	PWREN[5]	Y	PD	Active H, Note 1	--	Select input pulldown option if not used

Notes

1. Edge-triggered input. Note that on PWREN[5:2] the FS1610 may miss an edge if it happens while the chip is not in ACTIVE or READY states.
2. Active = Output, internal active pull-up. OD = Output, Open-Drain (an external pull-up is required). AOD = Output, Active Open-Drain = when transitioning from Low to High, the output is driven High to 2.5V for one clock period before it is set to open-drain condition (a weak external pull-up is required to take the signal all the way to the desired rail). PD = Input pull down (or not).

OPERATION

Note: The polarity or active state of some signals described in this section may change if the default configuration (Table 1) is changed.

SERIAL INTERFACE AND STAND-ALONE MODES

The FS1610 can operate in two modes:

- **Serial Mode.** In this mode of operation, the device communicates with and can be remotely managed by a host processor via an I^2C or UART interface. The type of serial interface, the I^2C port address and the UART baud rate are specified in the configuration EEPROM.
- **Stand-alone Mode.** In this mode of operation, the device is initially configured via the internal EEPROM and the system uses external pins to control the device. Since the serial interface is not operating, some device features will not be available.

POWER MANAGEMENT

Low power is a top priority in the FS1610. Nothing on the device is active unless its operation is required. To minimize power consumption, clocks are gated at their sources and parts of the device are completely powered down if not operating.

POWER STATES

Figure 9 illustrates the power states of the FS1610. Table 2 summarizes the state transition events.

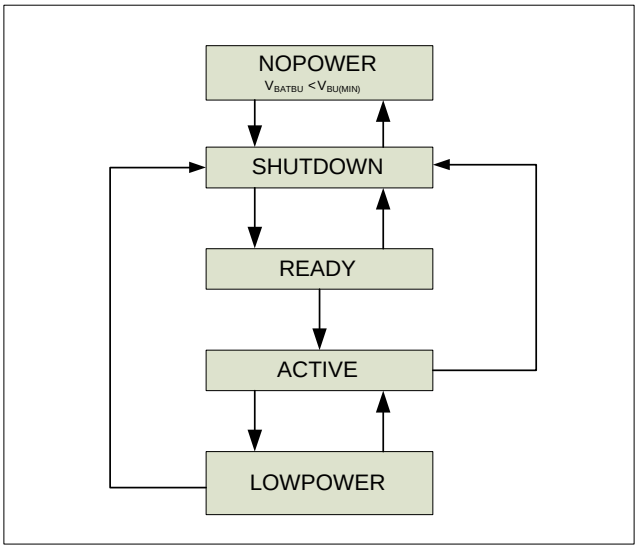


Figure 9. FS1610 Power States

Table 2. FS1610 State Transitions [1]

NEXT STATE	CURRENT STATE				
	NOPOWER	SHUTDOWN	READY	ACTIVE	LOWPOWER
NOPOWER		■ $V_{BATBU} < V_{BU(MIN)}$	■ $V_{BATBU} < V_{BU(MIN)}$	■ $V_{BATBU} < V_{BU(MIN)}$	■ $V_{BATBU} < V_{BU(MIN)}$
SHUTDOWN	■ $V_{BATBU} > V_{BU(MIN)}$		■ >10 seconds and no rails enabled ■ nEXTON goes HIGH before programmed timeout (Note 2) ■ Dead battery ■ T_{TSD} alarm	■ All voltage rails disabled ■ Power rail fault (Note 2) ■ Shutdown command or SD pin assertion ■ nEXTON input at LOW level (Note 2) ■ T_{TSD} alarm	■ All voltage rails disabled ■ Power rail fault (Note 2)
READY		■ RTC alarm ■ PWREN[1] asserted ■ nEXTON at LOW level ■ AC adapter detected Note 2)			
ACTIVE			■ Any rail enabled		■ nLOPWR pin L – H
LOWPOWER				■ nLOPWR pin H - L	

Notes:

1. This table is a general overview only. See detailed descriptions that follow for additional details.
2. EEPROM option

NOPOWER State

In this state the backup battery is below the threshold value required for operation of the device. The internal circuits have insufficient power to operate.

Table 3 summarizes the transition conditions into and out of the NOPOWER state.

Table 3. NOPOWER State Transitions

Transitions into NOPOWER State		
From	**Condition**	**Note**
ANY	Backup battery removed or discharges below $V_{BU(MIN)}$.	
Transitions from NOPOWER State		
To	**Condition**	**Note**
S'DOWN	(V_{BATBU} > $V_{BU(MIN)}$)	

SHUTDOWN State

The SHUTDOWN (SD) state is the 'Sleep' state of the FS1610. In this state, the RTC Power Domain is active and the V_{DD} Power Domain is off.

While in the SD state, the RTC is operational, the WDT and the serial interface do not operate and the VBAT output is active.

Table 4 summarizes the transition conditions into and out of the SD state.

READY State

In this state, The RTC and V_{DD} Power Domains are active. Shortly after the FS1610 enters this state, the device's internal registers are loaded with the power-up settings specified in the configuration EEPROM. The only active power supply output is VBAT. The RTC and WDT are enabled and running if they were so programmed before entering SD state. The serial interface is active.

After loading the power-up settings, the device will transition from READY to ACTIVE if any power rail is enabled by assertion of a PWREN input or if programmed as default (PWREN[0]) supplies in the EEPROM. It will return from READY to SD if ten seconds have elapsed since entry into the READY state and no supplies have been enabled, except if presence of an AC adapter is detected.

The FS1610 may not 'fully' enter the READY state from SD state if several tests based on the configuration data read from the EEPROM are not satisfied. These include a test that VIN is above the Minimum Voltage to Boot value (V_{BTMIN}) and a test that nEXTON stays Low for the time specified in the ExtOnTimeout EEPROM variable (if the TIMED_WAKEUP EEPROM option is enabled). See Figure 18.

Table 4. SHUTDOWN State Transitions

Transitions into SHUTDOWN State		
From	**Condition**	**Note**
NOPWR	A good backup battery (V_{BATBU} > $V_{BU(MIN)}$) is inserted	
ACT	All voltage rails, including rails in PWREN group [0], are disabled	5, 11
	A channel fault occurs	2, 5
	Over-temperature alarm occurs	5
	A Shutdown command is received or the SD pin is asserted	5
	nEXTON goes from High to Low and stays Low for the time specified in the ExtOnTimeout EEPROM variable	8
LOPWR	All voltage rails are disabled	1, 5
	A channel fault occurs	2, 5
READY	Ten seconds since entry into READY state and no supplies have been enabled	1
	nEXTON does not stay Low for the time specified in the ExtOnTimeout EEPROM variable	10
Transitions from SHUTDOWN State		
To	**Condition**	**Note**
READY (Note 6)	An RTC alarm	3
	Assertion of the PWREN[1] input	3, 4
	The nEXTON input goes from High to Low	3, 9
	nEXTON stays Low for the time specified in the ExtOnTimeout EEPROM variable	3, 10
	AC adapter is detected	7

Notes:

1. If AC adapter not detected.
2. If channel fault is configured to shutdown the chip
3. If VMAIN > V_{DBTH}
4. Not during a cold-start boot
5. The last commanded values for the output voltages of SW[4, 2, 0], LDO[3:1] and the last commanded current for SW[6] are saved. See Shutdown Restore section for additional information.
6. The FS1610 reads the contents of the configuration EEPROM and the transition to READY state continues if VIN is above the Minimum Voltage to Boot value (V_{BTMIN}) read from the EEPROM. If it is not, the device returns to SD state.
7. Only if Wake on ADPTR_IN option is enabled via the EEPROM.
8. If the TIMED_ACTIVE_SHUTDOWN EEPROM option is enabled.
9. If the TIMED_WAKEUP EEPROM option is disabled.
10. If the TIMED_WAKEUP EEPROM option is enabled.
11. Only if Wake on ADPTR_IN option is disabled via the EEPROM.

ACTIVE State

This is the normal operational state. The RTC and V_{DD} Power Domains are active. The serial interface begins operating at the conclusion of the RSTO timeout. This timeout expires t_{RSTO} after the set of voltage

rails specified in the EEPROM are enabled and reach POK status.

Table 5 summarizes the transition conditions into and out of the ACTIVE state.

Table 5. ACTIVE State Transitions

Transitions into ACTIVE State		
From	**Condition**	**Note**
READY	One or more power rails enabled via PWREN inputs or by initial configuration setting.	
LO'PWR	L – H transition of the nLOPWR pin	
Transitions from ACTIVE State		
To	**Condition**	**Note**
LO'PWR	H – L transition of the nLOPWR pin	1, 2
SHUTDOWN	All voltage rails, including rails in PWREN group [0], are disabled	3
	A channel fault occurs	3, 4
	Over-temperature alarm occurs	3
	A Shutdown command is received or the SD pin is asserted	3
	nEXTON goes from High to Low and stays Low for the time specified in the ExtOnTimeout EEPROM variable	5

Notes:

1. SW[0] and/or SW[2] must be enabled.
2. The FS1610 waits until SW[7, 6, 5, 4, 3, 1] are disabled before it begins the transition to LOWPOWER state.
3. The last commanded values for the output voltages of SW[4, 2, 0], LDO[3:1] and the last commanded current for SW[6] are saved. See Shutdown Restore section for additional information.
4. If channel fault is configured to shutdown the chip
5. If the TIMED_ACTIVE_SHUTDOWN EEPROM option is enabled.

LOWPOWER State

In LOWPOWER state, the RTC and V_{DD} Power Domains are active. Buck converters SW[2, 0] operate in PFM (pulse frequency modulation) mode and are limited to 5% of their ACTIVE mode programmed maximum current. This reduces their quiescent current and improves efficiency at low load currents. The LDO regulators and RTC operate normally, but the WDT and serial interface are not operational.

An EEPROM option allows selected PWREN inputs to be disabled while in this mode. An attempt to enable any power rail other than SW[2, 0] or LDO[3:1] via a non-disabled PWREN while in this mode is ignored.

Table 6 summarizes the transition conditions into and out of the LOWPOWER state.

Table 6. LOWPOWER State Transitions

Transitions into LOWPOWER State		
From	**Condition**	**Note**
ACTIVE	H – L transition of the nLOPWR pin	1, 2, 3
Transitions from LOWPOWER State		
To	**Condition**	**Note**
ACTIVE	L - H transition of the nLOPWR pin	

Notes:

1. SW[0] and/or SW[2] must be enabled.
2. The FS1610 waits until SW[7, 6, 5, 4, 3, 1] are disabled before it begins the transition to LOWPOWER state.
3. To ensure that a pending interrupt is not missed because of this transition by a host such as the PXA270 that handles wake-up interrupts only once in sleep mode, an EEPROM option causes the device to pulse nINTR once at the end of the transition if an interrupt was pending at the start of the transition.

Shutdown Restore

When the FS1610 enters SHUTDOWN from ACTIVE or LOWPOWER states, it stores the voltages of SW[4, 2, 0] and the LDOs and the current of SW[6]. If the Shutdown Restore option is enabled via the EEPROM, those stored values override the values read from the EEPROM during the transition to ACTIVE state. Thus, their outputs will be at the same values they were at before going to SHUTDOWN.

BUCK CONVERTERS: SW[4, 2, 0]

These three power rails, Figure 10, use a patented digital control algorithm to provide a high-efficiency step-down converter implementation.

The output voltage of these converters is programmable from 0.85 V to 3.3 V. Each converter is independently programmable to be enabled by one of the PWREN enable inputs, by a serial command, or via the configuration EEPROM.

The buck converters support several features that may be required in the system application.

Soft-Start

Each regulator includes a soft-start circuit that limits start-up inrush current to a value specified in the configuration EEPROM.

Dynamic Voltage Management (DVM)

SW[4, 2, 0] support the ability to alter their output voltage with a prescribed ramp interval. If this mode is enabled, the voltage ramp is initiated when a new target voltage is programmed. Figure 11 depicts the timing for transitioning between voltages. The step size is programmable in increments of approximately 5 mV to a maximum of 300 mV. The time between steps is programmable in increments of approximately N x 7.6 µs, where N is a value from 0 to 31.

For N = 0, or when this mode is disabled, the voltage transition to the final value is made without any intermediate steps.

If a serial command to change the voltage of a rail operating with DVM enabled is received while a previously requested voltage change is in progress, the new command will be rejected (NAK).

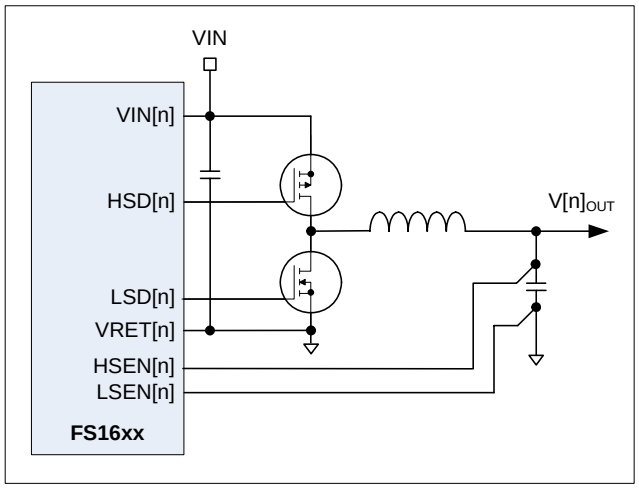


Figure 10. Buck Converter, SW[4, 2, 0]

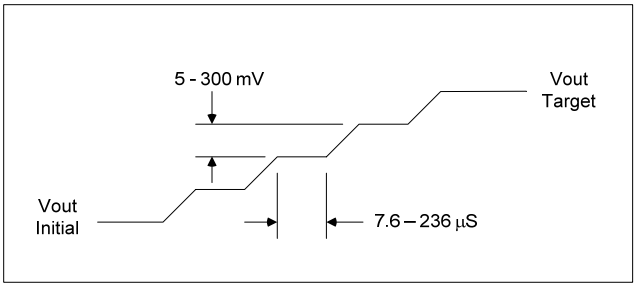


Figure 11. Dynamic Voltage Management

Output Voltage Range Checking

SW[4, 2, 0] may be programmed independently to limit their output voltage to minimum and maximum voltages specified in the configuration EEPROM. If programmed to operate in this manner, any command to change the output voltage to a value outside the specified minimum and maximum limits will be rejected.

Low Power Mode

When the FS1610 is in LOWPOWER mode, buck converters SW[2, 0] operate in PFM (pulse frequency modulation) mode, which increases efficiency at low power levels. Output current in this mode is limited to 10% of the programmed ACTIVE mode maximum current.

The output voltage of buck converters SW[2, 0] is automatically changed to a preset low-power value configured in the EEPROM (which can be the same or different from the ACTIVE mode value). This allows compatibility with the TI OMAP processor or others requiring this feature.

Active Discharge

SW[4, 2, 0] can be configured to actively discharge the output capacitance when disabled. If this feature is enabled, the output voltage is monitored for a specified voltage level. If the output is at a higher voltage, the low-side driver is pulsed at a programmable rate to discharge the output capacitance until the specified voltage level is sensed.

Shutdown Restore

Shutdown Restore can be enabled for the buck converters via the EEPROM. See Shutdown Restore section.

WHITE LED DRIVER: SW[6]

The White LED driver, illustrated in Figure 12, uses step-up (boost) architecture and is designed to drive from two to ten LEDs in series, providing identical LED currents and eliminating the need for ballast resistors. The unit operates in programmable constant current mode.

The full scale constant current is programmable up to 30mA via the serial interface. This current can then be controlled by one of several methods:

- A digital PWM signal applied to the BLCTL_D input can control the duty cycle.
- The average current can also be controlled by an analog signal applied at the BLCTL_A input. For this mode of operation, parameters stored in the EEPROM provide for eight levels of brightness corresponding to specified input voltage ranges.
- Serial commands can specify one of the eight preconfigured brightness levels in the EEPROM or can specify the current in increments of one mA.

The White LED Driver has over-voltage protection at a value read from the EEPROM at power-up. If the output voltage exceeds the over-voltage threshold, the channel will switch to constant voltage mode operation at the threshold voltage. If the cause of the over-voltage is removed, the channel will automatically revert to constant current operating mode. See Power Rail Fault Monitoring for additional information.

The SDDIS[6] pin is used to reduce leakage current from the resistor divider on the output of this converter. SDDIS[6] turns on, connecting the resistive divider to LSEN (ground), prior to the output ramping up when the

converter is enabled and turns off (high-impedance), disconnecting the resistive divider, after the output goes below VIN when the converter is disabled.

Output Current Range Checking

SW[6] limits the output current to minimum and maximum values specified in the configuration EEPROM regardless of the value programmed into its current programming register. The output current will not go below the specified minimum value or above the specified maximum value.

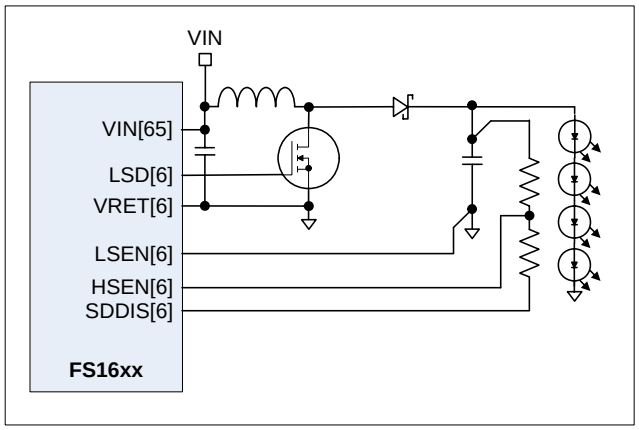


Figure 12. White LED Driver, SW[6]

BOOST CONVERTERS: SW[5, 3, 1]

These power rails are high-efficiency switching converters operating in a step-up configuration to supply positive output voltages of up to 25 V. The output voltages for these rails are specified in the EEPROM and cannot be changed during operation.

The SDDIS[n] pin is used to reduce leakage current from the resistor divider on the output of these converters. SDDIS[n] turns on, connecting the resistive divider to LSEN (ground), prior to the output ramping up when the converter is enabled and turns off (high-impedance), disconnecting the resistive divider, after the output goes below VIN when the converter is disabled.

The boost converter is illustrated in Figure 13.

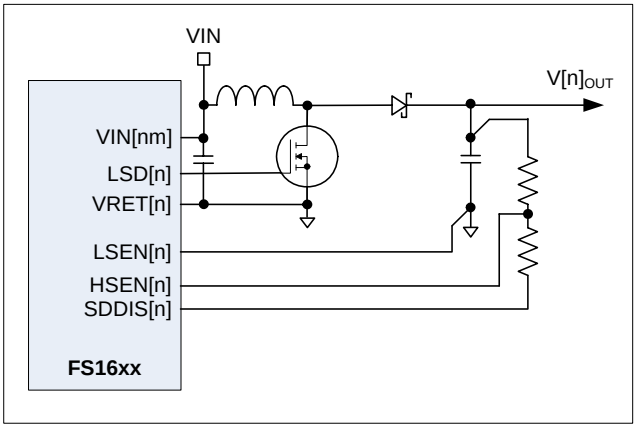


Figure 13. Boost Converter, SW[5, 3, 1]

LOW DROP-OUT REGULATORS: LDO[3:1]

These linear regulators are designed for low quiescent current operation and incorporate internal pass transistors. All are fully programmable by software commands. LDO[2] provides low noise performance via a bypass capacitor. Each LDO has a separate input voltage pin that allows the input to be selected to maximize system efficiency.

Shutdown Restore can be enabled for the LDOs via the EEPROM. See Shutdown Restore section.

The LDOs can operate during LOWPOWER mode.

> **Note:** The LDO should be disabled before commanding an output voltage change and then re-enabled. Failure to do so may result in an LDO fault condition. See Power Rail Fault Monitoring for fault handling options.

BUCK/BOOST CONVERTER: SW[7]

This power rail, illustrated in Figure 14, is a high-efficiency switching converter operating in a step-up configuration, and is capable of supplying a negative output voltage of -20 V maximum. The output voltage is specified in the EEPROM and cannot be changed during operation.

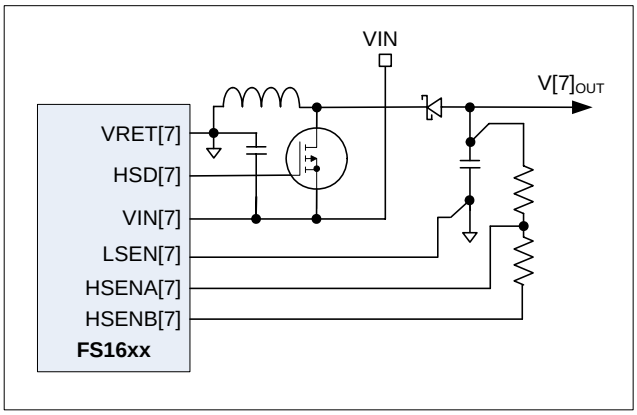


Figure 14. Buck/Boost Converter, SW[7]

VBAT (SLEEP MODE) SUPPLY OUTPUT

Intended primarily for Intel PXA27x applications, VBAT can be used with any processor requiring an active voltage rail during their Sleep mode. It is the first supply to be active and the last to power-off. This provides a means to supply power for circuits such as a time-clock and memory that need to operate even in the absence of main battery input power.

- VBAT = VINSW[2] if SW[2] is enabled and in regulation.
- VBAT = BATBU if SW[2] is disabled or out of regulation.

REAL TIME CLOCK (RTC)

The FS1610 provides an RTC operating from the crystal clock. It features a span of 10 years, with a granularity of one second. A programmable alarm can cause an interrupt to be issued to the host CPU. The RTC and the RTC alarm are automatically cleared and the RTC is enabled upon power-up.

If the RTC alarm occurs while the FS1610 is in SHUTDOWN state, the event will 'wake-up' the device and cause it to transition to READY state. The nINTR output will be asserted to alert the host to enable appropriate supplies in the device, if not automatically enabled (see POWER CONTROL AND SEQUENCING), so it can determine the cause of the interrupt.

WATCH DOG TIMER

The device incorporates a watch-dog timer (WDT) with an EEPROM programmable timeout of up to 32 seconds and a granularity of one millisecond. The WDT can be optionally disabled at power-up via the EEPROM. If so configured, it begins to operate when it receives an Enable WDT serial command from the host.

Expiration of the WDT asserts nRSTO for t_{RSTO}. To ensure that this event does not occur, the Host must reset the WDT before the programmed time-out period expires. The WDT is reset upon receipt of any valid serial command addressed to the device (see Table 9, FS1610 Command Set Overview) or, if so configured, via any transition at the MFP[3] input in stand-alone mode or I^2C serial mode.

Note: The WDT does not operate in LOWPOWER mode and is not reset when the FS1610 transitions from LOWPOWER to ACTIVE modes. To prevent inadvertent expiration of the WDT when returning to ACTIVE mode, it is recommended that the WDT be reset before placing the device in LOWPOWER mode.

POWER CONTROL AND SEQUENCING

The FS1610 provides multiple levels of power on/off sequencing via a very flexible scheme to control and sequence power of all voltage rails.

- Any number of rails can be programmed, via the EEPROM, to be automatically turned on when the device is loaded with the EEPROM contents when entering the READY state. Any rail thus enabled is said to belong to the PWREN[0] group. These rails are disabled when transitioning to the SHUTDOWN state after a SHUTDOWN command or assertion of the SD input.
- Groups of rails can be programmed to be controlled by the PWREN[5:1] inputs or by equivalent serial commands.
- Any single rail can be enabled or disabled by a serial command. This should not be used to control rails that are controlled by PWREN[5:0].

Note: If a channel that is part of a PWREN group is turned ON individually by a command, a subsequent PWREN group disable command may not turn it off.

Note: The PWREN[5:1] inputs are edge-triggered. A low-high transition enables the power-rail group, a high-low transition disables the group.

Note: The FS1610 permits a maximum of 11 instances of power rails in PWREN[5:0]. Thus, for example, if one rail is placed in three groups, only 8 of the remaining 10 rails can be controlled by PWREN[5:0], and the remaining two rails, if used, have to be controlled by single-rail enable/disable serial commands.

When a group of supplies mapped to PWREN[5:0] is enabled or disabled, a programmed load activation/shedding sequence defined in the configuration EEPROM is activated for that group of supplies. This is illustrated in Figure 15.

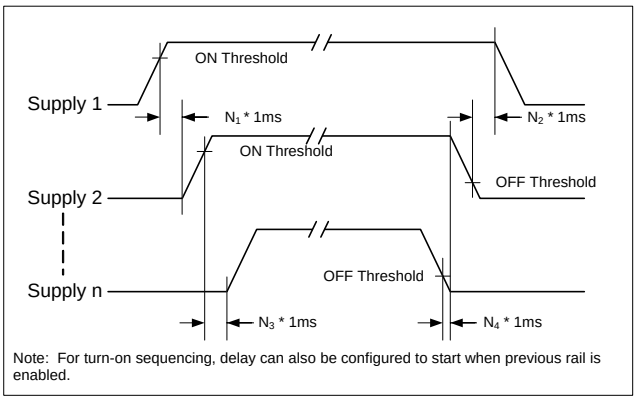


Figure 15. Power Sequencing

As illustrated, the supplies within the group sequence each other on and off. This ensures that any number of supplies is well controlled with respect to each other regardless of load capacitance and ramp time. Core and I/O relationships are one example of where this mode would be useful.

The ON threshold (Figure 15) is the internal POK signal for every supply. Also note that the ON sequence delay can start from when a rail is enabled rather than from its POK. The OFF threshold is:

- EEPROM configurable for switchers SW[4, 2, 0]
- (VIN + 0.4 V) for switchers SW[5, 3, 1] and SW[6]
- For SW[7], the same as the SW[0] OFF threshold programmed in the EEPROM

There is no OFF Threshold for LDO[3:1], and the turn-off delay for the next voltage rail begins immediately after the LDO is disabled.

N can range from 0 to 255 and is independently programmable for each voltage rail transition. Where N = 0, the subsequent supply immediately begins its power-on or power-off cycle after the previous supply's output reaches its ON or OFF threshold.

CRYSTAL OSCILLATOR

A crystal oscillator operating from a low-cost 32.768 KHz crystal is used for all internal timing. If a clock at the proper frequency and voltage is available in the system, it may be connected to the X1 input and the crystal is eliminated. **Error! Reference source not found.** illustrates the external connections required for this oscillator. Capacitor values may be different for a different crystal.

A 32.768 KHz output is provided on CLKOUT for external use. This output is initially enabled and thus is active during the cold-start power up.

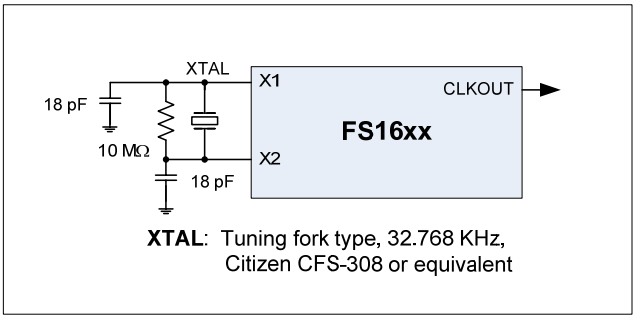


Figure 16. Crystal Oscillator

EEPROM options can be used to enable or disable CLKOUT after the first time that the device enters the READY state as follows:

- Always off
- Always on
- Always on except in SHUTDOWN mode when it is turned off
- on if nDB = 1, off if nDB = 0

BACKUP BATTERY INPUT

The FS1610 has a separate input for a backup battery (BATBU) for use if the main input VIN is not present. As described previously, a voltage must be present on BATBU in order for the device to operate. Normally, a primary or rechargeable backup battery is connected to this pin. If a backup battery is not used, then BATBU should connect to VIN through a diode or external regulator. See Figure 17 and Figure 22.

If the voltage of the main battery falls below the dead battery threshold, and if the device is operating in LOWPOWER mode, the device will be powered from the backup battery if $V_{BATBU} > V_{MAIN}$. See Battery Voltage Monitor and Backup Battery section for additional information.

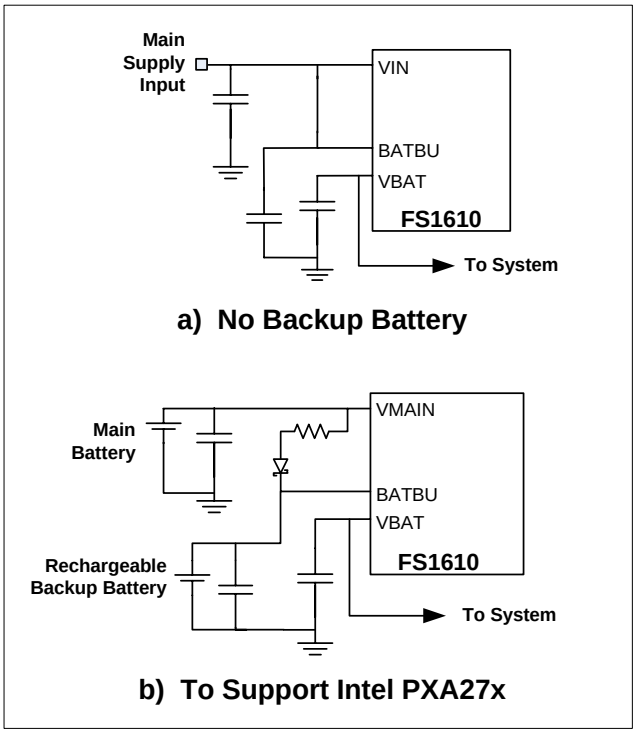


Figure 17. Typical Back Up Battery Configurations

nEXTON SWITCH INPUT

This input is normally connected to a momentary contact switch and is used to control ON and OFF events for the device. The input is normally High via an internal pull-up resistor and is connected to ground (Low) to initiate ON and OFF events as described below.

There are three EEPROM parameters associated with the nEXTON input:

- **ExtOnTimeout** – a variable configurable from 250 ms to 12 seconds. The 250 ms timer is a system timer that is not synchronized to the High to Low transition of nEXTON, so the actual time may be up to one count (250 ms) longer than programmed. Timing for this event begins after the nEXTON input debounce interval t_{EXTON} (approximately 100 ms) and reading of the EEPROM when transitioning out of SHUTDOWN state (approximately an additional 80 ms).

  When the device is in ACTIVE or LOWPOWER states and nEXTON goes from High to Low and stays Low for the time specified in ExtOnTimeout, the FS1610 sets a bit in its Status Register. See the FS1610 HSI User Manual for additional information.

- **TIMED_WAKEUP** – if this option is turned On, it requires that nEXTON goes from High to Low and stays Low for the time specified in ExtOnTimeout to cause a transition from SHUTDOWN to READY states. If this option is turned Off, that transition is initiated immediately upon detecting that nEXTON has changed from High to Low.

- **TIMED_ACTIVE_SHUTDOWN** – if this option is turned On, and the device is in ACTIVE state, and nEXTON goes from High to Low and stays Low for the time specified in ExtOnTimeout, the chip will transition from ACTIVE to SHUTDOWN states via a simultaneous shutdown of all Power Enable groups (with specified sequencing within each group). If this option is turned Off, bringing nEXTON Low while in ACTIVE state has no effect on the power rails.

COLD START POWER-ON SEQUENCE

The FS1610 performs a pre-defined startup sequence upon initial power-on. The chip's startup power supplies are powered via the BATBU input supply, which must be connected and at or above $V_{BU(MIN)}$ in order to guarantee that the device begins operation. As noted previously, application of the main battery power (V_{MAIN}/V_{IN}) by itself will not initiate device startup. Refer to the simplified flow chart, Figure 18, and the timing diagram, Figure 19, for the following discussion.

1. An internal power-on-reset (POR) cycle is initiated when BATBU reaches the operational threshold, $V_{BU(MIN)}$. The following events occur at this time:
   - o nDB is asserted.
   - o VBAT is kept off
   - o All RTC time values and alarms are cleared and the RTC is enabled.
2. The FS1610 enters the SHUTDOWN state. In this state most internal subsystems are unpowered, and the FS1610 draws very little power from the backup battery.
3. If the presence of an AC adapter is detected via the ADPTR_IN input, the FS1610 reads the contents of the configuration EEPROM and checks whether this condition is programmed to wake up the chip. If it is, the boot-up process continues at step 7 below. Otherwise, go to step 5 below.
4. If an AC adapter is not connected, the chip remains in the SHUTDOWN state monitoring the VMAIN input for a valid main battery voltage, using the default 'dead battery' voltage of 3.1V as a reference.
5. The FS1610 now waits until it detects a Low at the nEXTON input to continue the initial power-on sequence.
6. FS1610 reads the contents of the configuration EEPROM and checks whether the TIMED_WAKEUP option is enabled. If it is, it continues to monitor nEXTON to check if it remains low for the time specified in the ExtOnTimeout parameter read from the EEPROM. If the test fails, the FS1610 returns to SHUTDOWN. If it passes, or if the TIMED_WAKEUP option is not enabled, the initial boot-up process continues.
7. The following actions occur during the initial boot-up sequence:
   - o nDB is de-asserted
   - o The reset output nIRSTO is asserted for tIRSTO and the nRSTO output is asserted.
   - o POK is driven Low, indicating that one or more power rails are not in regulation.
   - o BATBU is routed to the VBAT output to serve as a Sleep power source for the host processor.

     Note: The VBAT output is intended primarily as the Sleep power source (VCC_BATT) for Intel's PXA27x processors. The behavior described above is designed to ensure that an anomaly in that device, which causes it to draw excessive current from this voltage rail before the processor is properly initialized for Sleep operation, does not drain the back-up battery. See FyreStorm application note AN52-1.
   - o The internal system controller and other circuitry are powered-up and begin operation.
   - o Device configuration parameters are read from the internal EEPROM and loaded into appropriate internal registers.
   - o VIN is checked to make sure it is above the Minimum Voltage to Boot value (V_{BTMIN}) read

from the EEPROM. If it is not, the device returns to SHUTDOWN state.

Note: An EEPROM-configurable option can be used to force continuation of the boot process even if this test fails.

- o The EXTPEN[3:2] output is asserted to enable external power rails, if this function has been selected by configuration option.
- o If so programmed via PWREN[0], any supply or group of rails can be automatically activated at this time. This provision allows CPUs without a resume power block running from VBAT to power themselves up.
- o The device enters the READY state and starts the ten second READY timeout. It remains in this state until a voltage rail is enabled via PWREN[0] or any one of the hardware power enable inputs, PWREN[5:1].

Note: An EEPROM-configurable option can be used to cause the FS1610 to ignore PWREN[5:1] or PWREN[5:2] until SW[2] is in regulation. If configured to ignore PWREN[5:1], SW[2] must be configured to belong to PWREN[0] so that it automatically turns on at power-up.

- o If no power rail is enabled and the READY timeout expires, the device returns to the SHUTDOWN state, except if ADPTR_IN indicates that AC adapter power is present and the wake-up on ADPTR_IN option is enabled.

8. If at least one power rail is enabled, the device enters the ACTIVE state and the voltage rails are activated using the power-on sequencing parameters read from the configuration EEPROM.
   - o nRSTO is de-asserted and the serial interface becomes active tRSTO after an EEPROM-specified set of voltage rails reach their power-good threshold.
   - o When the group of rails specified to be monitored by POK in the EEPROM reach their power-good threshold, the POK output is asserted.

SHUTDOWN After Cold–Start

When the FS1610 goes into SHUTDOWN mode for any reason after the cold-start boot, the transition from that state to READY is as previously described with the following differences:

- An EEPROM programmable option can be enabled to route BATBU to VBAT while in SHUTDOWN instead of only after the trigger event that initiates the SHUTDOWN to READY state transition (Figure 19).
- A transition from SHUTDOWN to READY states will be initiated if an RTC alarm occurs.
- A transition from SHUTDOWN to READY states will be initiated if the PWREN[1] input is asserted (in addition to the ‘trigger’ events described in section 3 above).

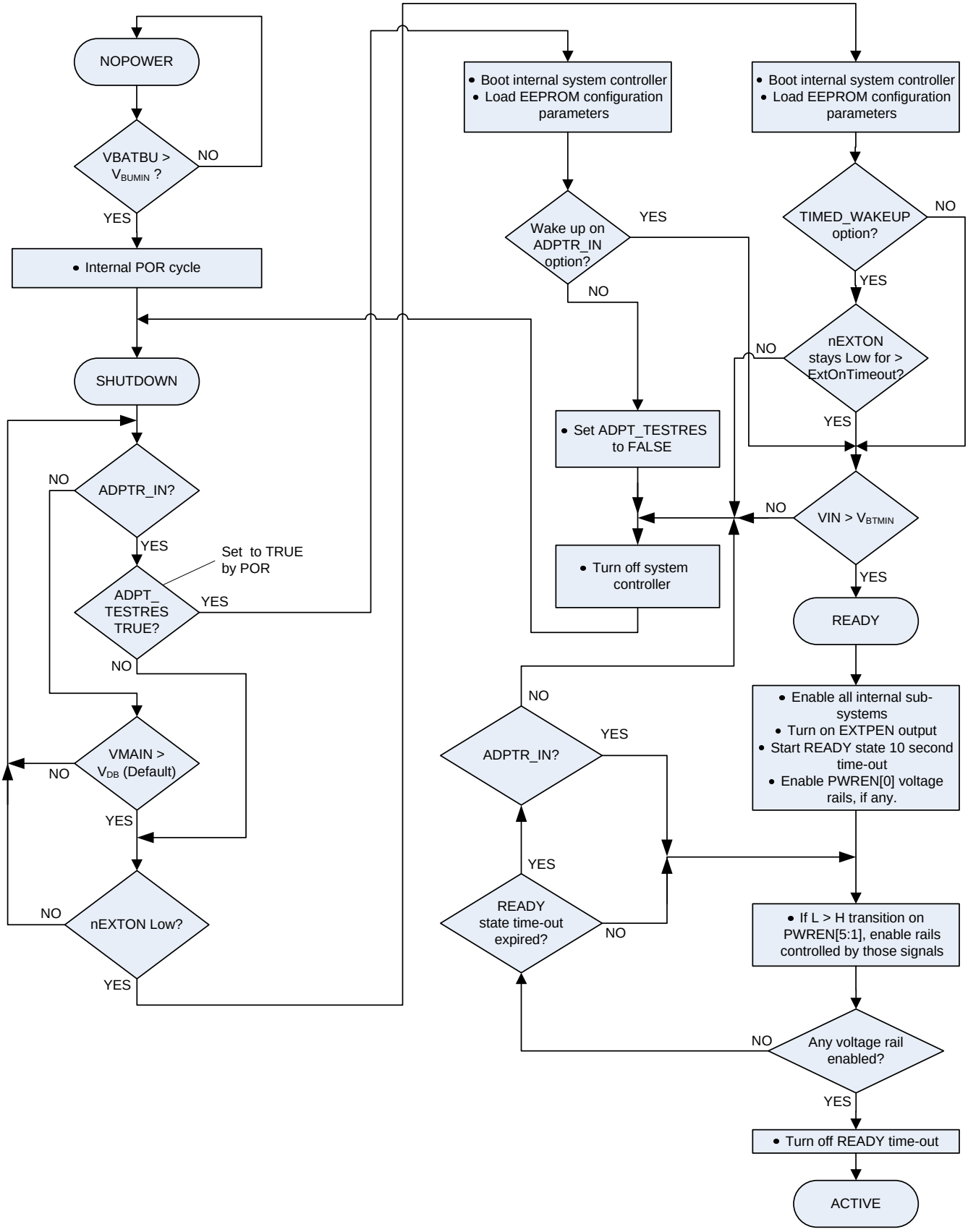
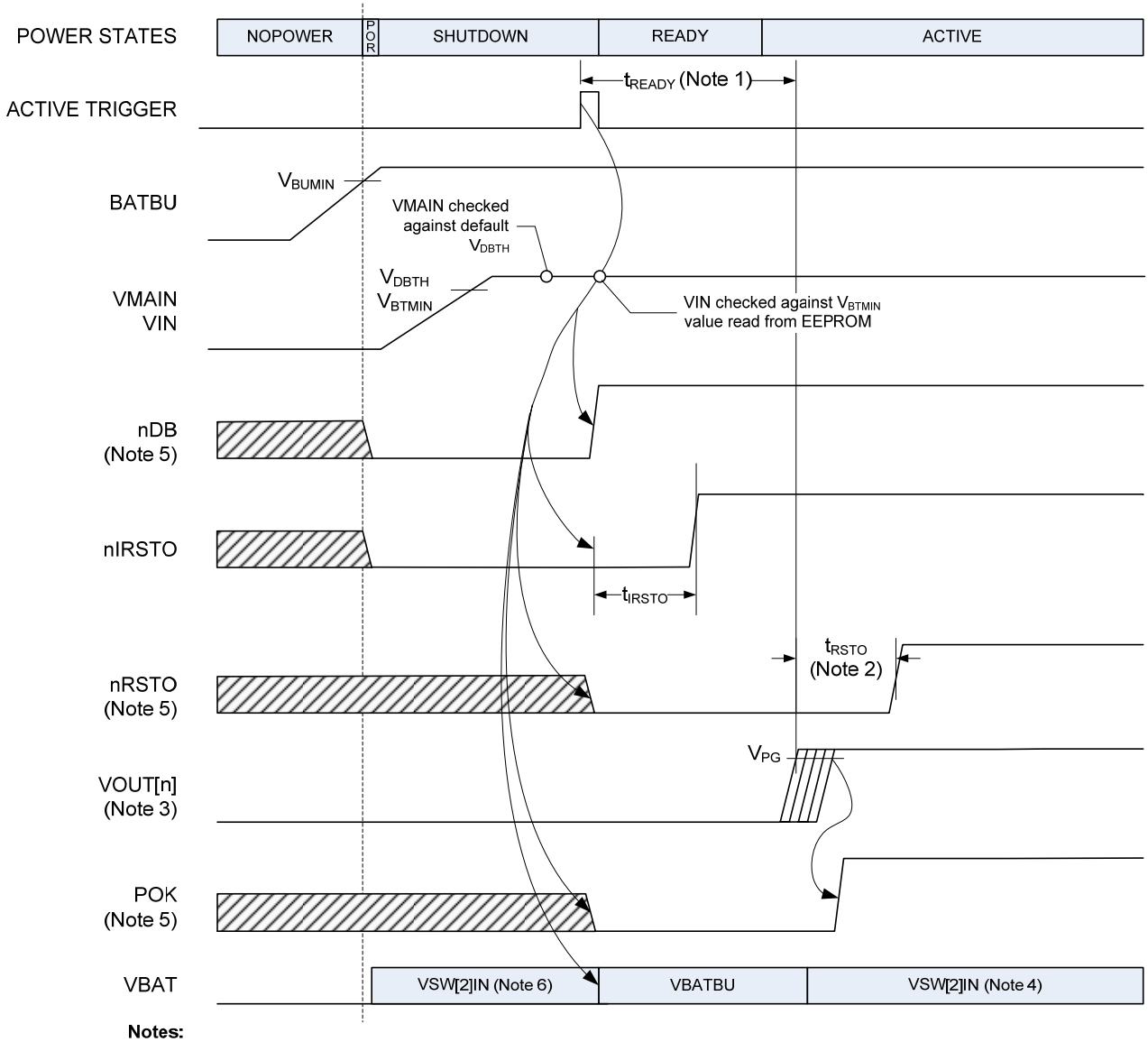


Figure 18. Simplified Cold Start Power-up Flow Chart



Notes:

1. Measured from active trigger until the first enabled supply reaches its power-good threshold.
2. De-asserted t_{RSTO} after an EEPROM-specified set of voltage rails reach their power-good threshold.
3. Illustrates several voltage rails being activated in sequence per parameters read from configuration EEPROM.
4. The input at VSW[2]IN is routed to VBAT when SW[2] is in regulation.
5. This is an open-drain output. The L – H transition on this signal indicates the time when the internal driver 'floats' the output. The actual waveform will depend on external connection at this output.
6. On cold-boot, VBAT is connected to SW[2]IN during this period. If SW[2]IN is connected to SW[2] output, the output at VBAT will be '0' during this time. For subsequent entries to SHUTDOWN state, an EEPROM option can be used to connect VBAT to either SW[2]IN or BATBU during this period.

Figure 19. Cold Start Power-up Timing Diagram

Reset Outputs

The FS1610 provides dual reset outputs. The nIRSTO output is intended for the Intel PXA27x or similar processors that do not support assertion of power-on reset subsequent to activation of their core and I/O power rails.

nIRSTO is asserted under the following conditions:

- When a valid 'trigger' event occurs during the cold-start power up sequence (Figure 19).
- When the manual reset input (nRSTI) in asserted.

The nRSTO output is intended for processors that require their reset input to be asserted until appropriate power rails are active and valid. This output is asserted under the following conditions:

- Shortly after a valid trigger event. It is then de-asserted t_{RSTO} after all the power rails designated in the EEPROM to trigger this action have reached their POK threshold.

- When the manual reset input (nRSTI) in asserted.
- When the WDT timer expires.
- When the device transitions from ACTIVE or LOWPOWER states to SHUTDOWN state.
- For the last three events, the signal de-asserts automatically.

Manual Reset Input

The Manual Reset input, nRSTI, is used to initiate a hardware reset that can be used as a system reset for the host CPU. Assertion of nRSTI will trigger assertion of the nIRSTO and nRSTO outputs for t_{IRSTO} and t_{RSTO} respectively as shown in Figure 20. Note that the I^2C interface is reset at the rising edge of tRSTO. Thus, if the host initiates an HSI command transmission on the I^2C between the trailing edge of nIRSTO and the trailing edge of nRSTO, it will be lost.

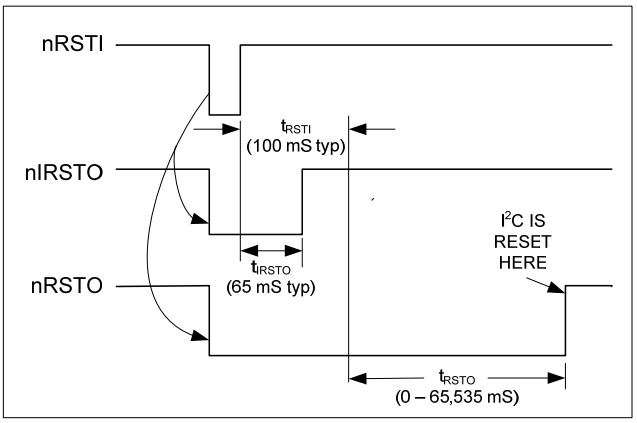


Figure 20. Manual Reset Timing

FAULT MANAGEMENT

POK Status

Each power rail can be programmed via the EEPROM to be monitored by the POK output signal. This initial setting can subsequently be changed via serial commands if required. If a monitored power rail is not in regulation (whether it is enabled or not), the POK output is de-asserted. An internal delay is implemented before the POK status is latched within the FS1610 to prevent false indications (see Fault Delay in next section).

Power Rail Fault Monitoring

The FS1610 monitors the status of each power rail, except VBAT. If any enabled rail indicates an out-of-regulation condition, the device will make one of several possible responses, as programmed for the rail in the configuration EEPROM.

Table 7 summarizes the fault conditions and responses for each power rail. All constant voltage (CV) switcher power rails have over-current protection with a limit value that can be programmed in the EEPROM. SW[6], the constant current (CC) Boost channel, has over-voltage protection, with the protection threshold configured in the EEPROM.

Note: The Buck channels that operate in LOWPOWER mode (SW[0] and SW[2]) have a separate programmable current limit used during that mode of operation.

Table 7. Channel Faults and Response Options

	Fault Response Options					
	Out of Regulation	Over-Current (Programmable in EEPROM)	Over-Voltage (Programmable in EEPROM)	Shutdown Channel and Set Status	Auto-Restart and Set Status	Shutdown Chip
Buck	X	X		X	X	X
CV Boost	X	X		X		X
CC Boost	X		X	X		X
Buck-Boost	X	X		X		X
LDO	X			X	X	X

When a fault in an enabled channel is detected, the FS1610 responds as configured for that channel in the EEPROM. The options are:

- Shutdown channel and set channel fault status bit
- Shutdown channel, set channel fault status bit and auto-restart channel (option not available for Boost and Buck-Boost channels)
- Shutdown the chip

Note: Setting the fault status bit for a channel will result in an interrupt to the host if the FS1610 is so programmed.

Note: Over-voltage in the CC Boost channel (SW[6]) is not classified as a fault and a fault condition is not indicated in that event. See WHITE LED DRIVER: SW[6] section for additional information.

In addition to the type of fault response, there are also two EEPROM-programmable parameters associated with the fault response. Fault Delay is the in-

terval between the time the channel reports a fault and the FS1610 recognizes the fault and takes any action related to it. A value of 0 for Fault Delay means to ignore all faults for the channel. Auto-Restart Delay is the time the FS1610 will wait after it shuts down the channel until it attempts to restart it. Each of these parameters is independently programmable for each channel from 0 – 255 ms via the EEPROM. The auto-restart activity is repeated until the fault is removed or the channel is disabled by the host.

If a channel is shutdown and not configured to auto-restart, it can be restarted by toggling the respective external power enable input or by a serial command.

A power rail fault event can be programmed to generate an interrupt to the host controller. The host can then use a serial command to determine which rail(s) experienced a fault.

A power rail fault can also be configured to assert the nRSTO output independently for each channel. When the fault causing that assertion is cleared, nRSTO will de-assert after its programmed duration (t_{RSTO}).

Battery Voltage Monitor and Backup Battery

The battery voltage monitor periodically checks the voltage at the main battery test input, VMAIN. There are three battery states defined; Battery-good, low battery (LB) and dead battery (DB). The LB and DB thresholds are EEPROM-programmable. Internal aver-aging and hysteresis prevent nuisance tripping when the battery voltage is near the LB and DB values.

When VMAIN falls below the low-battery threshold (V_{LBTH}), nINTR (if so programmed) and the LB output are asserted.

If the FS1610 is in ACTIVE or LOWPOWER states when VMAIN reaches the dead-battery threshold (V_{DBTH}), the FS1610 automatically shuts down the power rail groups designated in the EEPROM (PWREN[5:0]). An EEPROM option also determines whether this follows the programmed sequencing or is an immediate shutdown of the rails in the specified power rail groups. The FS1610 remains in the ACTIVE or LOWPOWER state with other enabled power groups or individually enabled power rails still active in order to allow the host to perform an orderly shutdown of the system. When the host subsequently disables the enabled power rails and power rail groups, the FS1610 will transition to SHUTDOWN state.

If the FS1610 is in LOWPOWER state when V_{DBTH} is detected, internal switches route power from BATBU to VIN to supply the active power rails. The DBOUT output is asserted during that time and should be used to switch the main battery out of the circuit while power is being routed to VIN from BATBU. See Figure 21.

> **NOTE**: If a dead battery condition occurs while in LOWPOWER mode and a request for a transition to ACTIVE mode is received, the FS1610 first checks the battery condition. It does not complete the requested transition until four consecutive tests, taken at 250 ms intervals, indicate that the battery is not below the dead battery threshold, V_{DBTH}.

DBOUT is also asserted if the presence of an AC adapter is detected via the ADPTR_IN input. In that case, the battery is switched out of the circuit and VIN is supplied from the adapter via an isolation diode.

nDB is asserted during a dead-battery condition. This output typically connects to the 'Battery Fault' host processor input.

> **Note:** If ADPTR_IN is active, nDB is not asserted and any of the actions described above relative to dead-battery detection will not take place.

The VBAT output is provided for use in Intel PXA27x or other applications requiring a power source during Sleep conditions. An internal switch connects the voltage from SW[2]IN to VBAT when SW[2] is active and in regulation. Otherwise, the switch supplies the VBAT output from BATBU.

Thermal Shutdown

While in ACTIVE mode, the FS1610 monitors its junction temperature to prevent possible damage to the IC due to thermal overload. There are two over-temperature conditions that are monitored. If the junction temperature exceeds T_{TAL} this state is latched and nINTR is asserted (if so programmed) so that the processor can perform an orderly shutdown of high power supplies. If the junction temperature exceeds T_{TSD} then all power supply channels are shut off immediately, nRSTO is asserted and the FS1610 transitions to the SHUTDOWN state.

Hysteresis is built into each thermal threshold to prevent multiple redundant alarms.

INTERRUPTS

The FS1610 provides an interrupt capability that can be used to alert the host of conditions requiring its attention, such as a low battery condition, a power rail fault or an RTC alarm.

The interrupt facility is handled by serial commands. Table 9 provides an overview of those commands. The commands dealing with interrupts are:

- Get Status: Shows current status of the device. Additional bytes in this command are related to the supply fault event and show the specific power rails in fault, if any.

- Clear Status: Clears designated bits in the device status register.
- Enable/Disable Interrupt: Used to enable selected status conditions to assert the nINTR output from the device.

All status bits are cleared and interrupts are disabled during a cold-start power up. Subsequent to this, the enabled/disabled interrupt status is saved when the chip goes to SHUTDOWN state and automatically restored when the chip next transitions to ACTIVE state. The nINTR signal itself is active only during READY, LOWPOWER and ACTIVE states.

Refer to the Host Serial Interface User Manual for a complete list of status conditions and a full description of all commands.

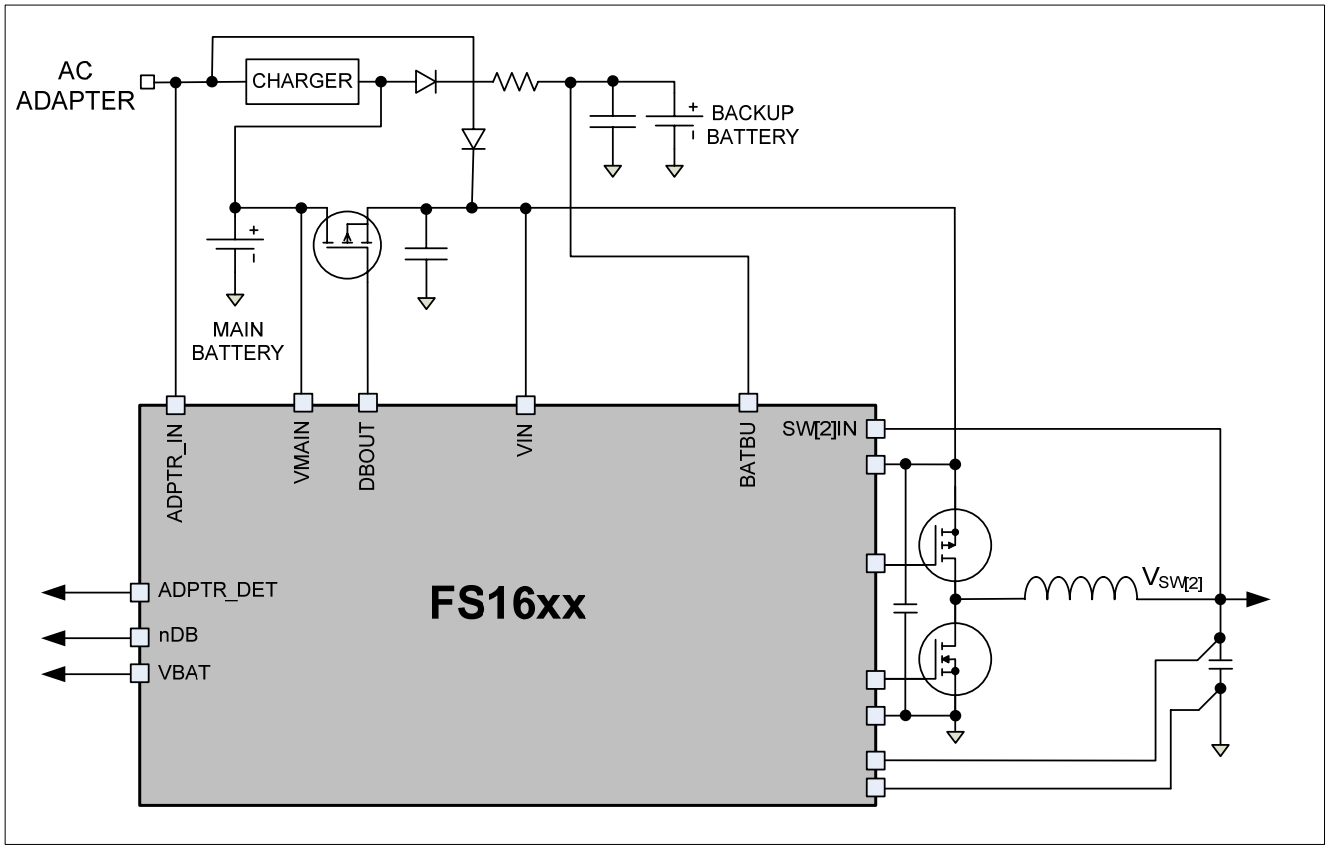


Figure 21. Battery Switching Circuit

PROGRAMMING

Programming of the FS1610 is done via a set of registers that configure, control and provide status for the device. These registers are subdivided into several classes.

Configuration Registers

These are read from the internal EEPROM at power-up and set various options for device operation. These configuration options can not be changed by host commands during operation.

Channel Control Registers

These have an initial setting that is loaded from the EEPROM at power-up, but can be written by the host processor via serial interface commands during device operation. These registers are specific to a power channel, although different types of channels may have different registers.

Device Control Registers

These registers control chip functions that are not typically channel-specific. They have an initial setting that is loaded from the EEPROM at power-up, but can be written by the host processor via the serial interface during device operation.

Device Status Registers

These provide device status to the host processor. The status is transmitted to the host via the serial interface in response to a status read command.

SERIAL COMMANDS

The serial interface between the host CPU and the FS1610 is a command/response interface. The FS1610 acts as a slave device on the serial bus and never sends an unsolicited message to the host. The host issues commands and the FS1610 responds.

Commands range from three to eight bytes in length and responses from four to eight bytes in length. Table 8 summarizes the serial command and response structures. Table 9 provides an overview of the commands and corresponding responses.

Additional detail is in the HSI User Manual that is available upon request.

Table 8. FS1610 Command/Response Structure

Byte	Command	Response
1	Number of additional bytes in command	Number of additional bytes in response
2	Command code	Echo of Command code
3	Optional byte 1	ACK (0x00) or NAK (0xFF)
4	Optional byte 2	Optional byte 1
5	Optional byte 3	Optional byte 2
6	Optional byte 4	Optional byte 3
7	Optional byte 5	Optional byte 4
8	Checksum: 2's complement of sum of previous bytes	Checksum: 2's complement of sum of previous bytes

Table 9. FS1610 Command Set Overview

Class	Description	C/R	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
		C	Length	Command	Optional	Optional	Optional	Optional	Optional	Optional
		R	Length	Command	ACK/NAK	Optional	Optional	Optional	Optional	Optional
WDT	Enable/Disable WDT	C	0x03	0x00	enab/dis	Checksum	N/A			
		R	0x03	0x00	0x00	Checksum	N/A			
	Reset WDT	C	0x02	0x01	Checksum	N/A				
		R	0x03	0x01	0x00	Checksum	N/A			
INT	Get Status	C	0x02	0x02	Checksum	N/A				
		R	0x07	0x02	0x00	INTRH status	INTRL status	SW Status	LDO Status	Checksum
	Enable/Disable Interrupt	C	0x04	0x03	INTRH ena/dis	INTRL ena/dis	Checksum	N/A		
		R	0x03	0x03	0x00	Checksum	N/A			
	Clear Interrupt	C	0x04	0x04	INTRH clear	INTRLclear	Checksum	N/A		
		R	0x03	0x04	0x00	Checksum	N/A			
ID	Read Device Rev/ID	C	0x02	0x05	Checksum	N/A				
		R	0x04	0x05	0x00	Rev/ID	Checksum	N/A		
RTC	Enable/Disable Alarm	C	0x03	0x42	enab/dis	Checksum	N/A			
		R	0x03	0x42	0x00	Checksum	N/A			
	Read Alarm Time	C	0x02	0x43	Checksum	N/A				
		R	0x07	0x43	0x00	MSB alarm	...	...	LSB alarm	Checksum
	Write Alarm Time	C	0x06	0x44	MSB alarm	...	...	LSB alarm	Checksum	N/A
		R	0x03	0x44	0x00	Checksum	N/A			
	Read RTC Time	C	0x02	0x47	Checksum	N/A				
		R	0x07	0x47	0x00	MSB RTC	...	...	LSB RTC	Checksum
	Write RTC Time	C	0x06	0x48	MSB RTC	...	...	LSB RTC	Checksum	N/A
		R	0x03	0x48	0x00	Checksum	N/A			
POWER	Read Voltage	C	0x04	0x61	Pin, Rail, VIN	inst/avg VIN	Checksum	N/A		
		R	0x05	0x61	0x00	MSB mV	LSB mV	Checksum	N/A	
	Set Voltage	C	0x06	0x62	Pwr Rail ID	MSB mV	LSB mV	modifier	Checksum	N/A
		R	0x03	0x62	0x00	Checksum	N/A			
	Set Current	C	0x06	0x64	SW[6] only	MSB mA	LSB mA	modifier	Checksum	N/A
		R	0x03	0x64	0x00	Checksum	N/A			
	Enable/Disable Power Rail Group	C	0x04	0x65	1, 2, 3, 4, 5	enab/dis	Checksum	N/A		
		R	0x03	0x65	0x00	Checksum	N/A			
	Enable/Disable Specific Power Rail	C	0x04	0x66	Pwr Rail ID	enab/dis	Checksum	N/A		
		R	0x03	0x66	0x00	Checksum	N/A			
	Set a Specific Power Rail to Standby/Normal	C	0x04	0x69	Pwr Rail ID	norm/stby	Checksum	N/A		
		R	0x03	0x69	0x00	Checksum	N/A			
	Shutdown	C	0x02	0x6B	Checksum	N/A				
		R	0x03	0x6B	0x00	Checksum	N/A			
	Set PWM of WLED Driver	C	0x03	0x6D	0 - 7	Checksum	N/A			
		R	0x03	0x6D	0x00	Checksum	N/A			
	Read Internal POK Status for All Rails	C	0x02	0x6E	Checksum	N/A				
		R	0x05	0x6E	0x00	SW Status	LDO Status	Checksum	N/A	
	Set POK Configuration	C	0x04	0x6F	Monitored SW	Monitored LDO	Checksum	N/A		
		R	0x03	0x6F	0x00	Checksum	N/A			
EEPROM	Write User EEPROM Segment Byte	C	0x04	0x06	Byte address	Byte Data	Checksum	N/A		
		R	0x03	0x06	0x00	Checksum	N/A			
	Read User EEPROM Segment Byte	C	0x03	0x07	Byte address	Checksum	N/A			
		R	0x04	0x07	0x00	Byte Data	Checksum	N/A		

Note: Responses are shown for the ACK case. For any NAK, the response will be :

0x03	Command	0xFF	Checksum

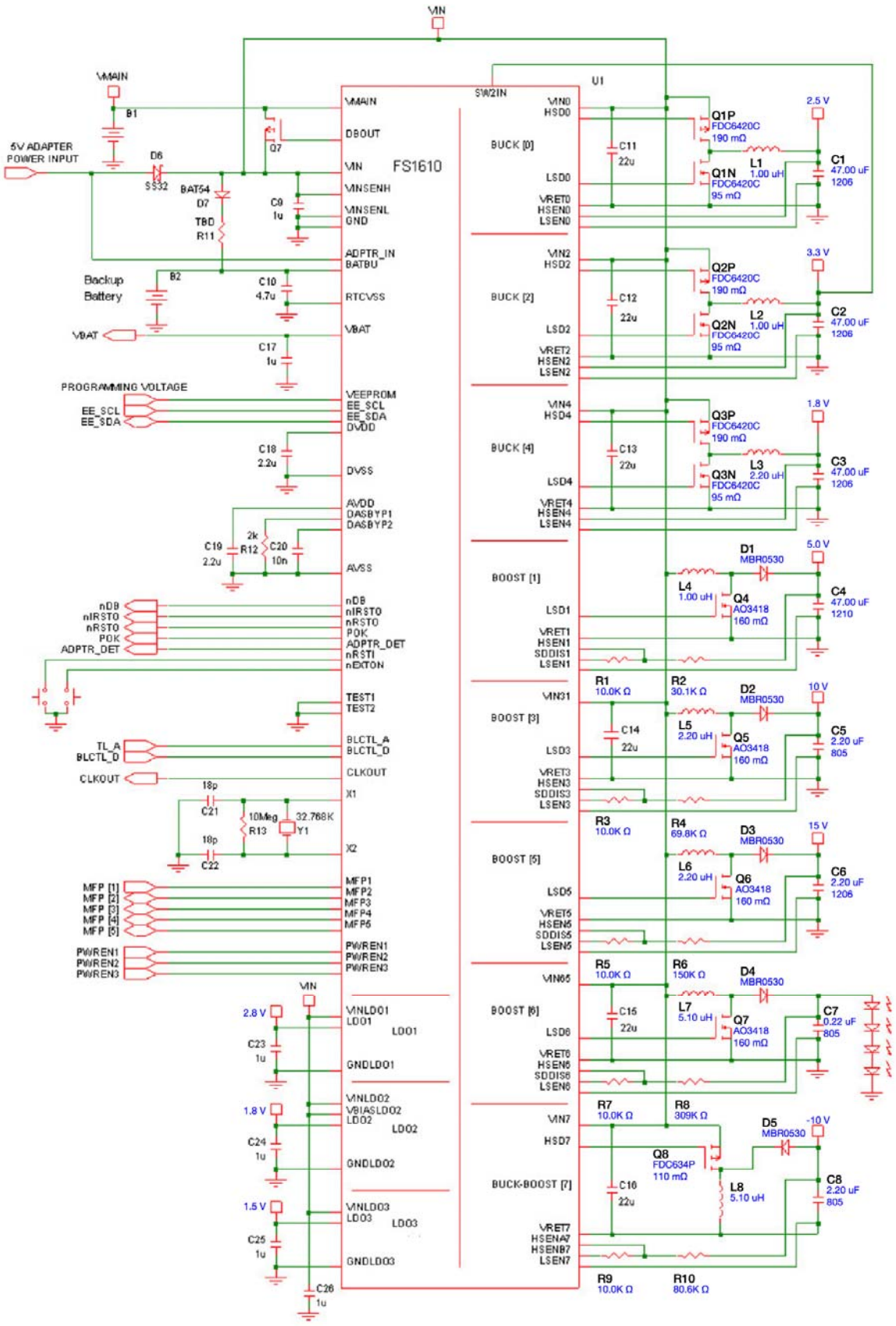
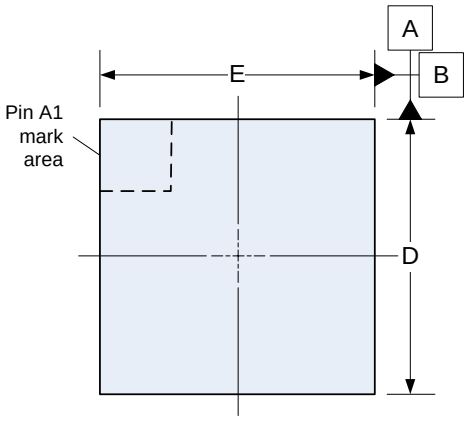
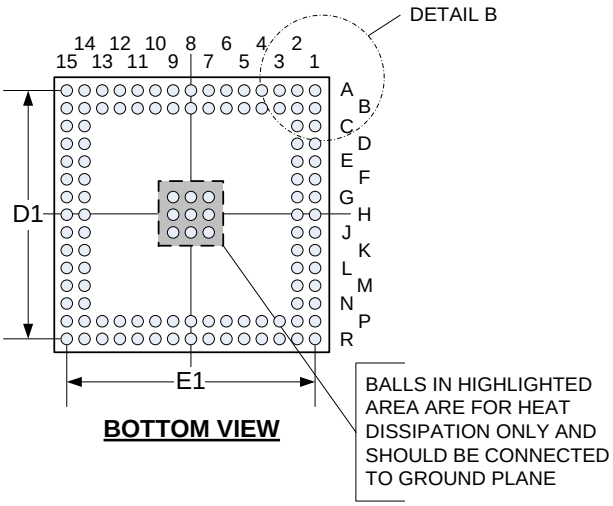


Figure 22. Typical FS1610 Configuration

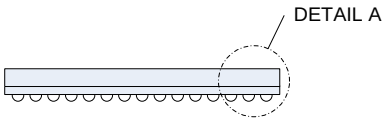
PACKAGE MECHANICAL CHARACTERISTICS



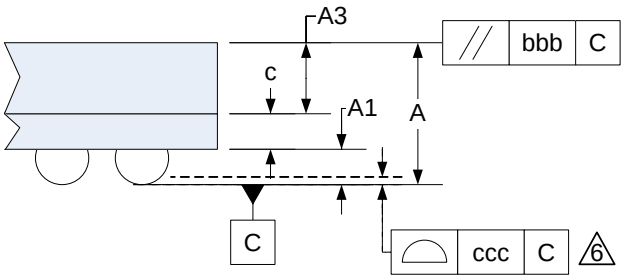
TOP VIEW



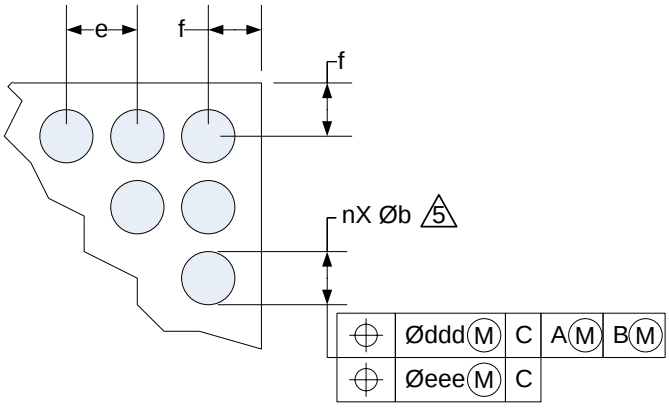
BOTTOM VIEW



SIDE VIEW



DETAIL A

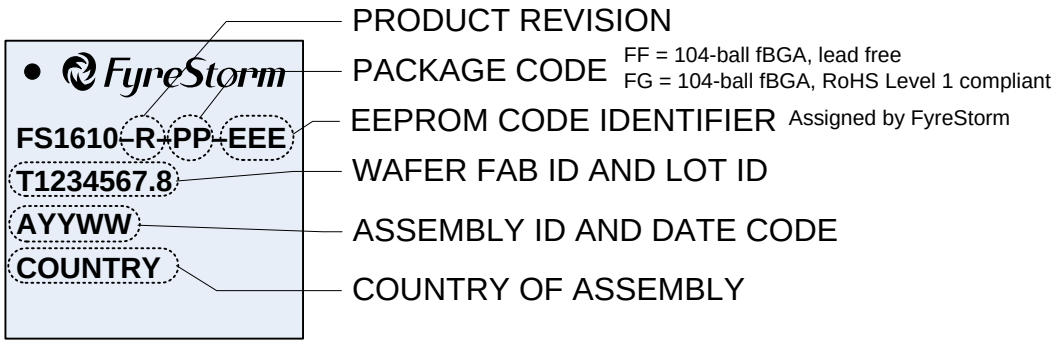


DETAIL B

DIMENSIONAL REFERENCES			
REF.	MIN	NOM	MAX
A	0.87	1.19	1.27
A1	0.17	0.22	0.27
A3	0.50	0.60	0.70
D	7.80	8.00	8.20
D1		7.00 BSC	
E	7.80	8.00	8.20
E1		7.00 BSC	
b	0.25	0.30	0.35
bbb			0.20
c	0.20	0.30	0.36
ccc		0.08	
ddd			0.15
e		0.50 BSC	
eee			0.05
f	0.40	0.50	0.60
M		15	
N		104	

1. Dimensioning and tolerancing per ASME Y14.5-1994.
2. All dimensions are in millimeters.
3. Dimension “e” represents the solder ball grid pitch.
4. Symbol “M” represents the basic solder ball matrix size and symbol “N” is the actual number of balls after depopulating.
5. Dimension “b” is measured at the maximum solder ball diameter in a plane parallel to Datum C.
6. Primary Datum C is defined by the crowns of the solder balls.
7. Package surface shall be matte finish Charmilles 24 to 27.
8. Substrate material base is BT resin.
9. The outline drawing is referenced to JEDEC specification MD-207, issue G.
10. Ball matrix variation CR-2.

PACKAGE MARKING (NOT TO SCALE)



COMPONENT AND PCB LAYOUT GUIDELINES

Careful component selection and proper PC board layout techniques are very important for successful power management design. MOSFETs must have the right breakdown voltage, threshold voltage and RDS_{ON}. Inductors must not saturate on peak current (significantly higher than output current). Capacitors must use the right dielectric and be properly de-rated. The PC layout must implement the FS1610 input/output voltage sense strategy correctly and be grounded properly. Improper components or poor layout can affect performance and disrupt system operation if the following guidelines are not followed.

- **MOSFETs:**
- RDS_{ON}: 50 milliOhm minimum to 200 milliOhm maximum at V_{GS} = 2.5 V.
- Buck Channels: V_{DS} = 8 V minimum to 20 V maximum.
- Boost Channels < 20 V or up to 5 White LEDs, Buck-Boost Channel < -15 V:
  - o V_{DS} = 25 V.
- Boost Channels 20 V to 25 V or 6 White LEDs, Buck-Boost Channel -15 V to -20 V:
  - o VDS = 30 V.
- For Boost channel > 25 V or more than 6 White LEDs, Buck-Boost channel <-20 V:
  - o Contact FyreStorm Applications Engineering.
- **Inductors**
- For most applications, use inductors approximately 3.2 mm x 3.2 mm per side such as Panasonic ELL3GM Series or equivalent.
- Inductor selection can be further optimized for smallest size or highest efficiency by contacting Fyre Storm Applications Engineering.
- **Capacitors**
- Output and bypass capacitors should always be ceramic with a voltage rating at least 50% higher than maximum output voltage. Electrolytic capacitors must not be used (ESR is too high).
- DVDD, AVDD, VBAT, BATBU bypass capacitors should be 0603 case size or higher (capacitance degrades with voltage in smaller case sizes).
- **Component Placement**
- Keep crystal input at least 4 mm away from all power FETs, diodes and inductors.
- Place bypass capacitors near FS1610 package.
- For buck channels 0, 2, 4, bypass capacitors should be between FS1610 and FETs.
- For all other switching channels, bypass capacitors should be between FS1610 and inductor.
- Place input capacitor near balls A6 and A7.
- For each channel place MOSFET (and diode) on same layer as inductor.
- Place buck channels (0, 2, 4) near balls J15 to P15.
- Place boost channels (1, 3, 5, 6) near balls B15 to H15.
- Place buck boost channel (7) near ball B15.
- Place sense resistors near balls M1 to R9.
- **There should be one ground plane split such that all VRET[x] returns are in one half and all other returns are in the other half (including DVSS and AVSS).**
- **For layouts with no ground planes (not recommended), tie all output channels together at the output capacitors with a star connection. From this star connection, run a ground trace to all FS1610 signal, digital and LDO ref-**

erences. Run a separate trace to each output RET[x] pad.

- **If using dual or complementary MOSFETs for two different channels, channels should be adjacent and output voltages should be of similar voltage rating.**
- **Minimize the loop areas of each channel including bypass capacitor, MOSFET, diode, inductor, output capacitor and return path.**
- **Keep switch net short and on one layer with no vias:**
  - Buck (0, 2, 4) switch net connects 2 MOSFET drains and inductor.
  - Boost (1, 3, 5, 7) switch net connects MOSFET drain, diode anode and inductor.
  - Buck-Boost (7) switch net connects MOSFET drain, diode cathode and inductor.
- **Wide traces on all switch nets: 20 mil (0.5 mm) average and very short.**
- **Wide traces on all power/supply/return/ref: 20 mil/ (0.5mm) average**
- **Multiple vias should be used for power FETs, diodes, inductors and output capacitors to reduce impedance**
- **Output and bypass capacitors: route traces directly to capacitor pad. Do not add traces in series with capacitors.**
- **All sense nets: do not route directly beneath power FETs, diodes or inductors. Use ground plane as intermediate shield between sense nets and FETs, diodes, and inductors.**
- **Input capacitor sense:**
  - Route VINSENH directly to positive side of input capacitor.
  - Route VINSENL directly to negative side of input capacitor.
- **Buck channels 0, 2, 4 sense:**
  - Route HSEN[x] net directly to output capacitor positive side.
  - Route LSEN[x] net directly to output capacitor ground side.
- **Boost channels 1, 3, 5, 6 sense:**
  - Route divider resistor net directly to output capacitor positive side.
  - Route LSEN[x] net directly to output capacitor ground side.
- **Buck-boost channel 7 sense:**
  - Route divider resistor net directly to output capacitor negative voltage.
  - Route LSEN[x] net directly to output capacitor ground side.
- **Test access:**
  - For fast design optimization, exposed connections to all balls (except C2, G2, H14, R3) should be available on either top or bottom layer.
- **Spare Pad Fields:**
  - If space permits, add spare pad fields for quickly breadboarding new circuits.

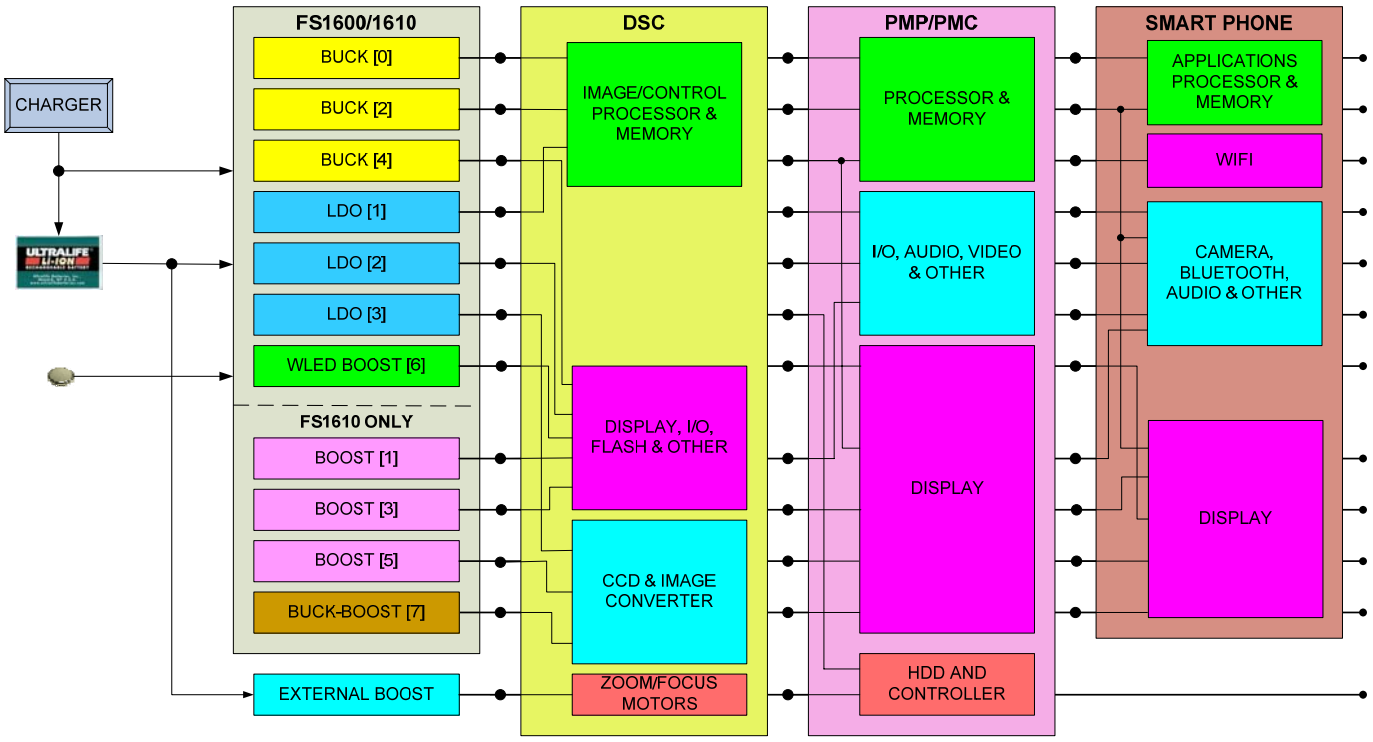


Figure 23. Typical Applications of the FS16xx Power Management Controller

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