FORESEE®

SPINAND
FS35ND04G-S2Y2
Datasheet

M-00140

Rev 1.4

Revision History:

Rev.	Date	Changes	Remark	Edited by
1.0	2019/11/26	Basic spec and architecture	Initial release	Cisu.Shi
1.1	2019/12/25	Removed Continuous read mode		Cisu.Shi
1.2	2020/8/4	Revised the descriptions of performance timing and removed the function of SR1-L		Cisu.Shi
1.3	2021/3/22	Revised some descriptions of Device Reset(FFh) & One Time Program Lock Bit (OTP-L) & tCH1 & tCL1.		Cisu.Shi
1.4	2021/4/23	Revised some descriptions of VIL & VIH.		Cisu.Shi

Contents

1. INTRODUCTION

1.1. General Description

The FS35ND04G-S2Y2 is a 4G-bit (512M-byte) SPI (Serial Peripheral Interface) NAND Flash memory, with advanced write protection mechanisms. The FS35ND04G-S2Y2 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O option.

1.2. Device Features

Voltage Supply
- V_{CC}: 3.3V (2.7V ~ 3.6V)

Organization
- Memory Cell Array : (512M + 16M) Byte
- Page Size : (2K + 64) Byte
- Data Register : (2K + 64) Byte
- Block Erase : (128K + 4K) Byte
- Device size : 4Gb(4096 blocks)

Serial Interface
- Standard SPI : CLK, CS#, DI, DO, WP#
- Dual SPI : CLK, CS#, DQ0, DQ1, WP#
- Quad SPI : CLK, CS#, DQ0, DQ1, DQ2, DQ3

High Performance
- 108MHz for fast read
- Quad I/O data transfer up to 432Mbits/s
- 2K-Byte cache for fast random read

Advanced Security Features
- Write protect all/portion of memory via software
- ECC status bits indicate ECC results
- bad block management and LUT(1) access
- Power Supply Lock-Down and OTP protection
- 2KB Unique ID and 2KB parameter pages
- Ten 2KB OTP pages (2)

Program/Erase/Read Speed
- PAGE PROGRAM time : 430μs typical
- BLOCK ERASE time : 3.5ms typical
- PAGE READ time : 180μs typical

Advanced Features for NAND
– Internal ECC option, per 512 bytes
– Promised golden block0

Package
- WSON8 (8x6mm)

Reliability
- 100,000 Program/Erase Cycles(Typical)
- 10 Year Data retention (with 4bit/536Byte ECC)

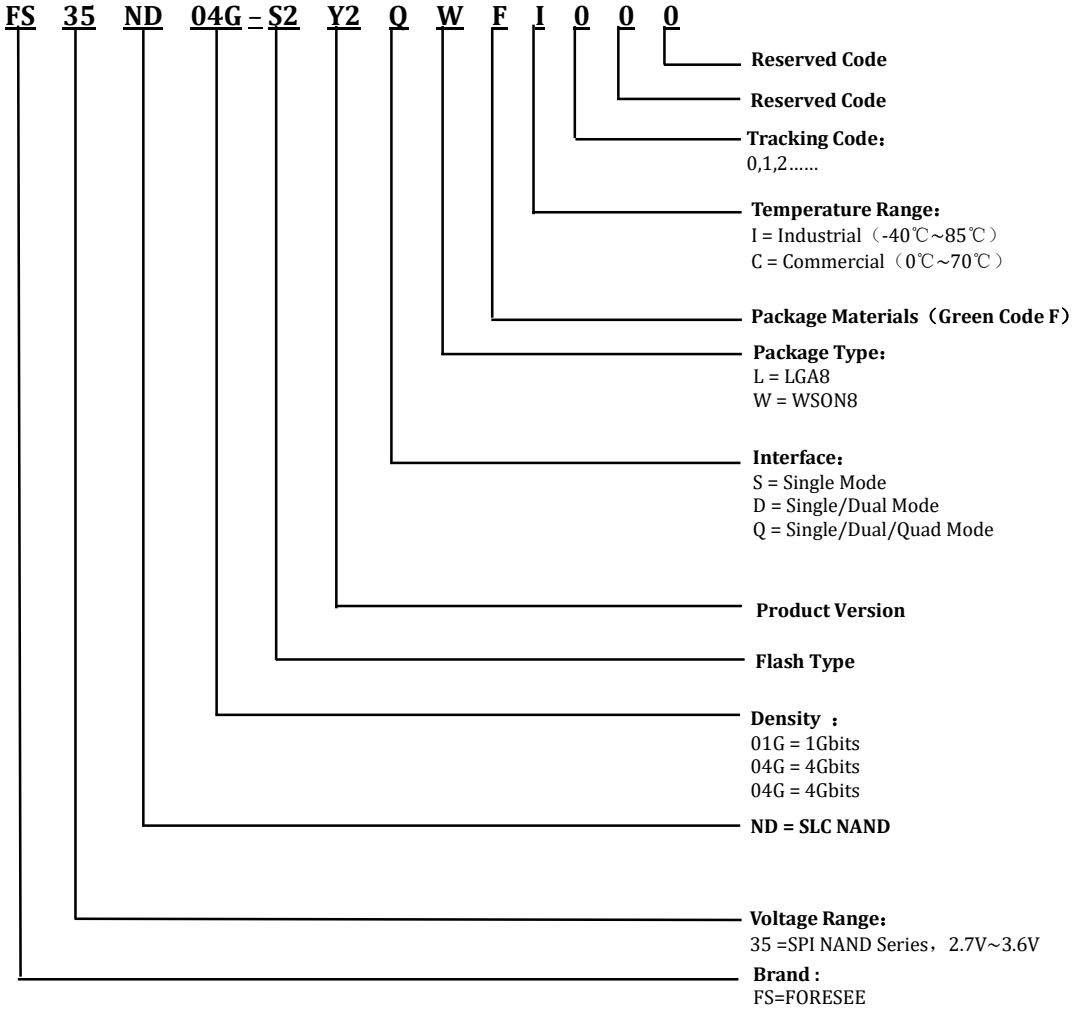
Notes:
1. LUT stands for Look-Up Table.
2. OTP pages can only be programmed.

1.3. Product List

[Table 1] Product List

Part Number	MID	DID	Density	Package Type	Organization	Package Size(mm)	VCC Range
FS35ND04G-S2Y2QWFI000	CDh	EC11h	4Gb	WSON8	X1/X2/X4	8*6	2.7V ~ 3.6V

Marketing Part Number Chart



1.4. Connection Diagram

WSON8 (8x6mm)

Top View

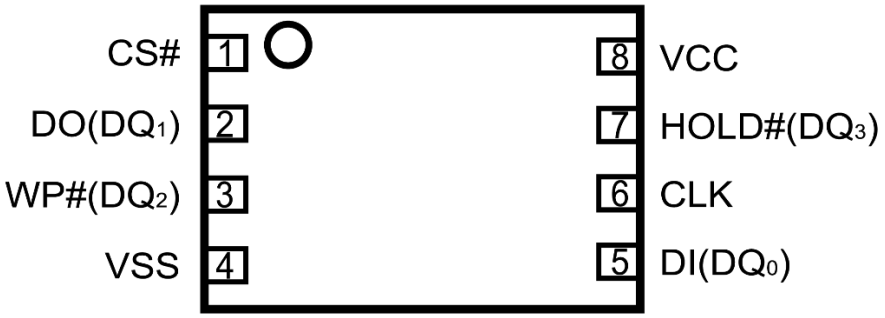


Figure 1-1 Pad Assignments

1.5. Pin Description

[Table 2] Pin Description

PIN NO.	PIN NAME	I/O	Pin Function
1	CS#	I	Chip Select Input
2	DO (DQ1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS	--	Ground
5	DI (DQ0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD# (DQ3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC	--	Power Supply

NOTE:
1) DQ0 and DQ1 are used for Dual SPI instructions.
2) DQ0 - DQ3 are used for Quad SPI instructions.

1.6. System Block Diagram

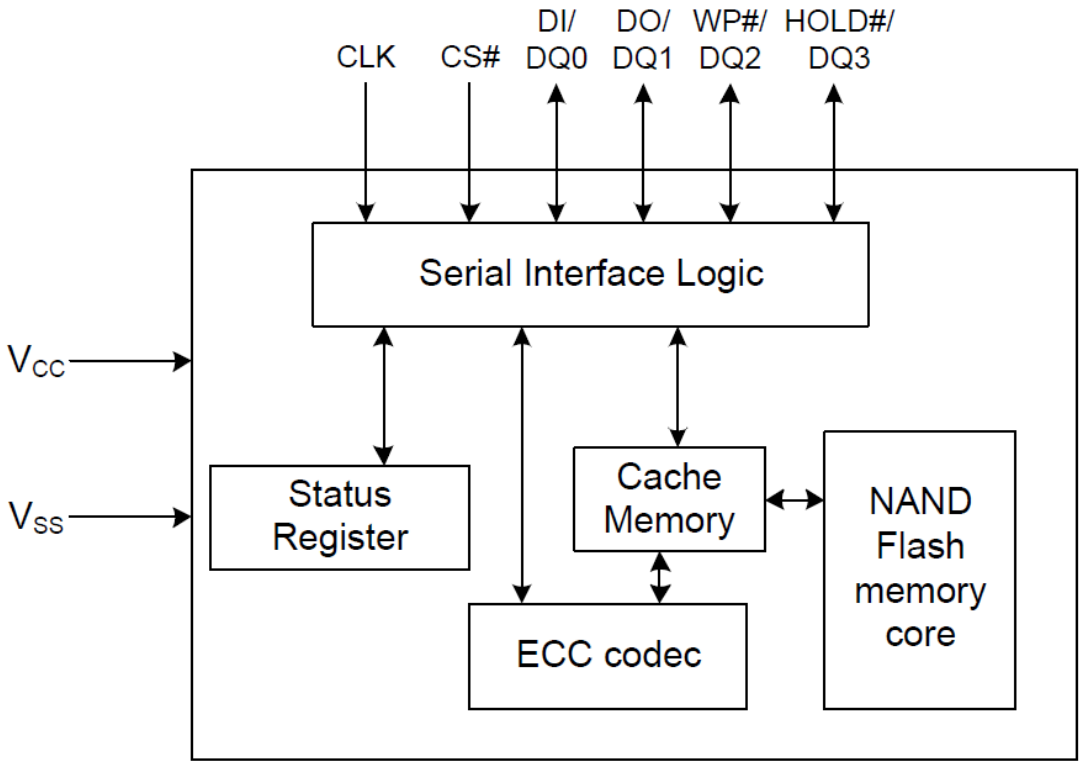


Figure 1-2 SPI NAND Flash Memory Block Diagram

1.7. Memory Mapping

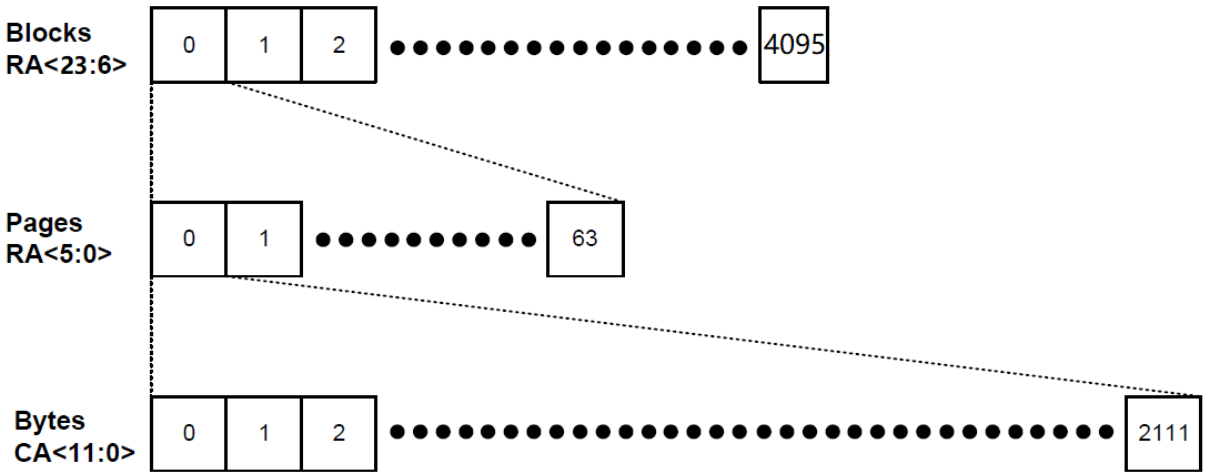


Figure 1-3 Memory Map

Note:
1) CA: Column Address. The 12-bit column address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are "out of bounds," do not exists in the device, and cannot be addressed.
2) RA: Row Address. RA<5:0> selects a page inside a block, and RA<23:6> selects a block.

[Table 3] Array Organization

Each device has	Each block has	Each page has	Unit
512M + 16M	128K + 4，K	2K + 64	Bytes
4096 x 64	64	--	Pages
4096	--	--	Blocks

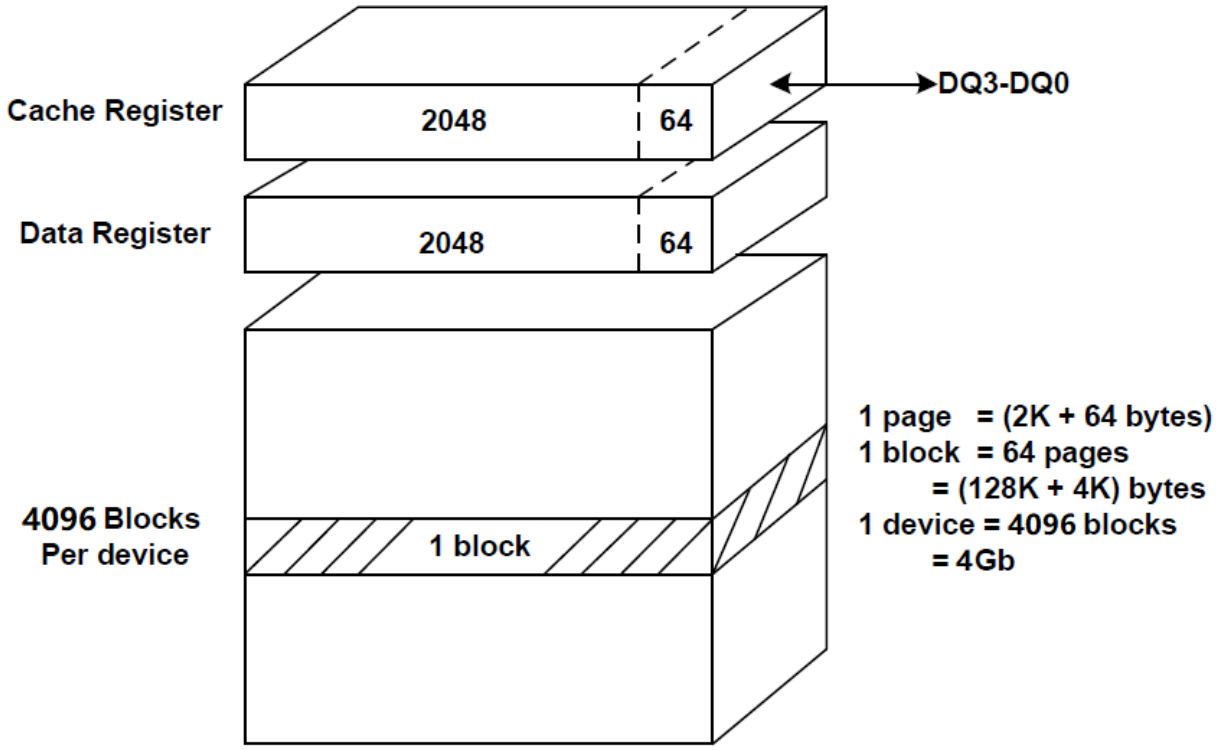


Figure 1-4 Array Organization

2. Device Operations

2.1. SPI Mode

2.1.1. Standard SPI

The FS35ND04G-S2Y2 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

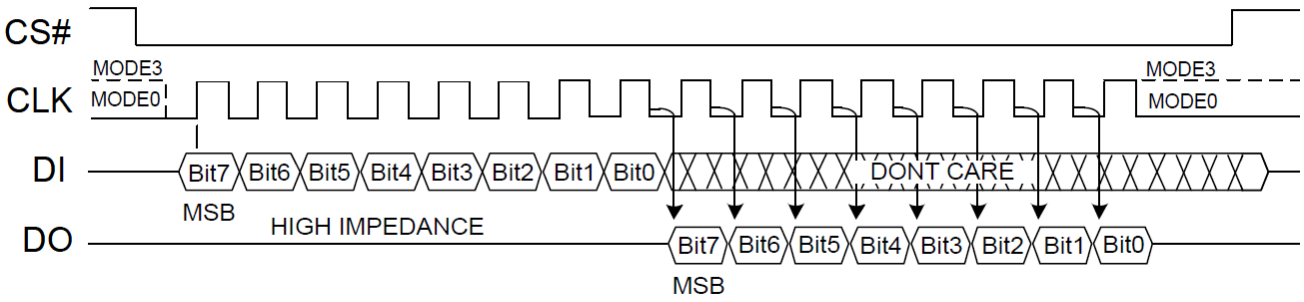


Figure 2-2 SPI SDR Modes Supported

2.1.2. Dual SPI

The FS35ND04G-S2Y2 supports Dual SPI operation when using the x2 and dual IO instructions. These instructions allow data to be transferred to or from the device at two times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ0 and DQ1.

2.1.3. Quad SPI

The FS35ND04G-S2Y2 supports Quad SPI operation when using the x4 and Quad IO instructions. These instructions allow data to be transferred to or from the device four times the rate of ordinary Serial Flash. When using Quad SPI instructions the DI and DO pins become bidirectional DQ0 and DQ1 and the WP # and HOLD# pins become DQ2 and DQ3 respectively. Quad SPI instructions require the Quad Enable bit (QE) to be set.

2.2. CS#

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ0, DQ1, DQ2, DQ3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program, read, reset or individual block lock / unlock cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

2.3. CLK

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the CLK signal. Data output changes after the falling edge of CLK.

2.4. Serial Input (DI) / DQ0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial CLK clock signal.

DI becomes DQ0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

2.5. Serial Output (DO) / DQ1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial CLK clock signal.

DO becomes DQ1 - an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

2.6. Write Protect (WP#) / DQ2

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte (2x128KB blocks) or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the WP# pin.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The WP# pin functions as a data I/O pin for the Quad SPI operations, as well as an active low input pin for the Write Protection function for SR-1. Refer to section 3.8.1 for detail information.

When WP-E=1, the device is in the Hardware Protection mode that WP# becomes a dedicated active low input pin for the Write Protection of the entire device. If WP# is tied to GND, all "Write/Program/Erase" functions are disabled. The entire device (including all registers, memory array, OTP pages) will become read-only. Quad SPI read operations are also disabled when WP-E is set to 1.

2.7. Hold (HOLD#) / DQ3

During Standard and Dual SPI operations, the HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low.

When a Quad SPI Read/Buffer Load command is issued, HOLD# pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finished. HOLD# (IO3) must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# input to float.

3. Command Definition

3.1. Command Set Tables

[Table 4] Instruction Set Table

Commands	OpCode	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Device RESET	**FFh**								
JEDEC ID	**9Fh**	Dummy	**CDh**	**ECh**	**11h**				
Read Status Register	**0Fh / 05h**	SR Addr	**S7-0**	**S7-0**	**S7-0**	**S7-0**	**S7-0**	**S7-0**	**S7-0**
Write Status Register	**1Fh / 01h**	SR Addr	S7-0						
Write Enable	**06h**								
Write Disable	**04h**								
BB Management (Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	**LBA0**	**LBA0**	**PBA0**	**PBA0**	**LBA1**	**LBA1**	**PBA1**
Block Erase	**D8h**	**PA23-16**	**PA15-8**	**PA7-0**					
Program Data Load (Reset Buffer)	**02h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad Program Data Load (Reset Buffer)	**32h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	Data-0 / 4	Data-1 / 4	Data-2 / 4	Data-3 / 4	Data-4 / 4	Data-5 / 4
Program Execute	**10h**	**PA23-16**	**PA15-8**	**PA7-0**					
Page Data Read	**13h**	**PA23-16**	**PA15-8**	**PA7-0**					
Read	**03h**	**CA15-8**	**CA7-0**	Dummy	**D7-0**	**D7-0**	**D7-0**	**D7-0**	**D7-0**
Fast Read	**0Bh**	**CA15-8**	**CA7-0**	Dummy	**D7-0**	**D7-0**	**D7-0**	**D7-0**	**D7-0**
Fast Read with 4-Byte Address	**0Ch**	**CA15-8**	**CA7-0**	Dummy	Dummy	Dummy	**D7-0**	**D7-0**	**D7-0**
Fast Read Dual Output	**3Bh**	**CA15-8**	**CA7-0**	Dummy	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**
Fast Read Dual Output with 4-Byte Address	**3Ch**	**CA15-8**	**CA7-0**	Dummy	Dummy	Dummy	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**
Fast Read Quad Output	**6Bh**	**CA15-8**	**CA7-0**	Dummy	**D7-0 / 4**	**D7-0 / 4**	**D7-0 / 4**	**D7-0 / 4**	**D7-0 / 4**
Fast Read Quad Output with 4-Byte Address	**6Ch**	**CA15-8**	**CA7-0**	Dummy	Dummy	Dummy	**D7-0 / 4**	**D7-0 / 4**	**D7-0 / 4**
Fast Read Dual I/O	**BBh**	**CA15-8 / 2**	**CA7-0 / 2**	Dummy / 2	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**
Fast Read Dual I/O with 4-Byte Address	**BCh**	**CA15-8 / 2**	**CA7-0 / 2**	Dummy / 2	Dummy / 2	Dummy / 2	**D7-0 / 2**	**D7-0 / 2**	**D7-0 / 2**
Fast Read Quad I/O	**EBh**	**CA15-8 / 4**	**CA7-0 / 4**	Dummy / 4	Dummy / 4	**D7-0 / 4**	**D7-0 / 4**	**D7-0 / 4**	**D7-0 / 4**
Fast Read Quad I/O with 4-Byte Address	**ECh**	**CA15-8 / 4**	**CA7-0 / 4**	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	Dummy / 4	**D7-0 / 4**

Notes:
1. Output designates data output from the device.
2. Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.
3. Page Address (PA) requires 24 bits. PA[23:6] is the address for 128KB blocks (total 4,096 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).
4. Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[9:0] & PBA[9:0] are effective Block Addresses. LBA[15:14] is used for additional information.
5. Status Register Addresses:
   Status Register 1 / Protection Register: Addr = A0h
   Status Register 2 / Configuration Register: Addr = B0h
   Status Register 3 / Status Register: Addr = C0h

6. Dual SPI Address Input (CA15-8 / 2 and CA7-0 / 2) format:

IO0 =	x,	x,	CA10,	CA8,	CA6,	CA4,	CA2,	CA0
IO1 =	x,	x,	CA11,	CA9,	CA7,	CA5,	CA3,	CA1

7. Dual SPI Data Output (D7-0 / 2) format:

IO0 =	D6,	D4,	D2,	D0,	……
IO1 =	D7,	D5,	D3,	D1,	……

8. Quad SPI Address Input (CA15-8 / 4 and CA7-0 / 4) format:

IO0 =	x,	CA8,	CA4,	CA0
IO1 =	x,	CA9,	CA5,	CA1
IO2 =	x,	CA10,	CA6,	CA2
IO3 =	x,	CA11,	CA7,	CA3

9. Quad SPI Data Input/Output (D7-0 / 4) format:

IO0 =	D4,	D0,	……
IO1 =	D5,	D1,	……
IO2 =	D6,	D2,	……
IO3 =	D7,	D3,	……

10. All Quad Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.
11. For all Read operations, as soon as /CS signal is brought to high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.

3.2. Initialization Operation

3.2.1. Device Reset (FFh)

The FS35ND04G-S2Y2 provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits. Once the Reset command is accepted by the device, the device will take approximately tRST to reset, depending on the current operation the device is performing, tRST can be 5us~500us. During this period, only 05h/0Fh (Read Status Register instruction) command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

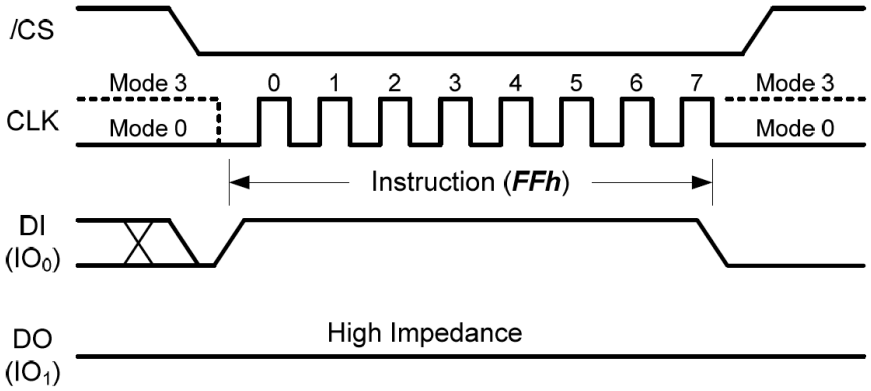


Figure 3-1 Device Reset Instruction

Default values of the Status Registers after power up and Device Reset

Register	Address	Bits	Shipment Default	Power Up after LUT is full	Power Up after OTP area locked	Power Up after SR-1 locked	After Reset command(FFh)
Protection Register	A0h	BP[3:0],TB	11111	11111	11111	FS35ND04G-S2Y2x(locked)	No Change
		SRP[1:0]	0 0	0 0	0 0	1 1(locked)	No Change
		WP-E	0	0	0	x(locked)	No Change
Configuration Register	B0h	OTP-L	0	0	1	0	Clear to 0 before OTP set
		OTP-E	0	0	0	0	0
		ECC-E	1	1	1	1	No Change
Status Register	C0h	LUT-F	0	1	0	0	No Change
		ECC-1	0	0	0	0	0
		ECC-0	0	0	0	0	0
		P-FAIL	0	0	0	0	0
		E-FAIL	0	0	0	0	0
		WEL	0	0	0	0	0
		BUSY	1 during tRST≥0	1 during tRST≥0	1 during tRST≥0	1 during tRST≥0	1 during tRST≥0

3.2.2. Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the CS# pin low and shifting the instruction code "9Fh" followed by 8 dummy clocks. The JEDEC assigned Manufacturer ID byte for FORESEE(CDh) and two Device ID bytes are then shifted out on the falling edge of CLK with most significant bit (MSB) first. For memory type and capacity values refer to Manufacturer and Device Identification table.

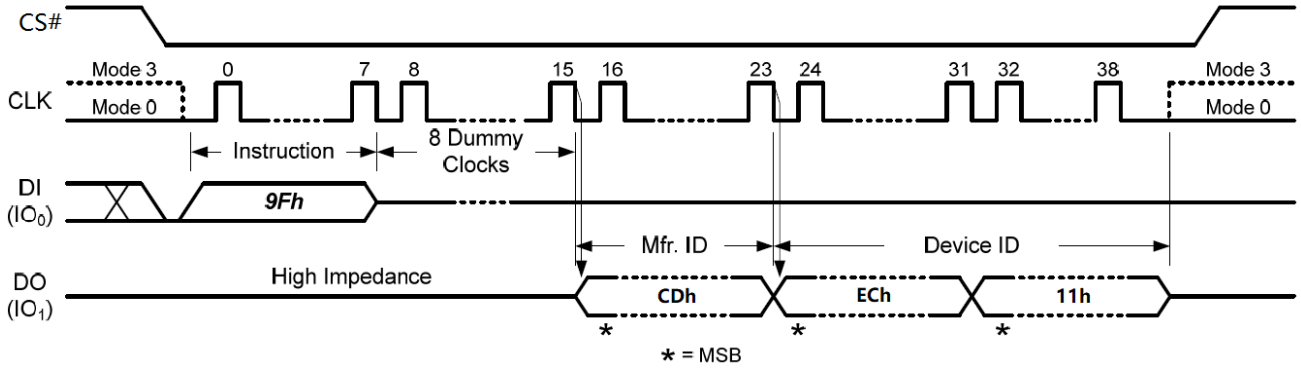


Figure 3-2 Read JEDEC ID Instruction

3.3. WRITE operation

3.3.1. WRITE ENABLE (WREN) (06h)

The Write Enable instruction sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program. Block Erase and Bad Block Management instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

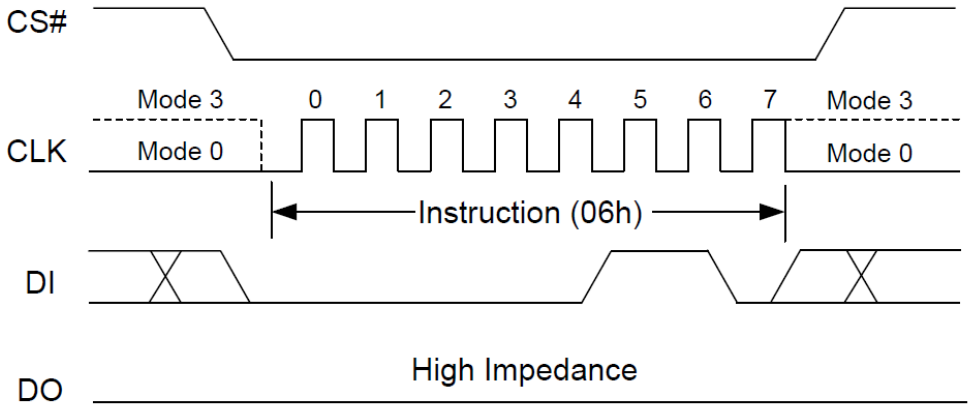


Figure 3-3 WRITE ENABLE (06h) Timing

3.3.2. WRITE DISABLE (WRDI) (04h)

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CS# low, shifting the instruction code "04h" into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Quad Page Program, Block Erase, Reset and Bad Block Management instructions.

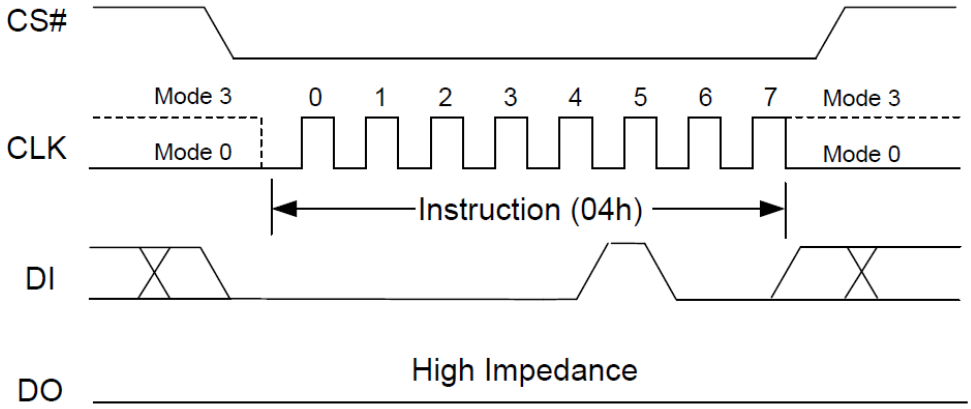


Figure 3-4 WRITE DISABLE (04h) Timing

3.4. PROGRAM Operation

3.4.1. Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 2,112 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Program operation involves two steps:

1. Load the program data into the Data Buffer.

2. Issue "Program Execute" command to transfer the data from Data Buffer to the specified memory page.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL= 1). The "Load Program Data" or "Random Load Program Data" instruction is initiated by driving the CS# pin low then shifting the instruction code "02h" or "84h" followed by a 16-bit column address (only CA[11:0] is effective) and at least one byte of data into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device.

Both "Load Program Data" and "Random Load Program Data" instructions share the same command sequence. The difference is that "Load Program Data" instruction will reset the unused the data bytes in the Data Buffer to FFh value, while "Random Load Program Data" instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

No matter internal ECC is enabled or disabled, all 2,112 bytes of data will be accepted. If the ECC-E bit is set to a 1, values of ECC-0 and ECC-1 bit of C0 Register will indicate the ECC status.

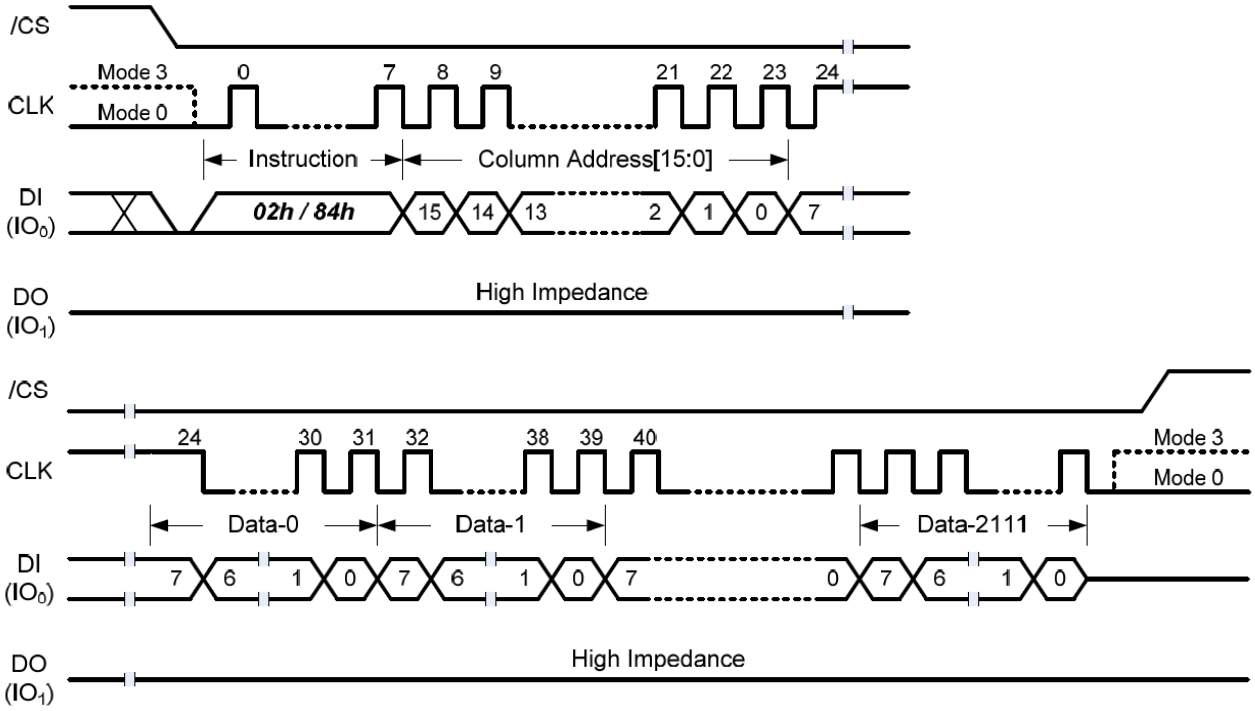


Figure 3-5 Load / Random Load Program Data Instruction

3.4.2. Quad Load Program Data (32h) / Quad Random Load Program Data (34h)

The "Quad Load Program Data" and "Quad Random Load Program Data" instructions are identical to the "Load Program Data" and "Random Load Program Data" in terms of operation sequence and functionality. The only difference is that "Quad Load" instructions will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer.
Both "Quad Load Program Data" and "Quad Random Load Program Data" instructions share the same command sequence. The difference is that "Quad Load Program Data" instruction will reset the unused the data bytes in the Data Buffer to FFh value, while "Quad Random Load Program Data" instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.
When WP-E bit in the Status Register is set to a 1, all Quad SPI instructions are disabled.

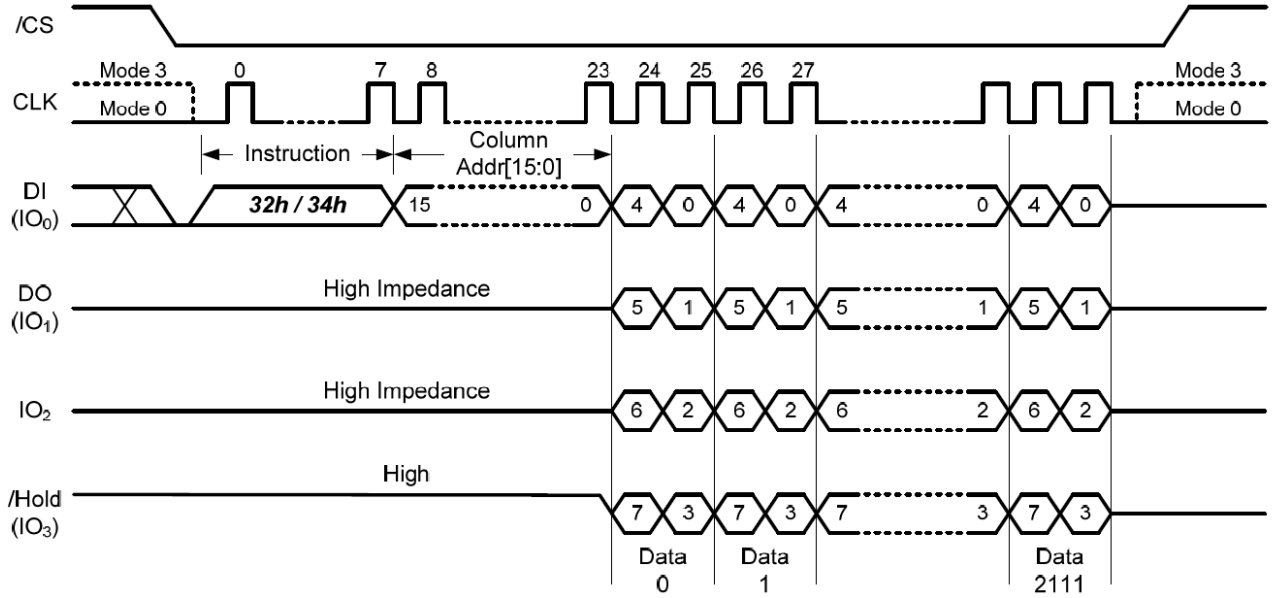


Figure 3-6 Quad Load / Quad Random Load Program Data Instruction

3.4.3. Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data are loaded into the 2,112-Byte Data Buffer , the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the CS# pin low then shifting the instruction code "10h" followed by the 24-bit Page Address into the DI pin.
After CS# is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tpp (See AC Characteristics). While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits. Only 1 partial page program times are allowed on every single page.
The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

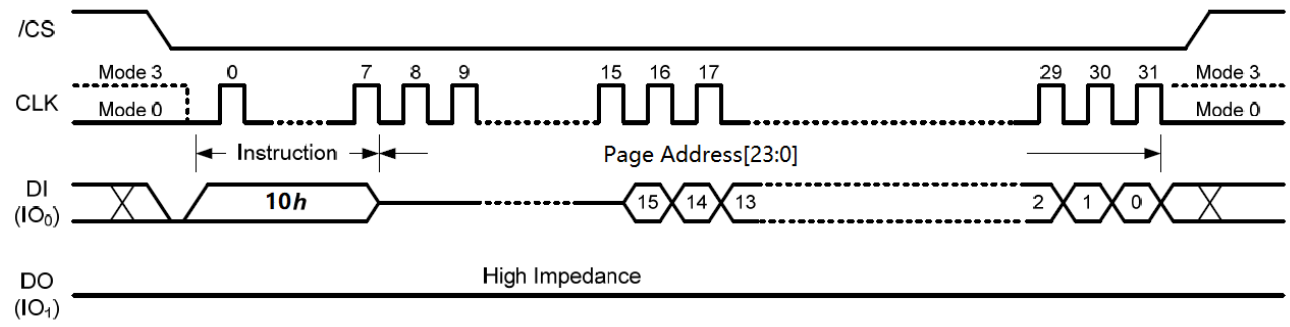


Figure 3-7 Program Execute Instruction

3.5. READ Operation

3.5.1. Page Data Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the 2,112-Byte Data Buffer. The instruction is initiated by driving the CS# pin low then shifting the instruction code "13h" followed by the 24-bit Page Address into the DI pin.
After CS# is driven high to complete the instruction cycle, the self-timed Read Page Data instruction will commence for a time duration of tRD (See AC Characteristics). While the Read Page Data cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Read Page Data cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the 2,112 bytes of page data are loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data.

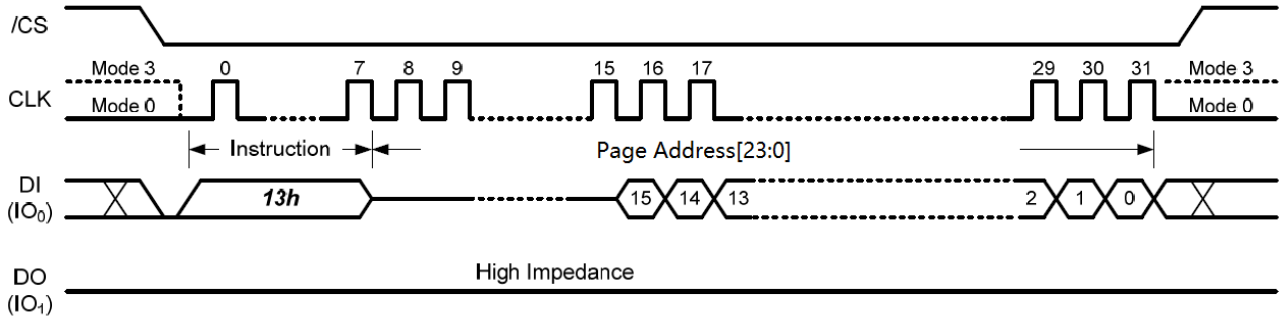


Figure 3-8 Page Data Read Instruction

3.5.2. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the CS# pin low and then shifting the instruction code "03h" followed by the 16-bit Column Address and 8-bit dummy clocks or a 24-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving CS# high.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

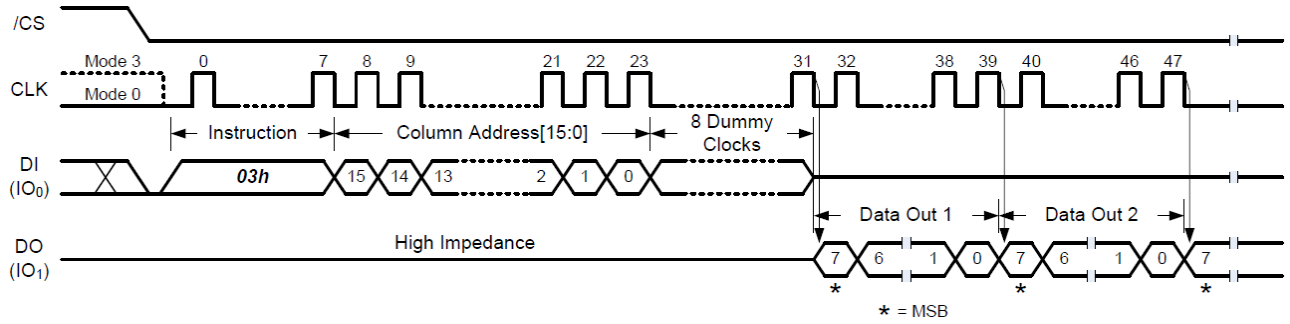


Figure 3-9 Read Data Instruction

3.5.3. Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the CS# pin low and then shifting the instruction code "0Bh" followed by the 16-bit Column Address and 8-bit dummy clocks or a 32-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving CS# high.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

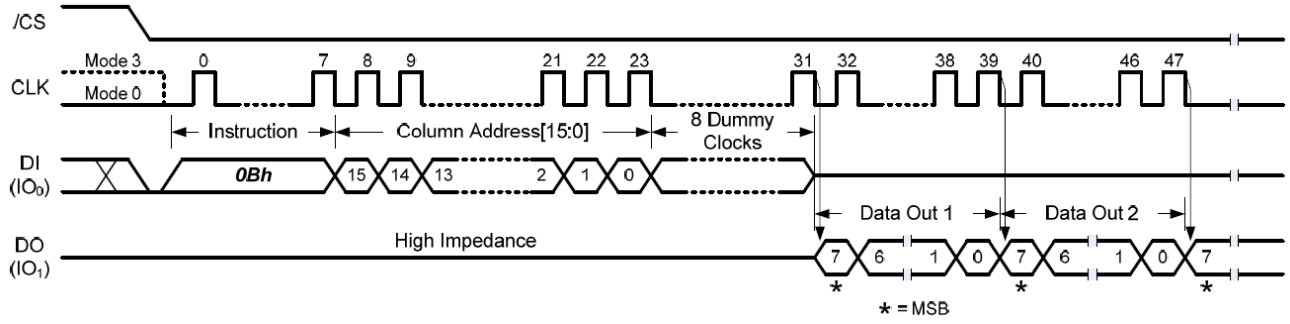


Figure 3-10 Fast Read Instruction

3.5.4. Fast Read with 4-Byte Address (0Ch)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the CS# pin low and then shifting the instruction code "0Ch" followed by the 16-bit Column Address and 24-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving CS# high.
The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

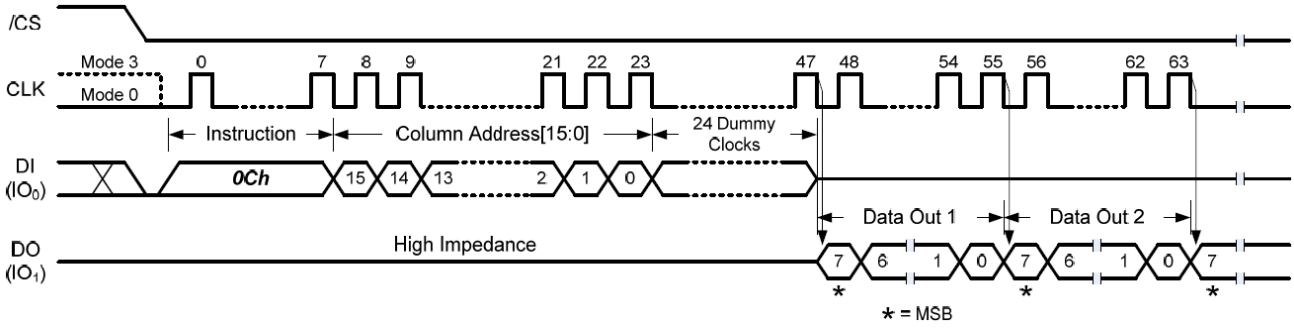


Figure 3-11 Fast Read with 4-Byte Address Instruction

3.5.5. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO0 and IO1. This allows data to be transferred at twice the rate of standard SPI devices.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

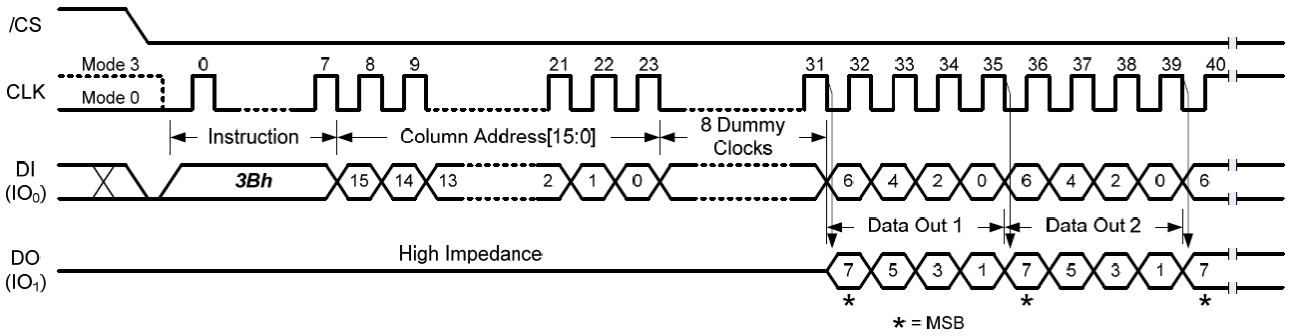


Figure 3-12 Fast Read Dual Output Instruction

3.5.6. Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output (3Ch) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO0 and IO1. This allows data to be transferred at twice the rate of standard SPI devices.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

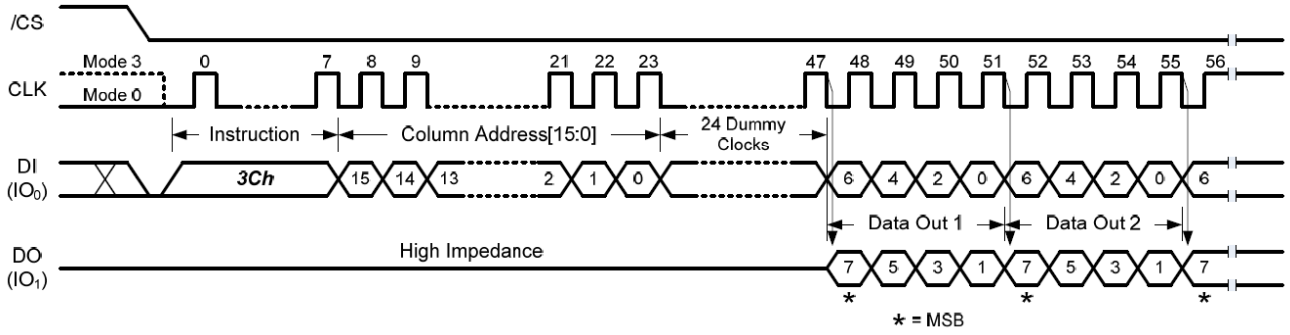


Figure 3-13 Fast Read Dual Output with 4-Byte Address Instruction

3.5.7. Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

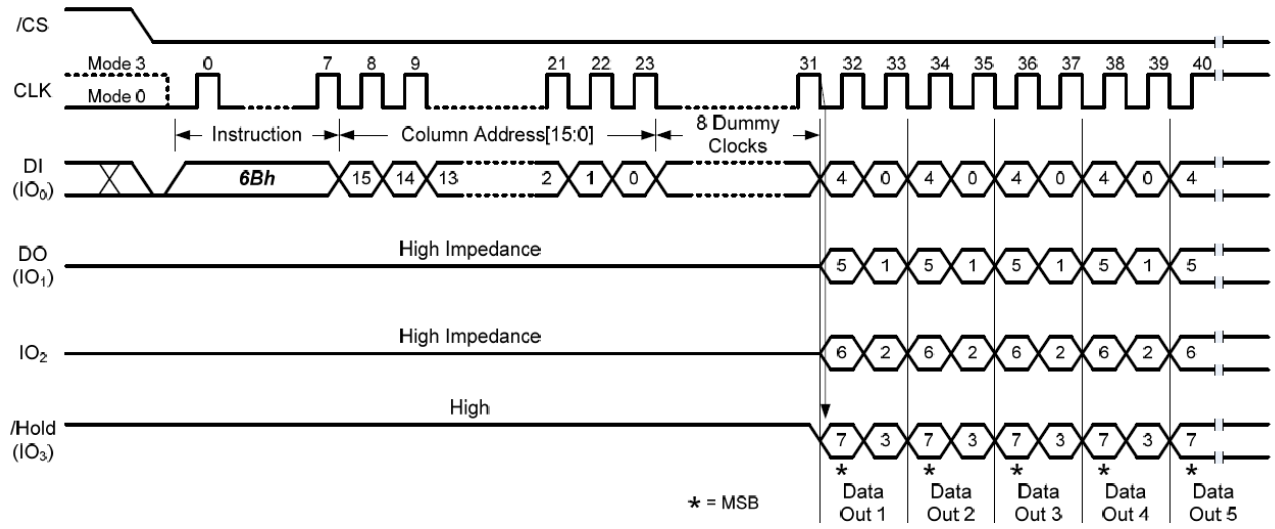


Figure 3-14 Fast Read Quad Output Instruction

3.5.8. Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output (6Ch) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

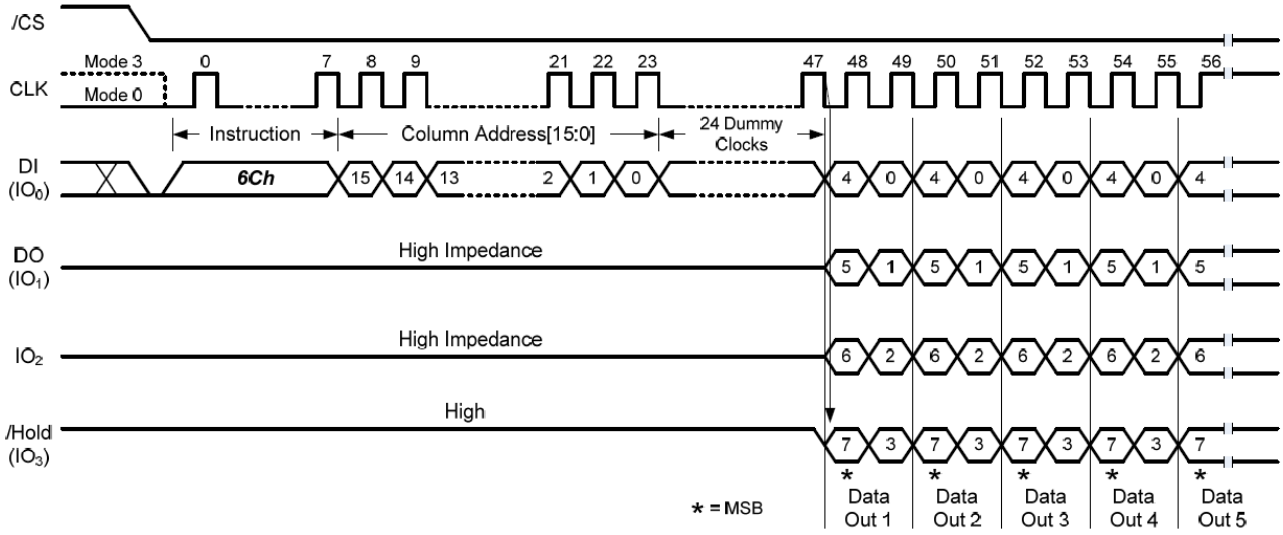


Figure 3-15 Fast Read Quad Output with 4-Byte Address Instruction

3.5.9. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

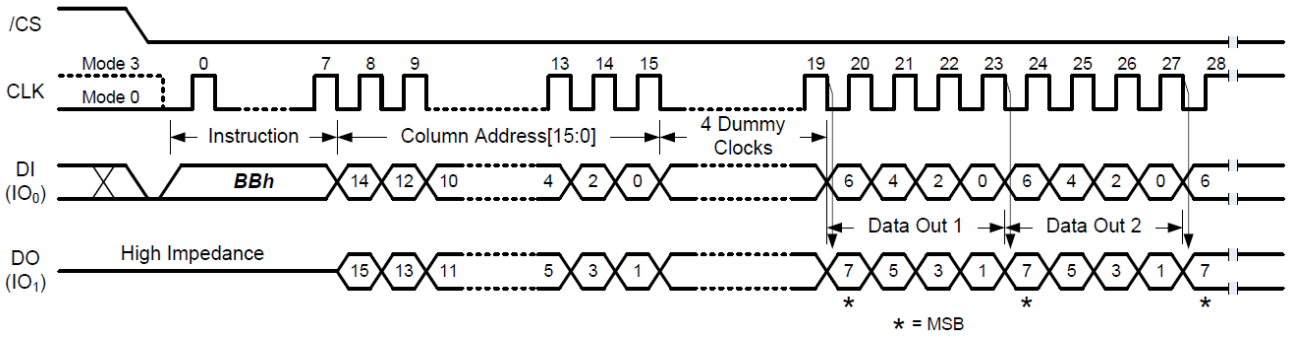


Figure 3-16 Fast Read Dual I/O Instruction

3.5.10. Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O (BCh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

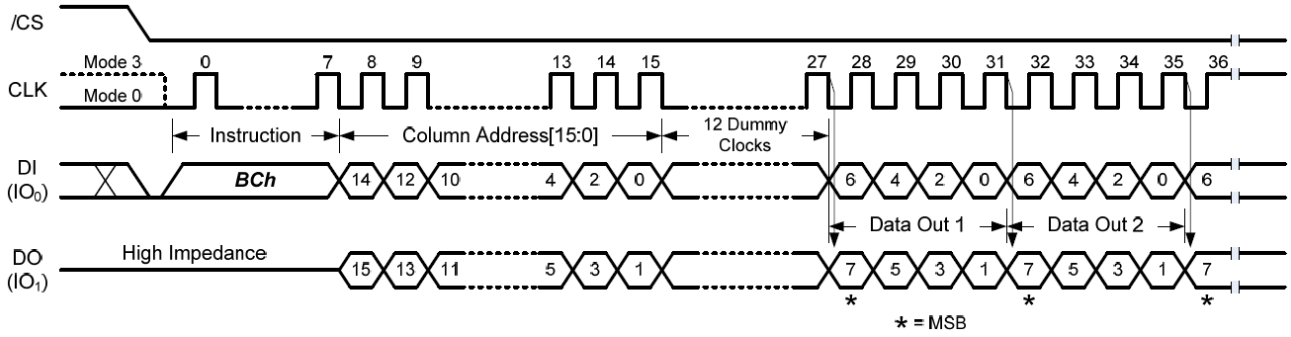


Figure 3-17 Fast Read Dual I/O with 4-Byte Address Instruction

3.5.11. Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.
The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.
When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

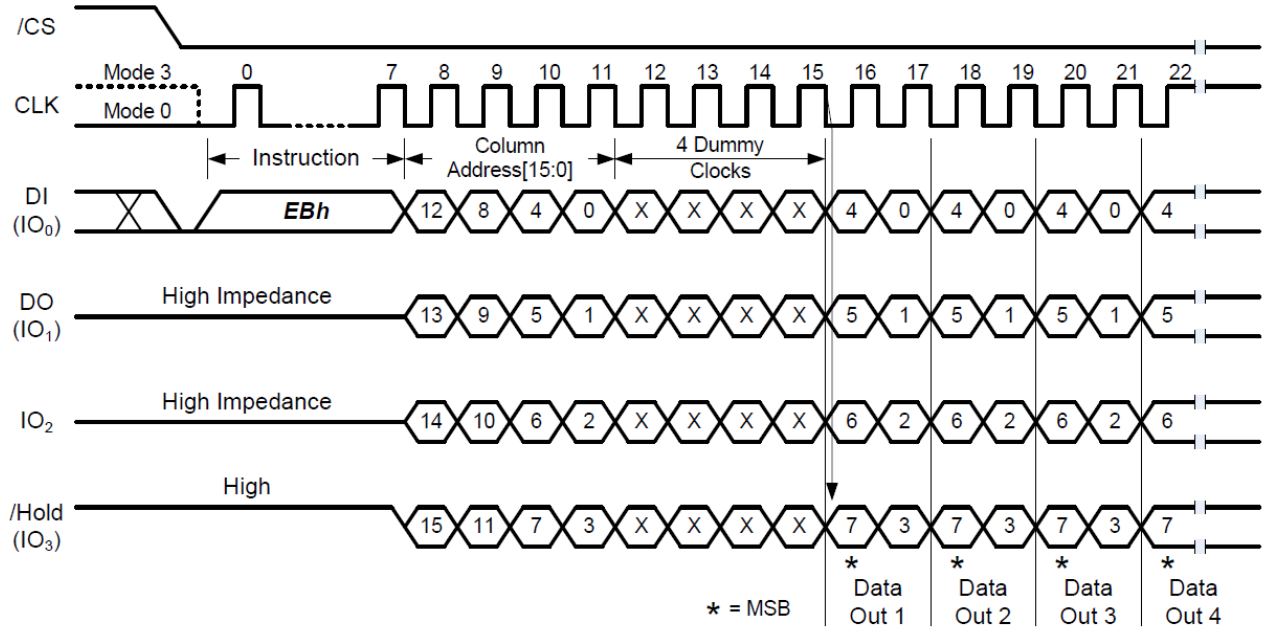


Figure 3-18 Fast Read Quad I/O Instruction

3.5.12. Fast Read Quad I/O with 4-Byte Address (ECh)

The Fast Read Quad I/O (ECh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.
The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.
When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

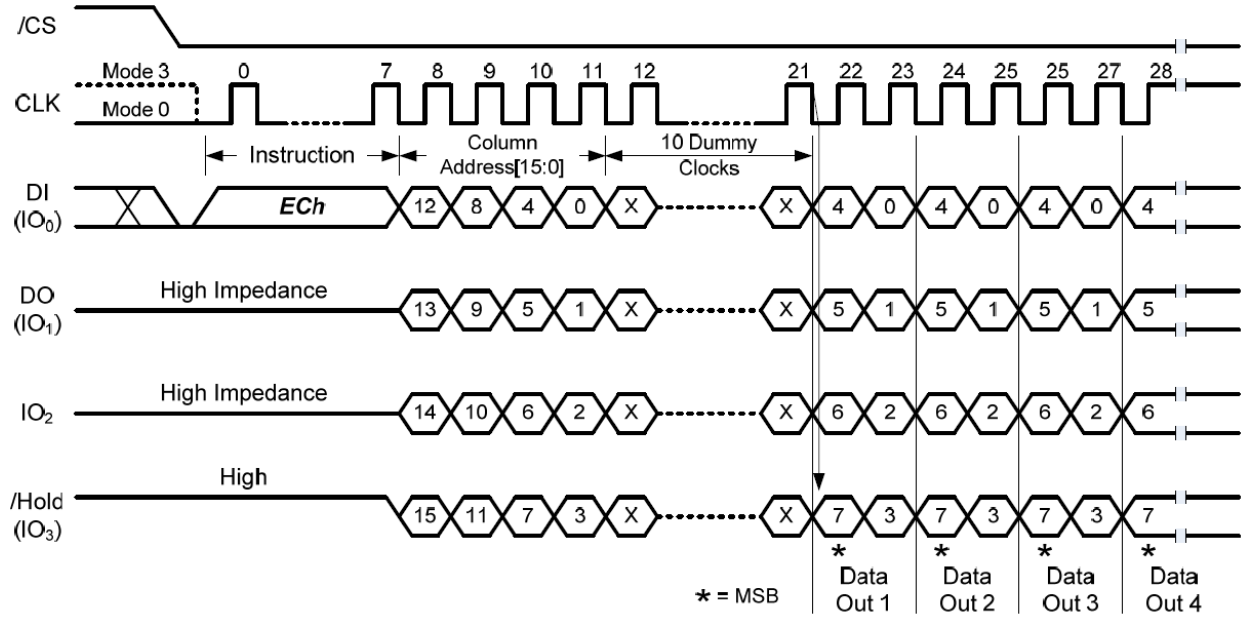


Figure 3-19 Fast Read Quad I/O with 4-Byte Address Instruction

3.5.13. Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the FS35ND04G-S2Y2 is also equipped with one Unique ID Page, one Parameter Page, and 10 OTP Pages.

[Table 5]OTP Area Address

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
02h	OTP Page [0]	Program Only, OTP lockable	2,112-Byte
…	OTP Pages [1:8]	Program Only, OTP lockable	2,112-Byte
0Bh	OTP Page [9]	Program Only, OTP lockable	2,112-Byte

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to "1" first. Then, Read operations can be performed on Unique ID and Parameter Pages. Read and Program operations can be performed on the OTP pages if it's not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A "Page Data Read" command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the command structure (CA[15:0], number of dummy clocks). ECC can also be enabled for the OTP page read operations to ensure the data integrity.

Program and OTP Lock Operations

OTP pages provide the additional space (2K-Byte x10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed one time until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to "1" to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any "Program Data Load" commands. The "Program Execute" command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during "Program Execute", and the ECC information will be stored into the Flash.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the "OTP Access Mode" (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to "1", and issue a "Program Execute" command(Page address is "00h"). After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.

3.5.14. Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

[Table 6] Parameter Page Data Definitions

Byte Number	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	02h, 00h
10~31	Reserved	All 00h
32~43	Device manufacturer	46h,4Fh,52h,45h,53h,45h, 45h,20h,20h,20h,20h,20h
44~63	Device model	46h,53h,33h,35h,4Eh,44h,30h,34h,47h,2Dh, 53h,32h,59h,32h,20h,20h,20h,20h,20h,20h
64	JEDEC manufacturer ID	CDh
65~66	Date code	00h, 00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	40h, 00h
86~91	Reserved	All 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 10h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	50h, 00h
105~106	Block endurance	05h, 04h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	01h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (us)	20h, 03h(800)
135~136	Maximum block erase time (us)	10h, 27h(10000)
137~138	Maximum page read time (us)	C2h, 01h(450)
139~163	Reserved	All 00h
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	Set at test
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768+	Reserved	

3.6. Erase Operation

3.6.1. 128KB Block Erase (D8h)

The 128KB Block Erase instruction sets all memory within a specified block (64-Pages, 128K-Bytes) to the erased state of all is (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed by the 24-bit page address.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP2, BP1, and BP0) bits.

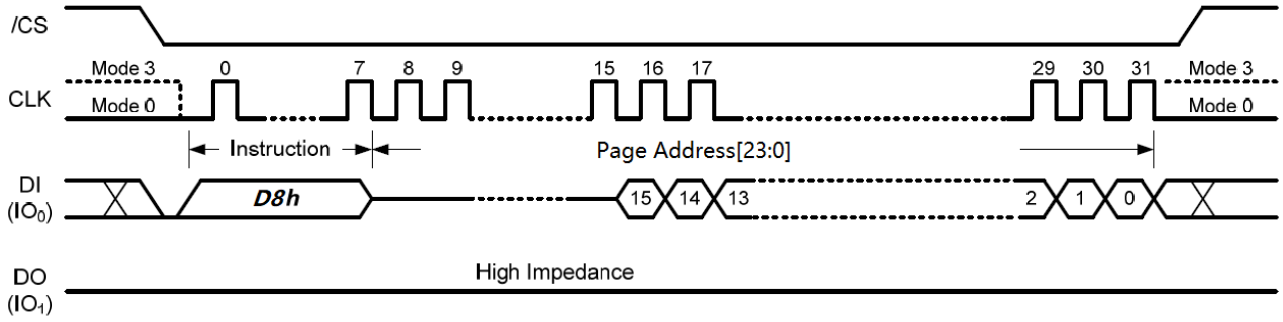


Figure 3-20 128KB Block Erase Instruction

3.7. Feature Operation

3.7.1. Bad Block Management (A1h)

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of "Bad Blocks" found in the factory testing. Up to 2% of the memory blocks can be marked as "Bad Blocks" upon shipment, which is a maximum of 20 blocks for FS35ND04G-S2Y2. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A "Bad Block Marker" is a non-FFh data byte stored at Byte2048 of Page 0 for each bad block.

FS35ND04G-S2Y2 offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The "Bad Block Management" command is initiated by shifting the instruction code "A1h" into the DI pin and followed by the 16-bit "Logical Block Address" and 16-bit "Physical Block Address". A Write Enable instruction must be executed before the device will accept the Bad Block Management Instructions (Status Register bit WEL= 1). The logical block address is the address for the "bad" block that will be replaced by the "good" block indicated by the physical block address.

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 20 links can be established in the non-volatile LUT. If all 20 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a "Read BBM Look Up Table" command can be issued to confirm if spare links are still available in the LUT.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

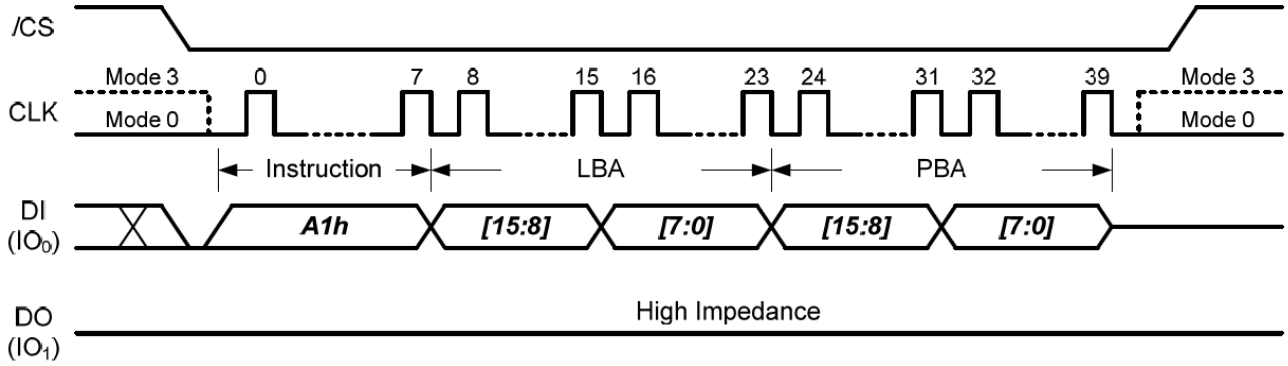


Figure 3-21 Bad Block Management Instruction

3.7.2. Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 20 Logical-Physical memory block links (from LBA0/PBA0 to LBA19/PBA19). The "Read BBM Look Up Table" command can be used to check the existing address links stored inside the LUT.

The "Read BBM Look Up Table" command is initiated by shifting the instruction code "A5h" into the DI pin and followed by 8-bit dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bit "Logical Block Address" and the 16-bit "Physical Block Address" as illustrated in Figure 3-22. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all "00h" data.

[Table 7] BBM Link

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled and it is a valid link.
1	1	This link was enabled, but it is not valid any more.
0	1	Not applicable.

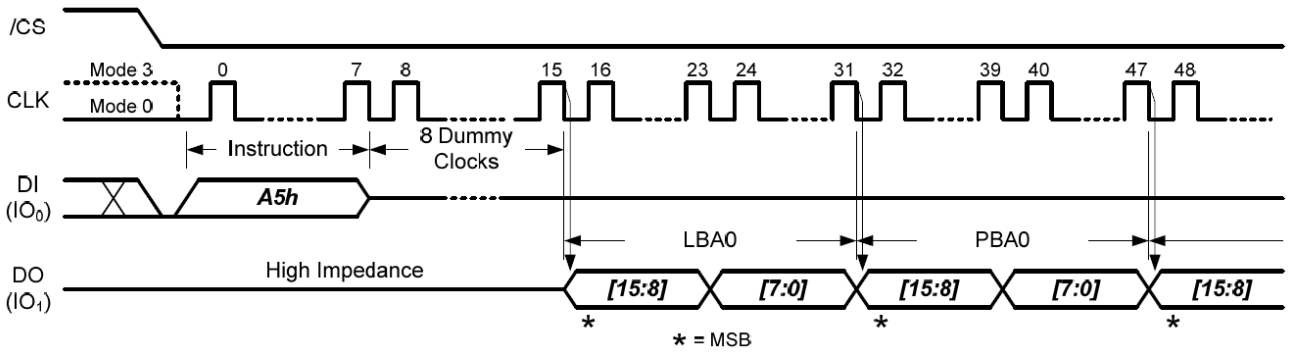


Figure 3-22 Read BBM Look Up Table Instruction

3.7.3. GET FEATURES (0Fh/05h) and SET FEATURES (1Fh/01h)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block lock can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown the following table). The status register is mostly read, except WEL, which is writable bit with the WREN (06h) command.
When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued.
The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E, ECC-E bit in Status Register-2. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.
After power up, factory default for BP[3:0], TB, ECC- E bits are 1, while other bits are 0.

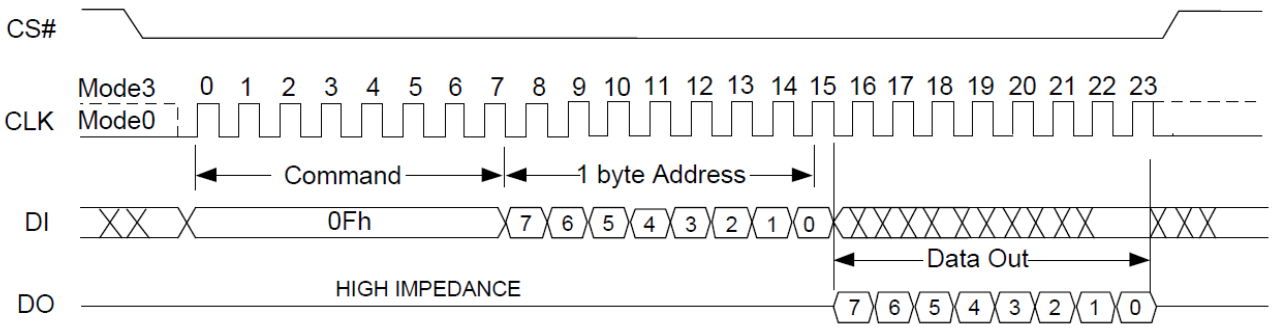


Figure 3-24 GET FEATURES (0Fh) Timing

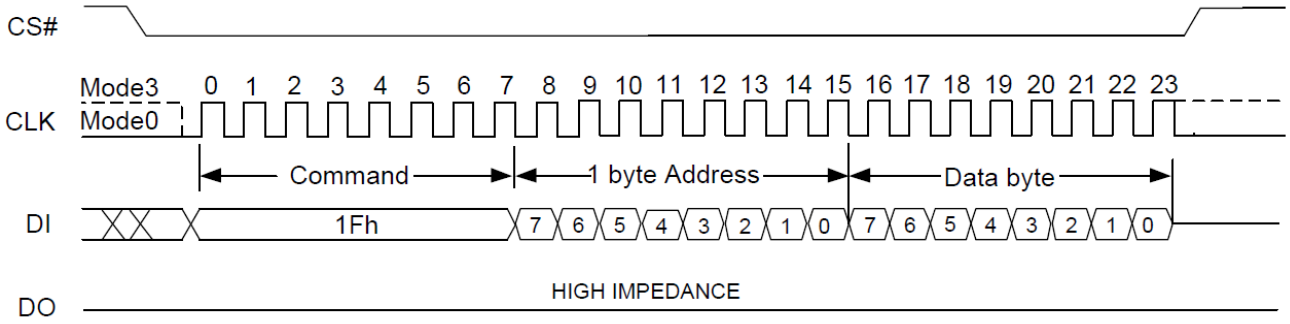


Figure 3-25 SET FEATURES (1Fh) Timing

3.8. PROTECTION, CONFIGURATION AND STATUS REGISTERS

Three Status Registers are provided for FS35ND04G-S2Y2: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results, ECC usage/status. The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes, enable/disable ECC, Protection Register/OTP area lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

3.8.1. Protection Register / Status Register-1 (Volatile Writable)

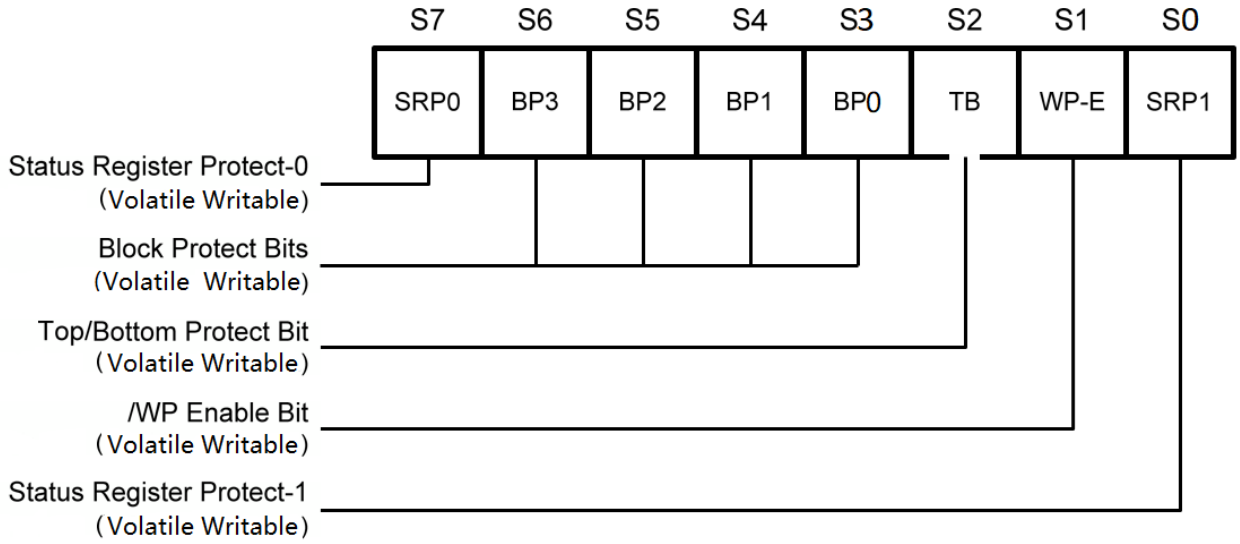


Figure 3-26a Protection Register / Status Register-1 (Address A0h)

Block Protect Bits (BP3, BP2, BP1, BP0, TB) – Volatile Writable

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array.

Write Protection Enable Bit (WP-E) – Volatile Writable

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled and /WP & /HOLD pins become dedicated control input pins.

Status Register Protect Bits (SRP1, SRP0) – Volatile Writable

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down.

[Table 8] Software Protection

Software Protection (Driven by Controller, Quad Program/Read is enabled)				
SRP1	**SRP0**	**WP-E**	**/WP / IO2**	**Descriptions**
0	0	0	X	No /WP functionality /WP pin will always function as IO2
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) /WP pin will function as IO2 for Quad operations
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) /WP pin will function as IO2 for Quad operations
1	0	0	X	Power Lock Down(1) SR-1 /WP pin will always function as IO2

[Table 9] Hardware Protection

Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down(1) SR-1
X	X	1	GND	All "Write/Program/Erase" commands are blocked Entire device (SRs, Array, OTP area) is read-only

Notes:
1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

3.8.2. Configuration Register / Status Register-2 (Volatile Writable)

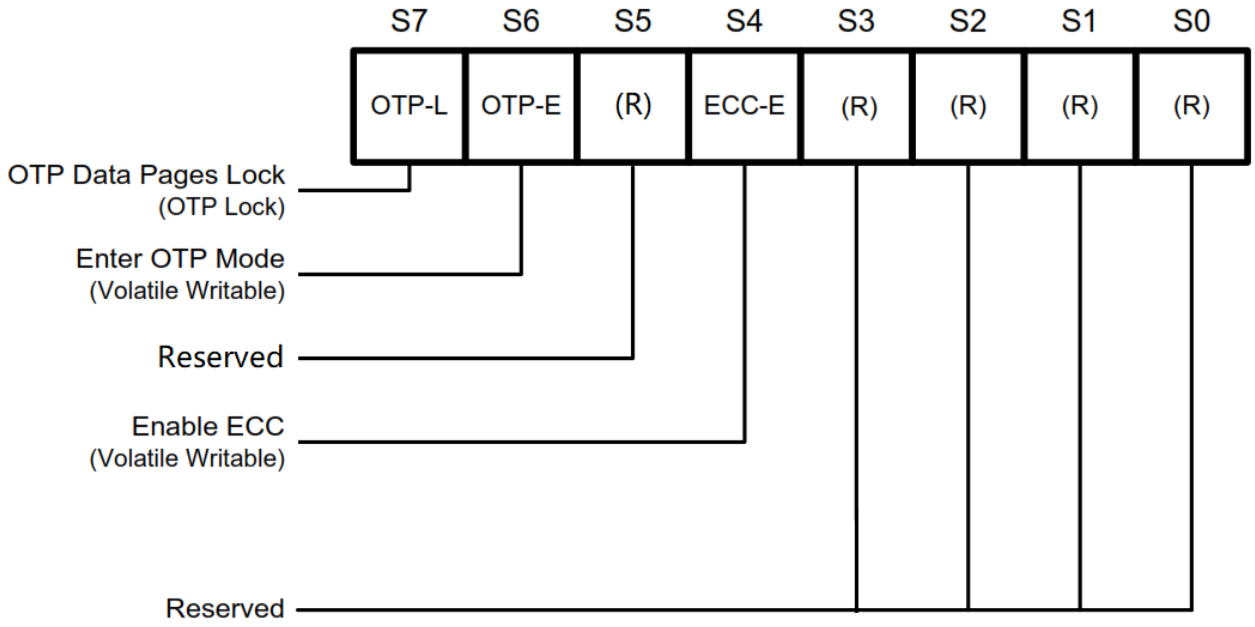


Figure 3-26b Configuration Register / Status Register-2 (Address B0h)

One Time Program Lock Bit (OTP-L) – OTP lockable

In addition to the main memory array, FS35ND04G-S2Y2 also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. The OTP area can only be programmed one time before it is locked. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

Enter OTP Access Mode Bit (OTP-E) – Volatile Writable

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

ECC Enable Bit (ECC-E) – Volatile Writable

FS35ND04G-S2Y2 has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

3.8.3. Status Register-3 (Status Only)

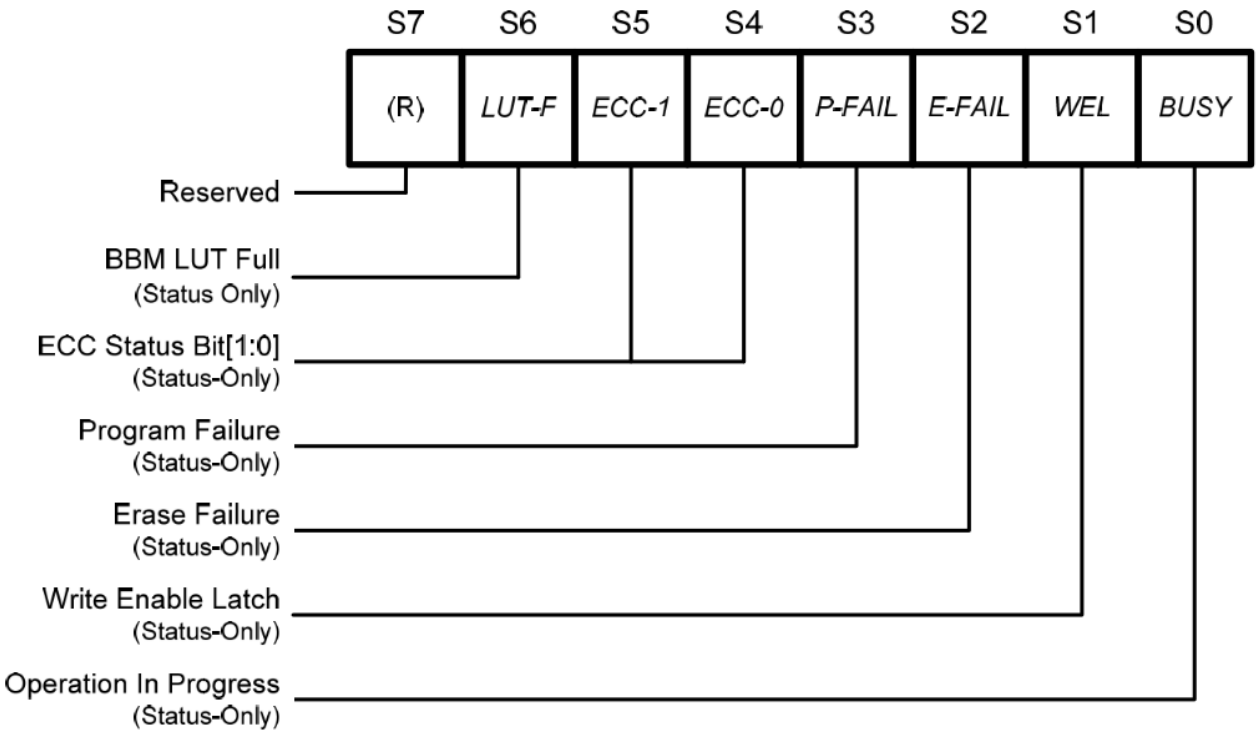


Figure 3-26c Status Register-3 (Address C0h)

Look-Up Table Full (LUT-F) – Status Only

To facilitate the NAND flash memory bad block management, the FS35ND04G-S2Y2 is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 20 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 20 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 20 links are used, LUT-F will become 1, and no more memory block links may be established.

Cumulative ECC Status (ECC-1, ECC-0) – Status Only

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command.

[Table 10] ECC Status

ECC Status		Descriptions
ECC-1	**ECC-0**	
0	**0**	Entire data output is **successful**, with 0~3bits/512bytes ECC corrections in a single page.
0	**1**	Entire data output is **successful**, with 4bits/512bytes ECC corrections in a single page.
1	**0**	Entire data output contains **more than 4 bits errors /512bytes only in a single page which cannot be repaired by ECC**.
1	**1**	Reserved

Program/Erase Failure (P-FAIL, E-FAIL) – Status Only

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory array or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device RESET instruction.

Write Enable Latch (WEL) – Status Only

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read, Program Execute and Bad Block Management for OTP pages.

Erase/Program In Progress (BUSY) – Status Only

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, Bad Block Management, Program Execute, Block Erase, Program Execute for OTP area, OTP Locking. During this time the device will ignore further instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

Reserved Bits – Non Functional

There are a few reserved Status Register bits that may be read out as a "0" or "1". It is recommended to ignore the values of those bits. During a "Write Status Register" instruction, the Reserved Bits can be written as "0", but there will not be any effects.

[Table 11] MEMORY PROTECTION

STATUS REGISTER(1)					FS35ND04G-S2Y2 (4G-bit / 512M-BYTE) MEMORY PROTECTION(2)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[15:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	4088 thru 4095	3FE00h - 3FFFFh	1MB	Upper 1/512
0	0	0	1	0	4080 thru 4095	3FC00h - 3FFFFh	2MB	Upper 1/256
0	0	0	1	1	4064 thru 4095	3F800h - 3FFFFh	4MB	Upper 1/128
0	0	1	0	0	4032 thru 4095	3F000h - 3FFFFh	8MB	Upper 1/64
0	0	1	0	1	3968 thru 4095	3E000h - 3FFFFh	16MB	Upper 1/32
0	0	1	1	0	3840 thru 4095	3C000h - 3FFFFh	32MB	Upper 1/16
0	0	1	1	1	3584 thru 4095	38000h - 3FFFFh	64MB	Upper 1/8
0	1	0	0	0	3072 thru 4095	30000h - 3FFFFh	128MB	Upper 1/4
0	1	0	0	1	2048 thru 4095	20000h –3FFFFh	256MB	Upper 1/2
1	0	0	0	1	0 thru 7	00000h - 001FFh	1MB	Lower 1/512
1	0	0	1	0	0 thru 15	00000h - 003FFh	2MB	Lower 1/256
1	0	0	1	1	0 thru 31	00000h - 007FFh	4MB	Lower 1/128
1	0	1	0	0	0 thru 63	00000h – 00FFFh	8MB	Lower 1/64
1	0	1	0	1	0 thru 127	00000h - 01FFFh	16MB	Lower 1/32
1	0	1	1	0	0 thru 255	00000h - 03FFFh	32MB	Lower 1/16
1	0	1	1	1	0 thru 511	00000h - 07FFFh	64MB	Lower 1/8
1	1	0	0	0	0 thru 1023	00000h – 0FFFFh	128MB	Lower 1/4
1	1	0	0	1	0 thru 2047	00000h – 1FFFFh	256MB	Lower 1/2
X	1	0	1	X	0 thru 4095	00000h - 3FFFFh	512MB	ALL
X	1	1	X	X	0 thru 4095	00000h - 3FFFFh	512MB	ALL

Notes:
1. X = don't care
2. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

4. Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

[Table 12] Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB)	4016
Total available blocks per die	4096
First spare area location	Byte 2048
Bad-block mark	Non FFh

5. ECC Protection

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the "active" state.
To enable/disable ECC, perform the following command sequence:

Issue the SET FEATURES command (1FH).
Set the feature bit ECC_EN as you want:
1. To enable ECC, Set ECC_EN to 1.
2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

Spare area definitions provided in the ECC Protection table below.
ECC can protect according main and spare areas. WRITEs to the ECC area are ignored.

Power on Read with internal ECC:
The device will automatically read first page of first block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correctly by internal ECC.

[Table13] ECC Protection and Spare Area

Min Byte Address	Max Byte Address	Number Of Bytes	Description
000H	1FFH	512	Sector 0
200H	3FFH	512	Sector 1
400H	5FFH	512	Sector 2
600H	7FFH	512	Sector 3
800H	80FH	16	Spare0
810H	81FH	16	Spare1
820H	82FH	16	Spare2
830H	83FH	16	Spare3

Notes：Byte2048 of page 0 for each block is "Bad Block Maker"

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

[Table 14] Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground <20nS Transient	–0.6 to +4.6	V
Transient Voltage on any Pin	VIOT	Relative to Ground	–2.0V to VCC+2.0V	V
Short Circuit Output Current, IOs			5	mA
Storage Temperature	TSTG		–65 to +150	°C
Operating Temperature	TA		-40 to +85°C	°C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. Pin Capacitance

[Table 15] Pin Capacitance

Applicable over recommended operating range from: T_A = +25°C, f = 1 MHz.

Symbol	Test Condition	Max	Units	Conditions
CIN(1)	Input Capacitance	6	pF	VIN = 0V
COUT(1)	Output Capacitance	8	pF	VOUT = 0V

Note:
1) characterized and is not 100% tested.

6.3. Power-up and Power-Down Timing

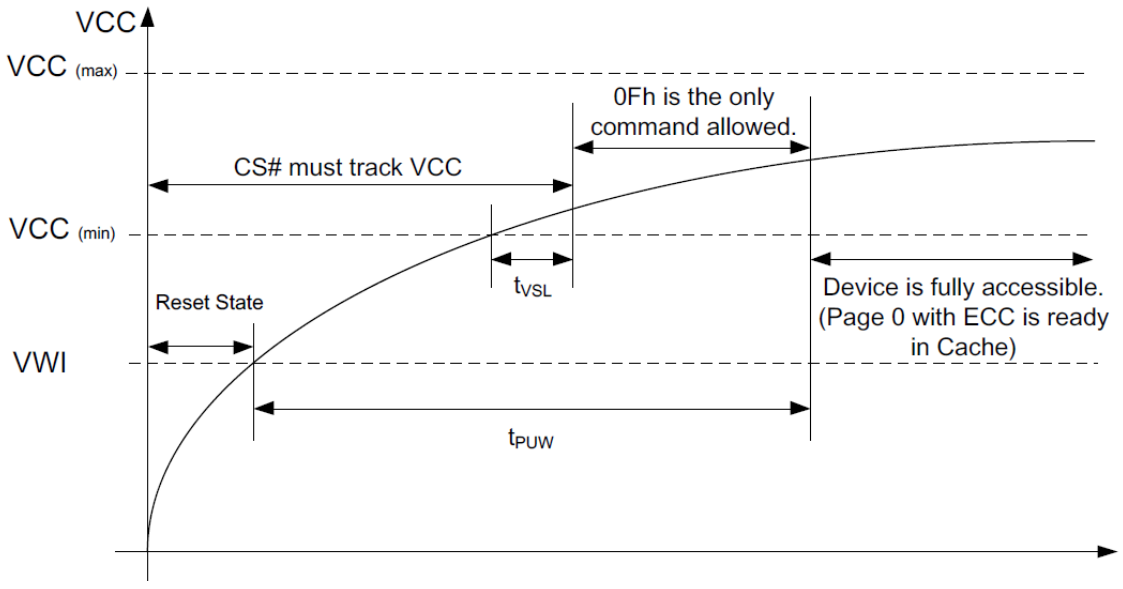


Figure 6-1 Power-On Timing

[Table 16] Power-On Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to CS# Low	tVSL	1		ms
Time Delay Before Write Instruction	tPUW	5		ms
Write Inhibit Voltage	VWI	1.0	2.0	V

6.4. DC Electrical Characteristics

[Table 17] DC Characteristics

Applicable over recommended operating range from: TA = -40°C to +85°C, VCC= 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
VCC	Supply Voltage		2.7		3.6	V
ILI	Input Leakage Current				±2	µA
ILO	Output Leakage Current				±2	µA
ICC1(1)	Standby Current	VCC=3.6V, CS# = VCC, VIN = VSS or VCC		50	200	µA
ICC2	Operating Current	CLK=0.1VCC/0.9VCC FC=108MHz			40	mA
VIL(2)	Input Low Voltage		-0.3		0.3VCC	V
VIH(2)	Input High Voltage		0.7VCC		VCC+0.3	V
VOL	Output Low Voltage				0.4	V
VOH	Output High Voltage		2.4			V

Notes:
1) The device will enter standby mode after pulling down CS# pin for 200ms.
2) VILmin and VIHmax are reference only and are not tested.

6.5. AC Measurement Conditions

[Table 18] AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 VCC to 0.8 VCC		V
IN	Input Timing Reference Voltages	0.3 VCC to 0.7 VCC		V
OUT	Output Timing Reference Voltages	0.5VCC		V

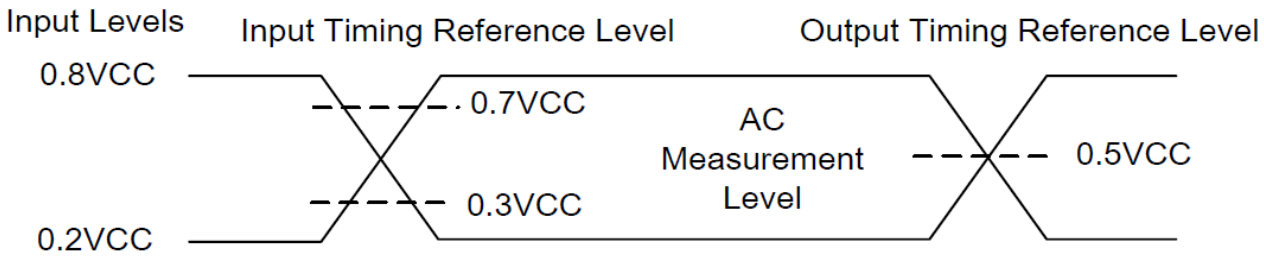


Figure 6-2 AC Measurement I/O Waveform

6.6. AC Electrical Characteristics

[Table 19] AC Characteristics
Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
FC	Serial Clock Frequency for: all command			108	MHz
tCH1(1)	Serial Clock High Time	4.3			ns
tCL1(1)	Serial Clock Low Time	4.3			ns
tCLCH(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
tCHCL(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL/tCS	CS# High Time	20			ns
tSHQZ(2)	Output Disable Time			10	ns
tCLQX	Output Hold Time	0			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	3			ns
tHLCH	HOLD# Low Setup Time (relative to CLK)	5			ns
tHHCH	HOLD# High Setup Time (relative to CLK)	5			ns
tCHHH	HOLD# Low Hold Time (relative to CLK)	5			ns
tCHHL	HOLD# High Hold Time (relative to CLK)	5			ns
tHLQZ(2)	HOLD# Low to High-Z Output			15	ns
tHHQX(2)	HOLD# High to Low-Z Output			15	ns
tCLQV	Output Valid from CLK			8	ns
tWHSL	WP# Setup Time before CS# Low	20			ns
tSHWL	WP# Hold Time after CS# High	100			ns

Notes:
1. TCH1+TCL1>= 1 / FC ;
2. characterized and not 100% tested.

[Table 20] Performance Timing

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
tRST	CS# High to Next Command After Reset(FFh)			500	µs
tRD	Page Read From Array		120	450	µs
tPROG	Page Program		430	800	µs
tERS	Block Erase		2	10	ms
NOP	Number of partial page program			1	time

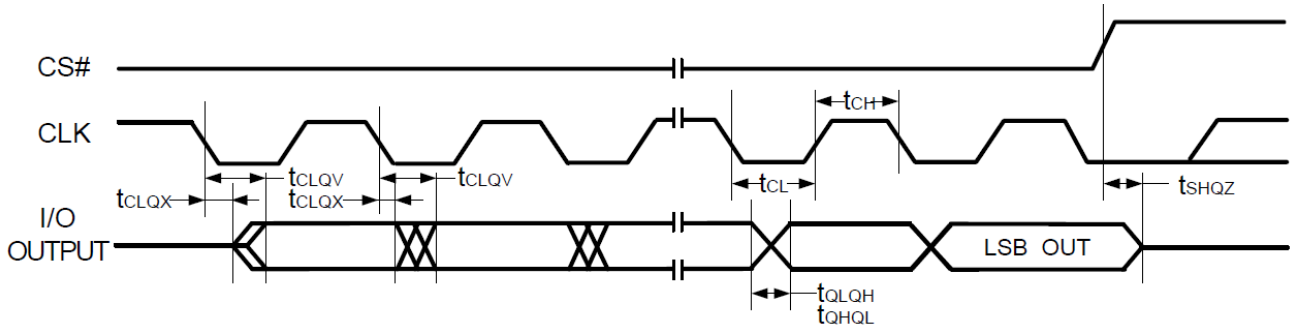


Figure 6-3 Serial Output Timing

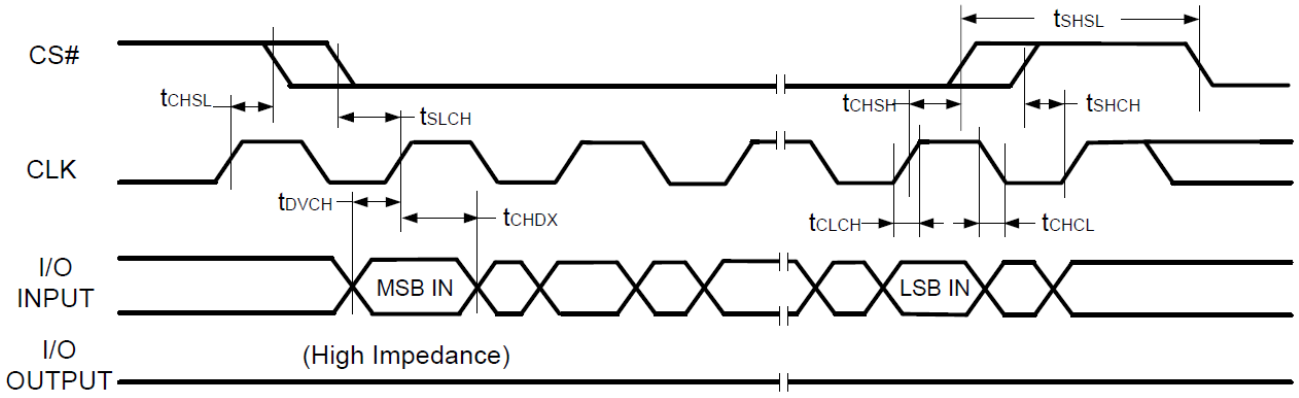


Figure 6-4 Serial Input Timing

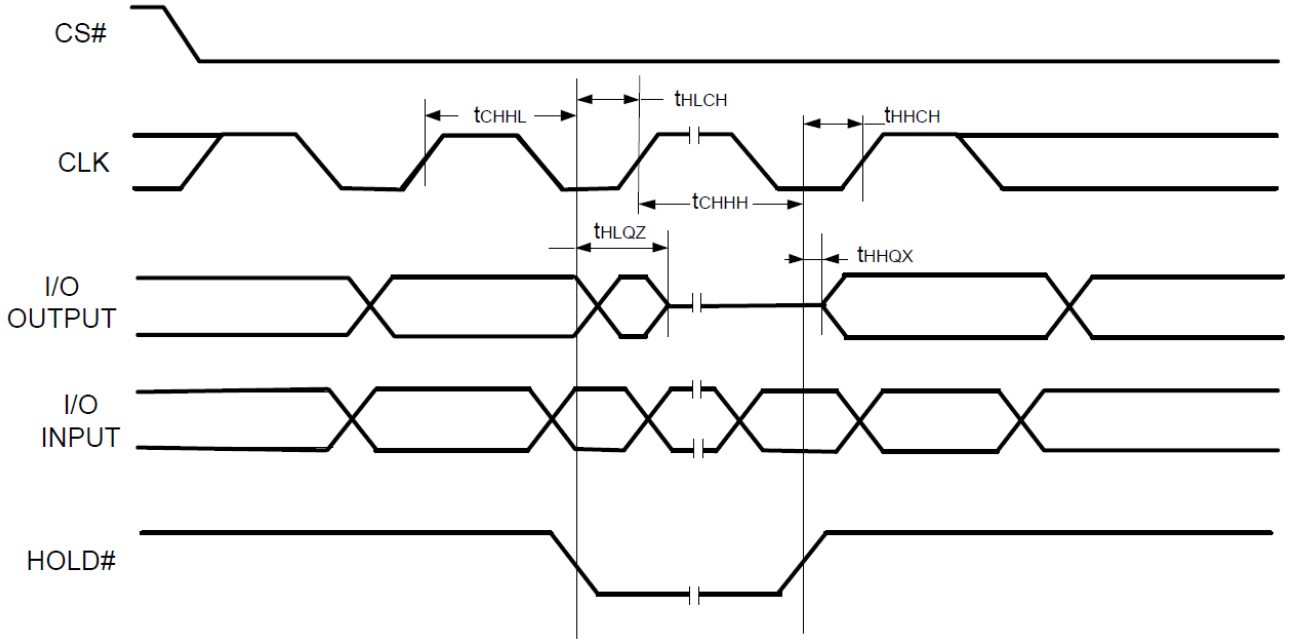


Figure 6-5 Hold Timing

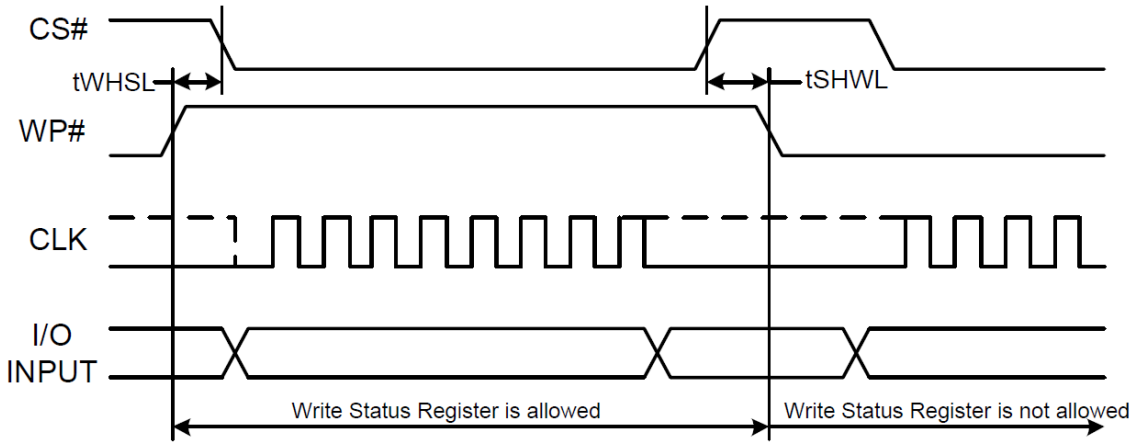
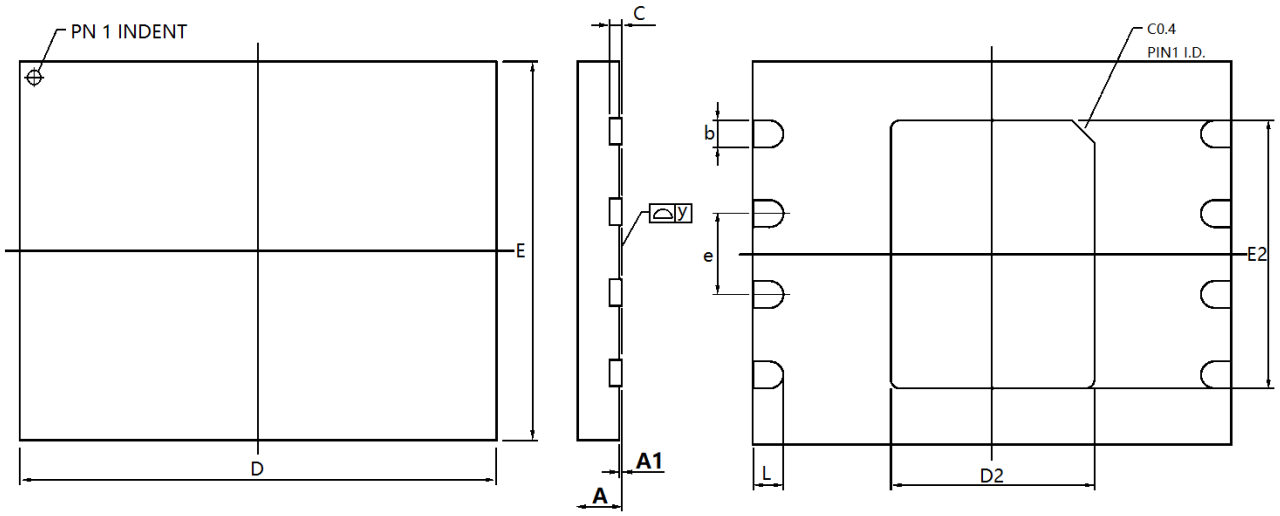


Figure 6-6 WP Timing

7. Packaging Information

WSON8 (8x6mm)



Symbol	MIN	MAX
e	1.270 BSC	
D	7.900	8.100
E	5.900	6.100
L	0.450	0.550
A	0.700	0.800
A1	0.000	0.050
C	0.180	0.250
b	0.350	0.450
D2	3.300	3.500
E2	4.200	4.400

Note: Dimensions are in Millimeters.