General Description

FS6823DG is a current mode PWM controller with integrated high voltage power MOSFET. It could be used in sub 10W(Note 1) applications.

In PWM mode, FS6823DG operates in fixed frequency which is precisely set internally.FS6823DG could operate in Extended Burst Mode at no load or light load, in which mode switching loss is minimized and the frequency is adjusted internally. To ensure that power supplies work quietly, the frequency is set beyond 20 KHz in Extended Burst Mode. Small current is needed when FS6823DG starts up and works, thus a large value resistor could be used in the startup circuit to minimize the standby power. Slope compensation circuit is integrated in FS6823DG, which improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle. Leading-edge blanking on current sense (CS) input eliminates the signal glitch due to snubber circuit diode reverse recovery current. Frequency jittering technique is integrated in FS6823DG, which helps to achieve excellent EMI performance.

FS6823DG offers complete protection functions including cycle-by-cycle current limiting protection(OCP), over load protection(OLP),VDD over voltage protection(OVP), VDD over voltage clamp and under voltage lockout(UVLO).FS6823DG is available in Pb-free SOP8 package.

Applications

- Battery Charger
- Power Adaptor for PDA and Digital Camera
- Set-Top Box Power Supplies
- Open-frame SMPS

Features

- Optimized for Sub 10W Applications(Note 1)
- 650V Power MOSFET is Integrated
- 4mS Soft Start
- Frequency Jittering for Improved EMI
- Extended Burst Mode for Improved Efficiency and Low Standby Power
- Audio Noise Free Operation
- Fixed 50KHz Switching Frequency in PWM Mode
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- Over Load Protection(OLP) and Cycle-by-Cycle Current Limiting Protection(OCP)
- VDD Over Voltage Protection(OVP),Under Voltage Lockout Protection(UVLO) and Over Voltage Clamp
- Pb-free SOP8 Package

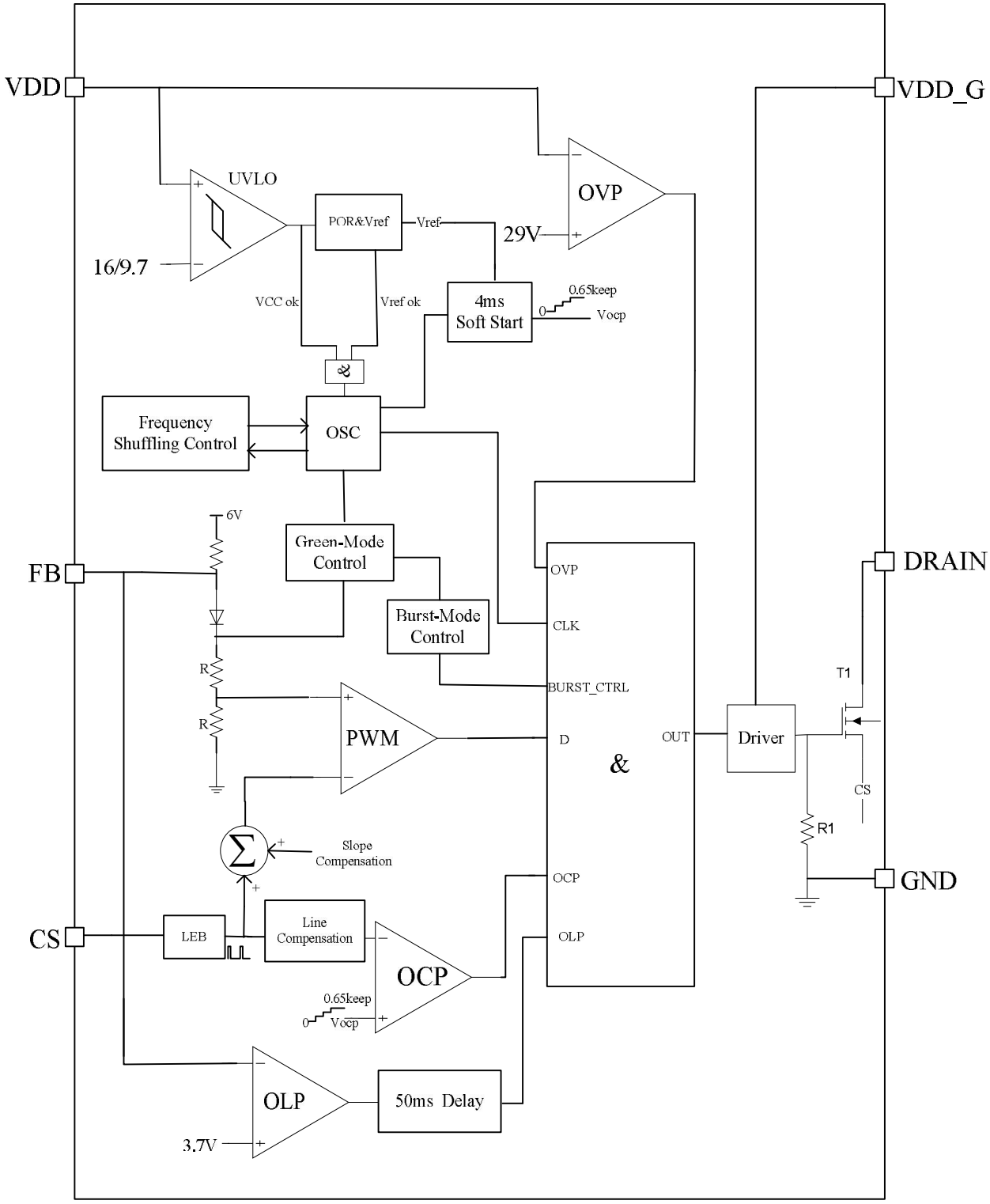
Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{DRAIN_MAX}	Drain Input Voltage	650	V
V_{DD}	VDD Input Voltage	32	V
V_{DD_G}	VDD-G Input Voltage	32	V
I_{DD}	VDD Input DC Current	10	mA
V_{FB}	FB Input Voltage	-0.3~7	V
V_{CS}	CS Input Voltage	-0.3~7	V
$T_{STORAGE}$	Min/Max Storage Temperature	-55 to 160	℃
T_{LEAD}	Lead Temperature（Soldering,10Sec）	260	℃

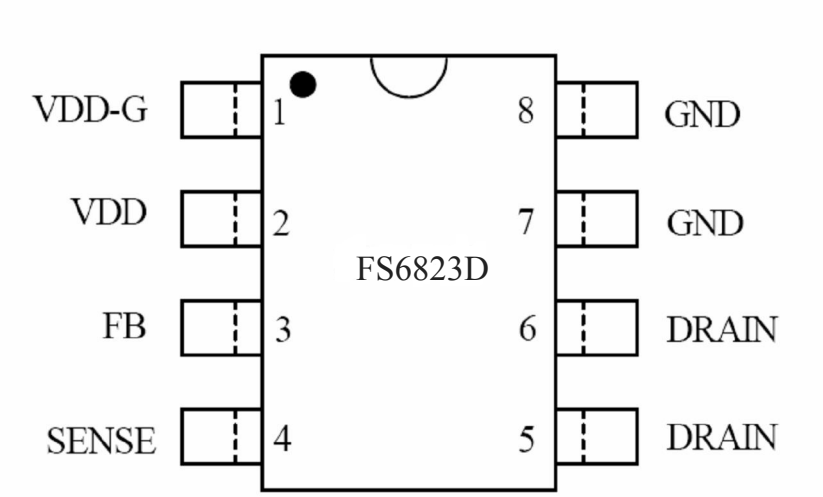
Recommended Operating Conditions

Symbol	Description	Value	Units
V_{DD}	VDD Input Voltage	12~25	V
V_{DRAIN_MAX}	Drain Input Voltage	<500	V

Block Diagram



Pin Function Description



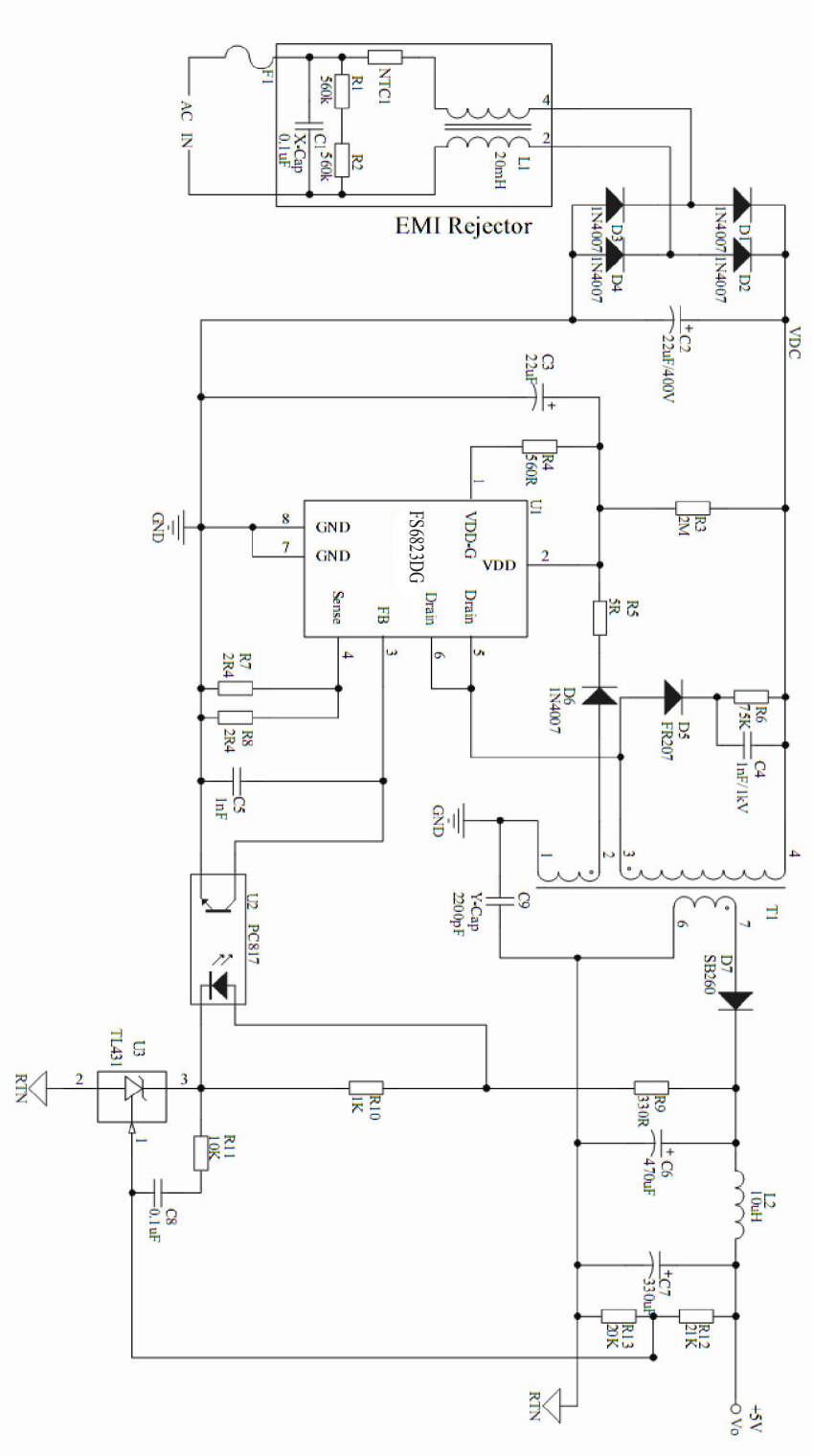
Pin No.	Pin Name	Function Description
1	VDD-G	Power Supply for Internal Gate Driver
2	VDD	Power Supply for IC
3	FB	Feedback Input Pin
4	SENSE	Current Sense Input Pin
5、6	DRAIN	Connected to the Drain of Internal Power MOSFET
7，8	GND	Ground

Electrical Characteristics

T_A=25℃,V_{DD}=16V, unless otherwise noted.

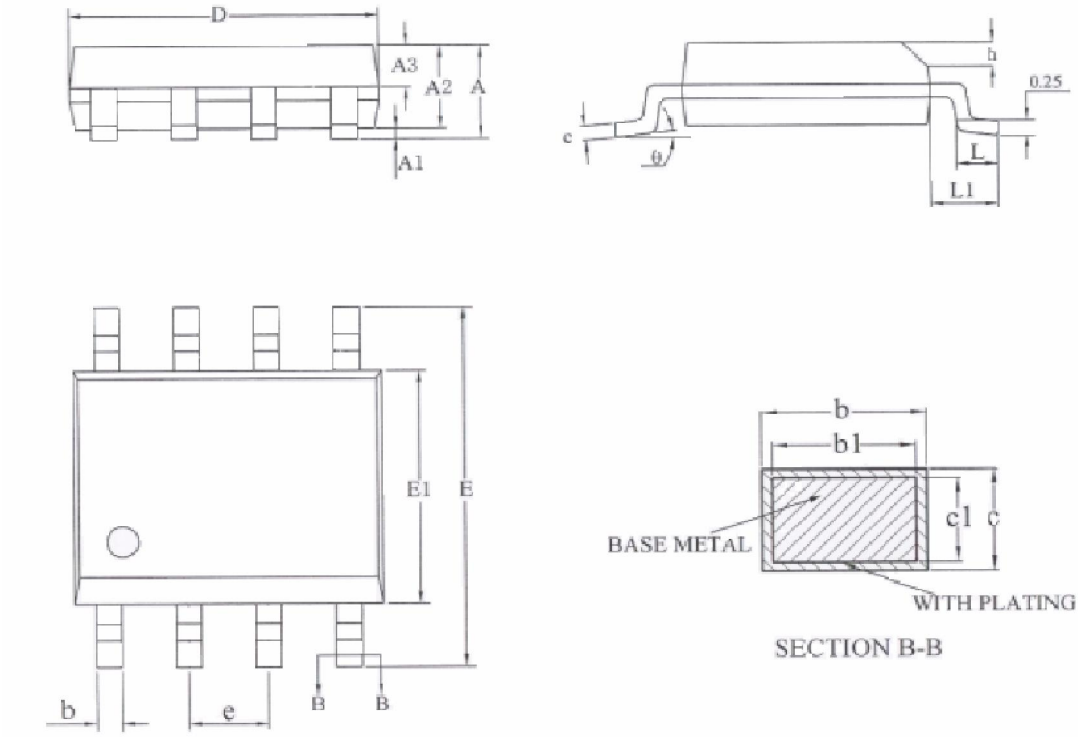
Symbol	Description	Test Conditions	Value			Units
			MIN	TYP	MAX	
I_{DD_ST}	VDD Startup Current	VDD=14.5V		5	20	uA
I_{OP}	Operating Current	V_{DD}=16V ,V_{FB}=3V,V_{CS}=0V		1.6		mA
V_{DD_ST}	VDD Turn-On Threshold Level	VDD Going Up	15.0	16.0	17.0	V
V_{UVLO}	VDD Under Voltage Lockout	VDD Going Down	8.7	9.7	10.7	V
V_{OVP}	VDD Over Voltage Protection		26.8	28.3	29.8	V
V_{DD_CLAMP}	VDD Voltage Clamp	I_{DD}=10mA		30.5		V
V_{FB_OPEN}	FB Open Loop Voltage	V_{DD}=16V	5.4	5.7	6.0	V
I_{FB_SHORT}	FB Short Circuit Current	V_{DD}=16V，Short FB to GND and Measure the Current		1.45		mA
V_{TH_0D}	Zero Duty Cycle FB Threshold Voltage	V_{DD}=16V,V_{CS}=0V,FB Going Down until the Power MOSFET Turn Off		1.28		V
T_{LEB}	Leading Edge Blanking Time			270		nS
Z_{SENSE_IN}	SENSE Input Impedance			40		KΩ
V_{TH_OC}	Internal Current Limiting Threshold Voltage	V_{DD}=16V,V_{FB}=3V,Voltage on CS Pin Going Up until the Power MOSFET Turn Off	0.72	0.77	0.82	V
T_{D_OC}	Over Current Detection and Control Delay	From Over Current Occurs till the Gate Driver Starts to Turn Off		120		nS
F_{OSC}	Oscillation Frequency	V_{DD}=16V ,V_{FB}=3V,V_{CS}=0V	45	50	55	KHz
D_{MAX}	Maximum Duty Cycle	V_{DD}=16V ,V_{FB}=3.3V,V_{CS}=0V	70	80	90	%
F_{BURST}	Burst Mode Frequency			22		KHz
ΔF_{OSC}	Frequency Modulation Range/Base Range		-4		4	%
$R_{DS(ON)}$	Static Drain-Source On-Resistance				15	Ω

Typical Application



Package Information

Units：mm



SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	_	_	1.75	D	4.70	4.90	5.10
A1	0.05	_	0.15	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	_	0.48	h	0.25	_	0.50
b1	0.38	0.41	0.43	L	0.50	_	0.80
c	0.21	_	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	_	8°

Accessories

- **General Description**

FS6823DG is a low power SMPS(Switching Mode Power Supply) switcher optimized for offline flyback converter in sub 10W(Note 1) applications. Integrated with functions as frequency jittering and extended burst mode control, FS6823DG helps to minimize the standby power and improve the EMI performance, which make designs more easily to meet the international power conservation requirements.

- **Start Up**

Startup current of FS6823DG is designed to be very low, so the voltage of the capacitance in VDD could be charged up to the Turn-on level quickly and then IC starts to work. Thus a large value resistor can be used in the startup circuit which will minimize the power loss when startup process is still reliable. For most AC/DC adaptor with universal input range design, a 2MΩ, 1/8W startup resistor could be used together with a VDD capacitance to provide a fast startup and yet low power dissipation design solution.

- **Operating Current**

The operating current of FS6823DG is very low, so the capacitance in VDD allows using smaller value with improved efficiency.

- **Frequency Jittering**

Frequency jittering technique is implemented in FS6823DG. The oscillation frequency is modulated with a random source so that the frequency is always changing in a preset range, which spreads the tone energy spectrum and minimizes the EMI in the conduction band. These make the design of SMPS become easier to meet relative international standards.

- **Extended Burst Mode**

At no load or light load condition, most of the power dissipation in a SMPS is from switching loss on the power MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency results in less power loss and thus conserves the energy.

The switching frequency is adjusted by the loop and controller IC in SMPS using FS6823DG. At no load or light load the frequency reduces to improve the conversion efficiency, otherwise if FB input drops below the burst mode threshold level, then FS6823DG enters burst mode. The gate drive output switches only when FB input is active to output an on state. Otherwise, the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

- **Switching Frequency**

The switching frequency of FS6823DG is internally set as 50 KHz in PWM mode. No external component is needed to program the switching frequency.

- **Current Sensing and Leading Edge Blanking**

Using current mode PWM control, cycle-by-cycle current limiting is offered in FS6823DG. The switch current is detected by a sense resistor connected to the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp on the current sense input voltage. This function greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation.

- **Power MOSFET Drive**

For most SMPS, Too weak gate driving strength results in higher conduction and switching loss of power MOSFET while too strong gate driving strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time control. Low idle loss and improved EMI is easier to achieve with this dedicated control scheme. An internal 16V clamp is added for internal MOSFET gate protection at higher than expected VDD input.

- **Protection Functions**

Good power supply system reliability is achieved with its rich protection features including cycle-by-cycle current limiting (OCP), over load protection (OLP), over voltage protection (OVP), VDD over voltage clamp and under voltage lockout on VDD (UVLO).

OCP compensation function is integrated in FS6823DG,with optimized design, OCP threshold voltage could be compensated with different line voltage, thus constant output power limit over the universal input voltage(85Vac~265Vac) is achieved.

At overload condition, when FB input voltage exceeds power limit threshold value for more than T_{D_PL}, control circuit reacts to shut down the internal power MOSFET.FS6823DG restarts when VDD voltage drops below UVLO limit.

VDD is supplied by transformer auxiliary winding output after start up. If the voltage on VDD is higher than V_{OVP}, control circuit reacts to shut down the internal power MOSFET, and then FS6823DG enters another startup sequence. When VDD is higher than 30.5V, an internal zener diode will clamp the VDD voltage at 30.5V to protect devices.

The internal MOSFET is shut down when VDD drops below UVLO limit and then device enters another start-up sequence.

Note 1：Test Condition: Input voltage is 230VAC±15%，T_A is not higher than 50℃。