FORESEE®

nMCP Datasheet

FS704B2R1CH6A2KDE
FS704B2R1CH6A2KAM

Rev. 1.5

2019-12

Document title：
nMCP
NAND(x8) Flash/ (x32) LPDDR2

Revision History:

Rev.	Date	Change	Remark
1.0	2019/04	Basic spec and architecture	
1.1	2019/05	Flash ID Description	
1.2	2019/05	PN Chart	
1.3	2019/07	Operation Temperature	
1.4	2019/07	PN Chart	
1.5	2019/12	Product list	Add FS704B2R1CH6A2KAM

Contents

1. INTRODUCTION

1.1. General Description

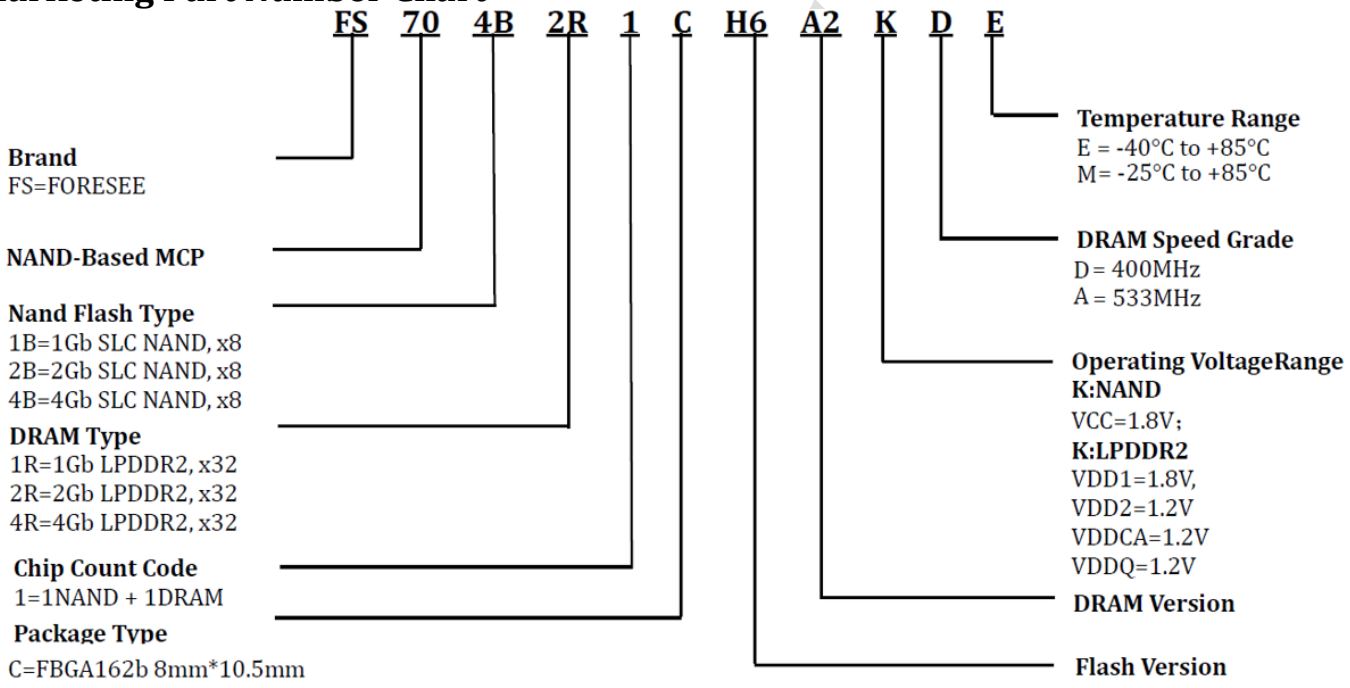
FORESEE MCP products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements.
The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces(no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses.
The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, VSS is tied together on the two devices).
The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction.

1.2. Product List

Product List

Part Number	Density	Frequency (MHz)	Package Type	Package Size(mm)
FS704B2R1CH6A2KDE	2Gbits LPDDR2+4Gbits NAND	400	BGA162	8.0x10.5x1.0
FS704B2R1CH6A2KAM	2Gbits LPDDR2+4Gbits NAND	533	BGA162	8.0x10.5x1.0

Marketing Part Number Chart



1.3. Device Features

[nMCP]

● Operation Temperature
- Commercial: (-25)°C ~ 85°C
- Industrial : (-40)°C ~ 85°C

● Package
- 162-ball FBGA – 8x10.5mm²

[NAND FLASH]

● Voltage Supply
- V_{CC}: 1.8V (1.7V ~ 1.95V)

● Organization
- Memory Cell Array : (512M + 32M) Byte
- Page Size : (2K + 128) Byte
- Data Register : (2K + 128) Byte
- Block Erase : (128K + 8K) Byte

● Automatic Program and Erase
- Page Program : (2K + 128) Byte

● Page Read Operation
- Random Read: 30μs(Max.)
- Serial Access : 45ns(Min.)

● Fast Write Cycle Time
- Page Program time : 300μs(Typ.)
- Block Erase Time : 3.5ms(Typ.)
- Multi-page program(2 pages): 300us(Typ)

● Command/Address/Data Multiplexed I/O Port

●COMMAND SET
- ONFI1.0 Compliant command set
- Read Unique ID

● Reliability
- 100,000 P/E Cycle(with 4bit/512+32Byte ECC)
- 10 Year Data retention (Typ.)

[LPDDR2]

Features

•Organization

- 8 banks x 8M words x 32 bits

•Power supply:

- VDD1=1.7 to 1.95V
- VDD2,VDDCA,VDDQ=1.14 to 1.3V

•Clock frequency:

533/466/400/333/266/200/166Mhz

•2KB page size

- Row address: AX0 to AX13
- Column address: AY0 to AY8 (X 32 bits)

•Eight internal banks for concurrent operation

•Interface: HSUL_12

- Burst lengths (BL): 4, 8, 16

•Burst type (BT):

- Sequential (4, 8, 16)
- Interleave (4, 8)

•Read latency (RL): 3, 4, 5, 6, 7, 8

•Write latency (WL): 1, 2, 3, 4

•Precharge: auto precharge option for each burst access

•Programmable driver strength

•Refresh: auto-refresh, self-refresh

•Refresh cycles: 8132 cycles/32ms

- Average refresh period: 3.9μs

•DLL is not implemented

•Low power consumption

•JEDEC LPDDR2-S4B compliance

•Partial Array Self-Refresh (PASR)

•Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor

•Deep power-down mode

•Double-data-rate architecture; two data transfers per one clock cycle

•The high-speed data transfer is realized by the 4 bits prefetch pipelined architecture

•Differential clock inputs

•Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS

•Data mask (DM) for write data

1.4. Connection Diagram

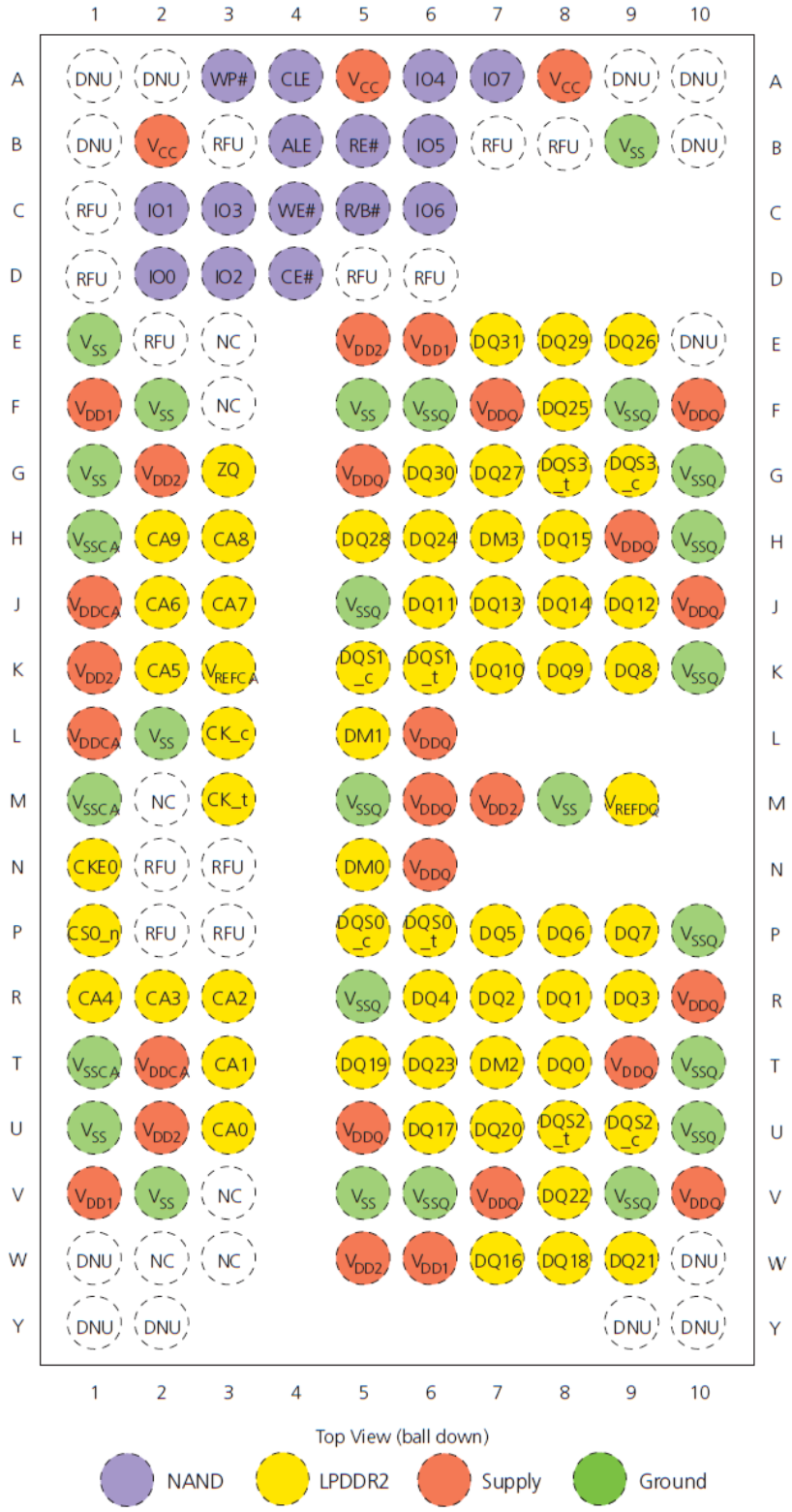


Figure 1-1 162-BGA Contact (Top View)

1.5. Pin Description

Pin Description

Symbol	Description	Type
<NAND(x8)>		
I/O0~ I/O7	Data I/O	Input/Output
CLE	Command Latch Enable	Input
ALE	Addess Latch Enable	Input
CE#(CE0)	Chip Enable	Input
RE#(NRE)	Read Enable	Input
WE#(WE)	Write Enble	Input
WP#(WP)	Write Protect	Input
R/B#(RB0)	Ready/Busy	Output
VCC	Power Supply	Power
VSS	Ground	Ground
<LPDDR2(x32,1CS)>		
CA[9:0]	Command/address inputs	Input
CK_t, CK_c	Clock	Input
CKE0	Clock enable	Input
CS_n	Chip select	Input
DM[3:0]	Input data mask	Input
DQ[31:0]	Data input/output	I/O
DQS[3:0]_t, DQS[3:0]_c	Data strobe	I/O
VDDQ	DQ power supply	Supply
VSSQ	DQ ground	Supply
VDD1	Core power: Supply 1	Supply
VDD2	Core power: Supply 2	Supply
VDDCA	Input Receiver Power Supply.	Supply
VSS	Common ground.	Supply
VREFCA, VREFDQ	Reference voltage: VREFCA is reference for command/address input buffers, VREFDQ is reference for DQ input buffers.	Supply
ZQ	External reference ball for output drive calibration	Reference
DNU	Do not use: Must be grounded or left floating	–
NC	No connect: Not internally connected	–
RFU	Reserved for future use	–

NOTE:
Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

1.6. System Block Diagram

DRAM Block Diagram(x32)：

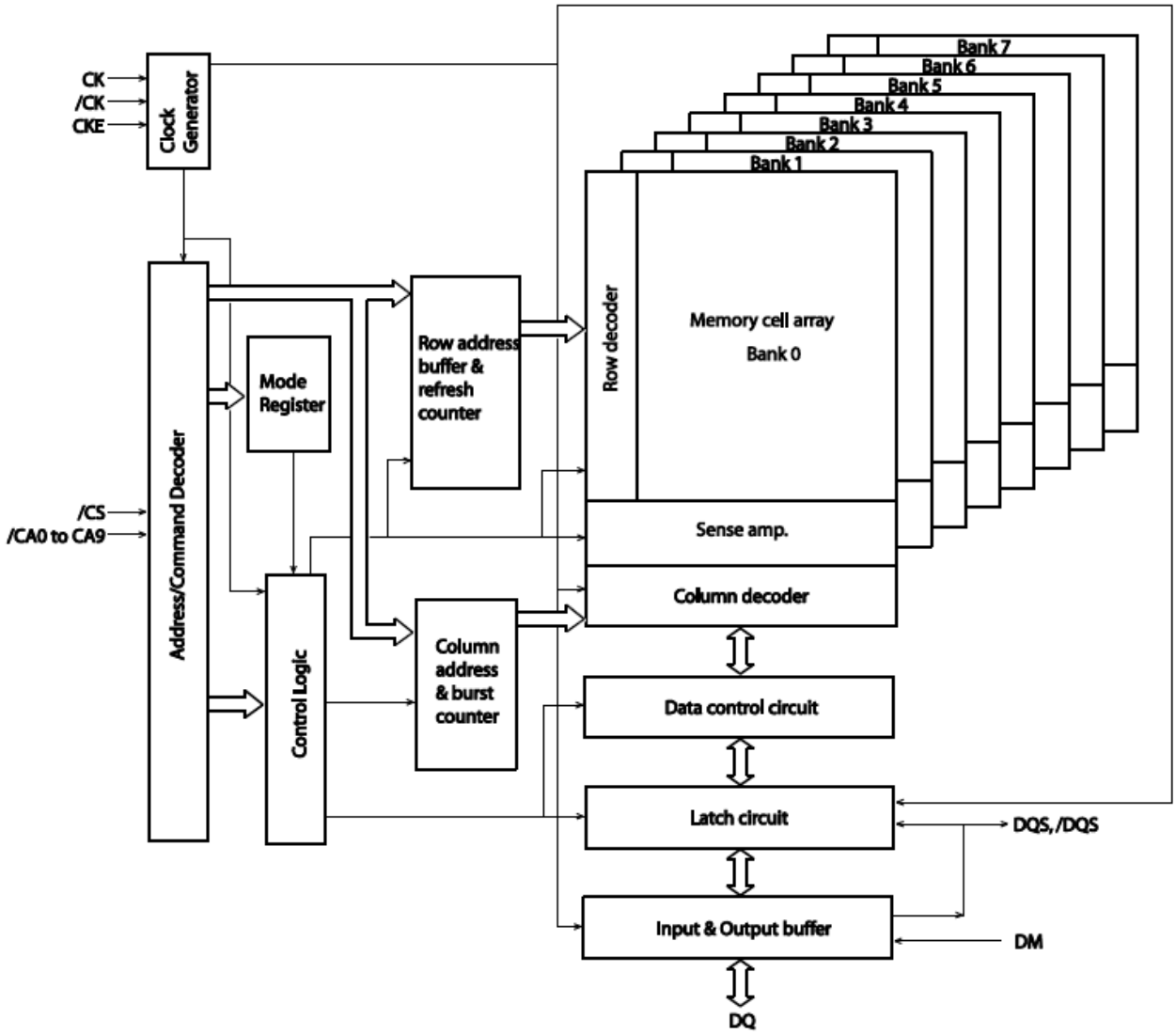


Figure 1-2 DRAM Block Diagram

NAND Block Diagram:

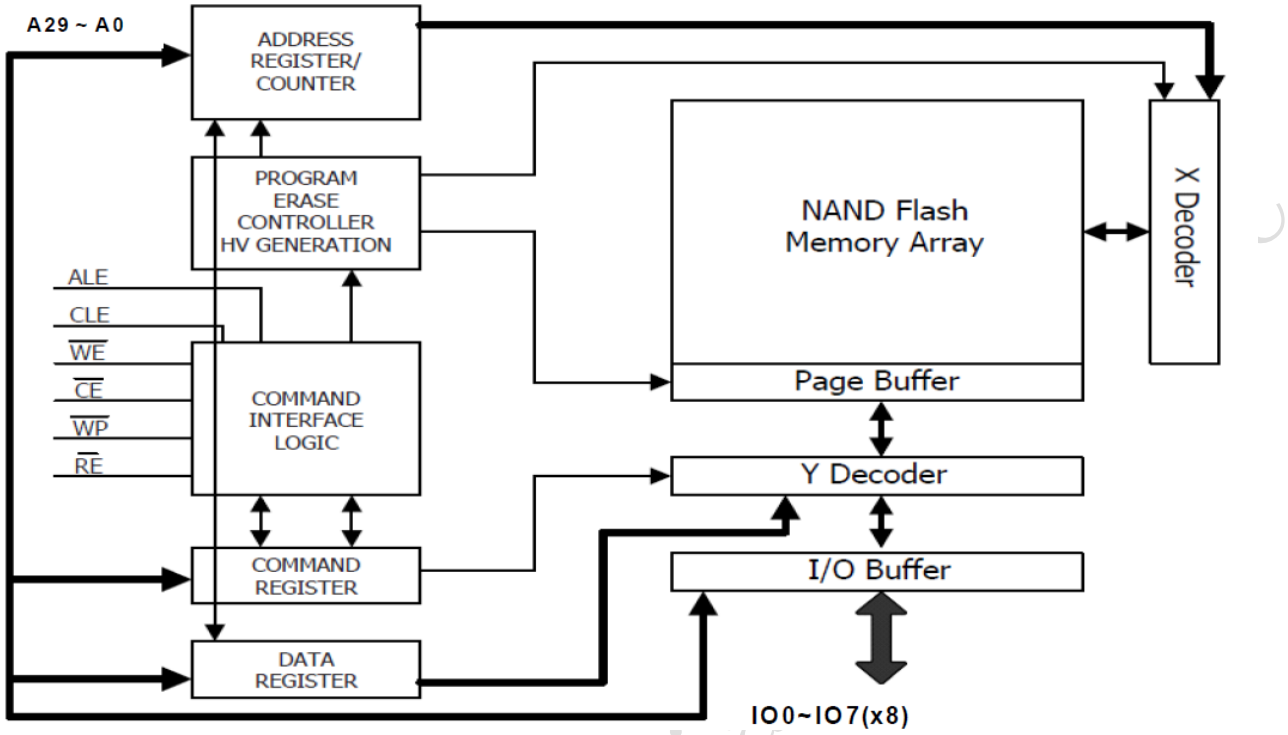
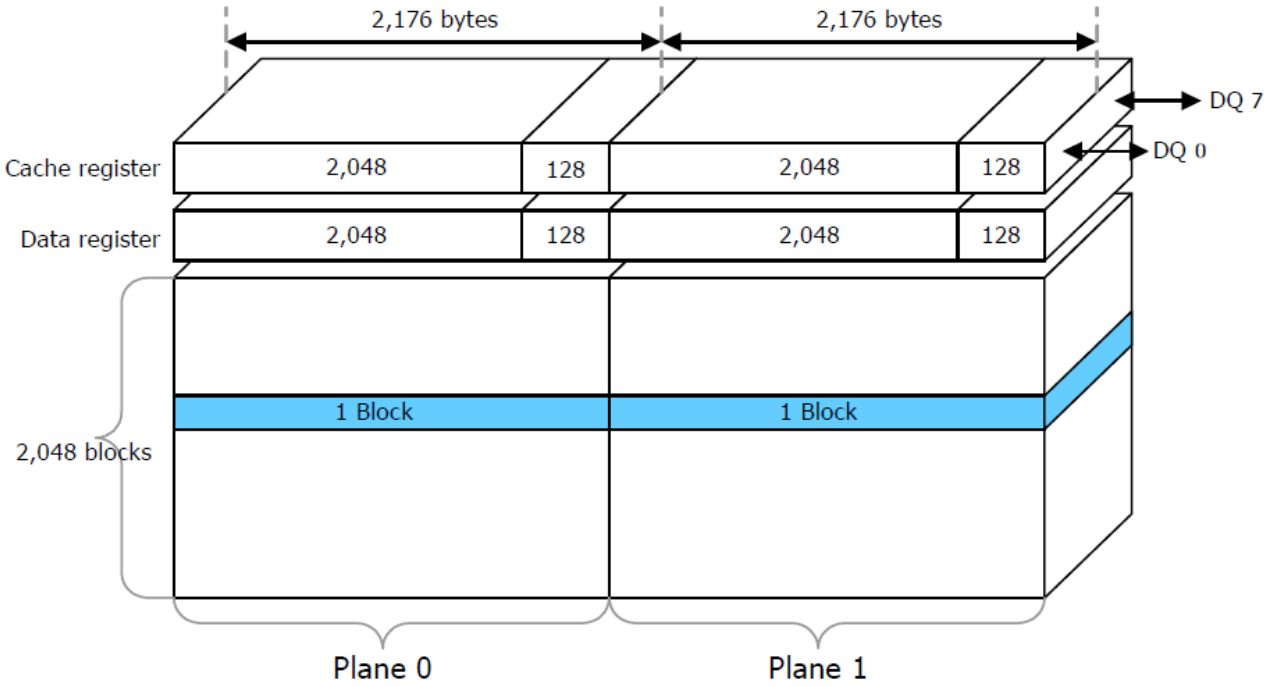


Figure 1-3 NAND Block Diagram

Array Organization:



1 Page = (2K+128) Bytes
1 Block = (2K+128) Bytes x 64 pages = (128K + 8K) Bytes
1 Device = (128+8K) Bytes x 4096 Blocks=(512M+32M)Bytes

Figure 1-4 4G NAND Array Organization

LPDDR2
SDRAM

2. LPDDR2 Description

2.1. LPDDR2 SDRAM Addressing

Key Timing Parameters

Speed Grade	Clock Rate	Access Time
-18	533 MHz	1.875ns
-25	400Mhz	2.500ns

Configuration Addressing – 2Gbits

Architecture	64 Meg x 32
Configuration	8 Meg x 32 x 8 banks
Row addressing	16K A[13:0]
Column addressing	512 A[8:0]

2.2. Pin Function

CK_t, CK_c (input pins)
The CK_t and the CK_c are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK_t rising edge and the CK_c falling edge. When in a read operation, DQSs and DQs are referred to the cross point of the CK_t and the CK_c. When in a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CK_t and the CK_c. The other input signals are referred at CK_t rising edge.

CS_n (input pin)
When CS_n is low, commands and data can be input. When CS_n is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

CA0 to CA9 (input pins)
These pins define the row & column addresses and operating commands (read, write, etc.) depend on their voltage levels. See "Addressing Table" and “Command operation”.

Addressing Table

Page Size	Organization	Row address	Column address
2KB	x 32 bits	R0 to R13	C0*1 to C8

Command operation

Command	DDR CA Pins										CK edge
	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
Active	--	--	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
	R0	R1	R2	R3	R4	R5	R6	R7	R13	--	↓
Write/Read	--	--	--	--	--	C1	C2	BA0	BA1	BA2	↑
	AP	C3	C4	C5	C6	C7	C8	--	--	--	↓

Remarks: Rx = row address. Cx = column address
Notes:
1.C0 is not present on the command & address, therefore C0 is implied to be zero.
2.BA0,1 &2 are bank select signals.The memory array is divided into banks 0, 1, 2, 3, 4, 5, 6 and 7. BA0, 1 & 2 define to which bank an active/read/write/precharge command is being applied.
3.AP defines the precharge mode when a read command or a write command is issued. If AP = high during a read or write command, auto precharge function is enabled.

CKE0 (input pin)
CKE0 controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE0 level must be kept for 2 clocks at least if CKE0 changes at the crossing point of the CK_t rising edge and the CK_c falling edge with proper setup time tIS, by the next CK_t rising edge CKE0 level must be kept with proper hold time tIH.

DQ0 to DQ31 (x32) - (input/output pins)
Data are input to and output from these pins.

DQS[3:0]_t, DQS[3:0]_c (input/ output pins)
DQS provide the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

DM0 to DM3 (input pins)
DM is the reference signals of the data input mask function. DM is sampled at the crossing point of DQS and VDDQ/2. When DM= high, the data input at the same timing are masked while the internal burst counter will be counting up.

DM truth table

Name (Functional)	DM	DQ	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes:
1.Used to mask write data. Provided coincident with the corresponding data.
2.Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table)

DQS and DM Correspondence Table

Part Number	Organization	DQS	Data Mask	DQ
FS704B2R1CH6A2KDE / FS704B2R1CH6A2KAM	x 32 bits	DQS0_t, /DQS0_c	DM0	DQ0 to DQ7
		DQS1_t, /DQS1_c	DM1	DQ8 to DQ15
		DQS2_t, /DQS2_c	DM2	DQ16 to DQ23
		DQS3_t, /DQS3_c	DM3	DQ24 to DQ31

VDD1, VSS, VSS2, VDDCA, VSSCA, VDDQ, VSSQ (power supply)
VDD1/2 and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers. VDDCA and VSSCA are power supply pins for command address input buffers.

2.3. STATE DIAGRAM

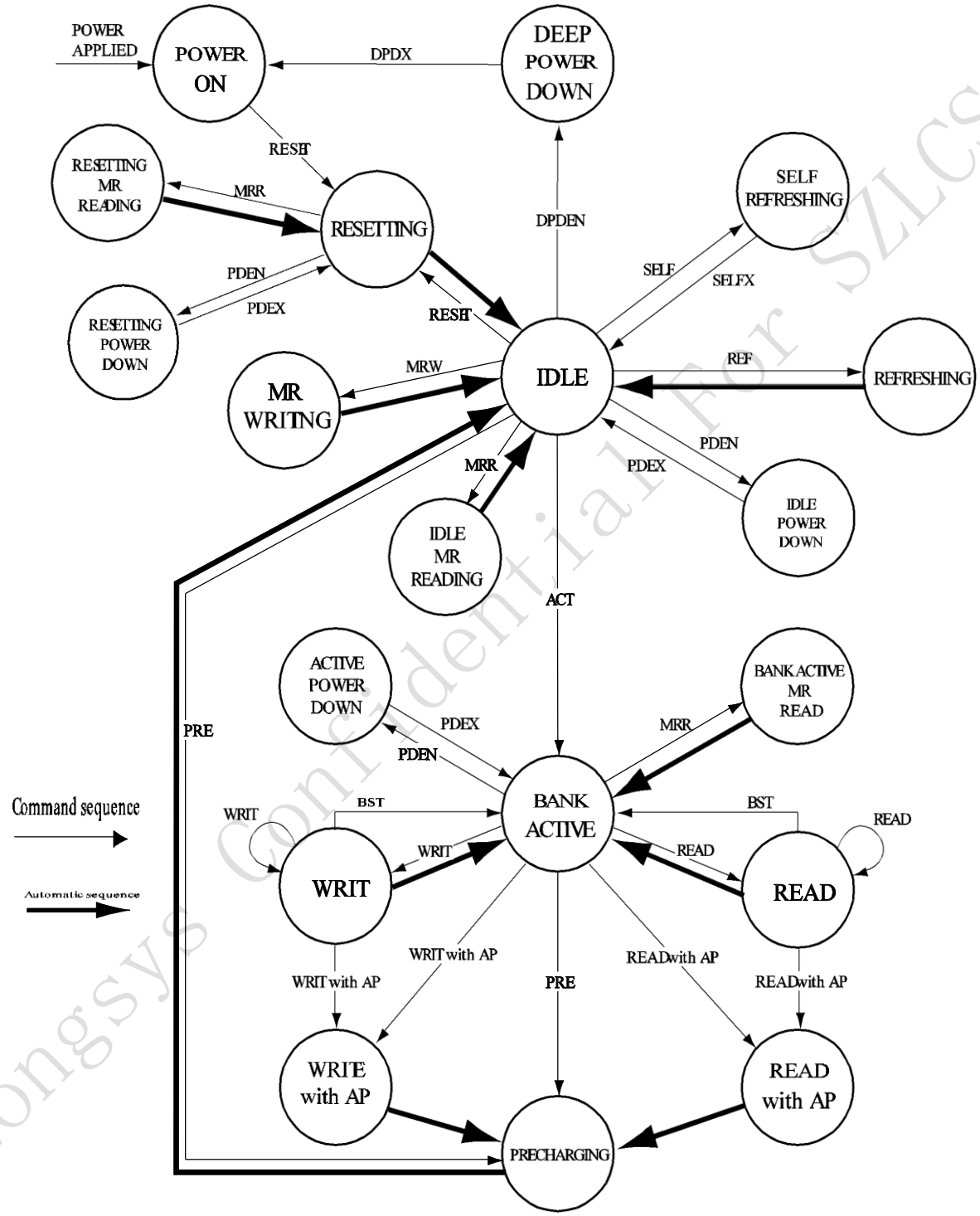


Figure 2-1 STATE DIAGRAM

3. Electrical Specifications

All voltages are referenced to each GND level (VSS, VSSCA, and VSSQ).
Execute power-up and Initialization sequence before proper device operation can be achieved.

3.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on any pin relative to VSSCA, VSSQ	VT	-0.4 to +1.6	V	
Power supply voltage (core power1) relative to VSS	VDD1	-0.4 to +2.3	V	
Power supply voltage (core power2) relative to VSS	VDD2	-0.4 to +1.6	V	
Power supply voltage for command, address relative to VSSCA	VDDCA	-0.4 to +1.6	V	
Power supply voltage for output relative to VSSQ	VDDQ	-0.4 to +1.6	V	
Storage temperature	Tstg	-55 to +125	°C	1
Power dissipation	PD	1	W	
Short circuit output current	IOUT	50	mA	

Notes:
1. Storage temperature the case surface temperature on the center/top side of the DRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

3.2. Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Grade	Notes
Operating case temperature	TC	-25 to +85	°C	Commercial	1
		-40 to +85	°C	Industrial	1

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

3.3. Recommended DC Operating Conditions

(TC = -40°C to +85°C)

Parameter		Symbol	min.	typical	max	Unit	Notes
Supply voltage	core power1	VDD1	1.7	1.8	1.95	V	1
		VSS	0	0	0	V	
	core power2	VDD2	1.14	1.2	1.3	V	1
		VSS	0	0	0	V	
	for command, address	VDDCA	1.14	1.2	1.3	V	1
		VSSCA	0	0	0	V	
	for output	VDDQ	1.14	1.2	1.3	V	1
		VSSQ	0	0	0	V	

Notes:
VDDQ tracks with VDD2, VDDCA tracks with VDD2. AC parameters are measured with VDD2, VDDCA and VDDQ tied together.

3.4. DC Characteristics 1

(TC = -40°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	Power Supply	Max							Unit
			1066	933	800	667	533	400	333	
Operating one bank active-precharge current	IDD01	VDD1	10							mA
	IDD02	VDD2	50							mA
	IDD0IN	VDDCA	6.5							mA
		VDDQ	1							mA
Idle power-down standby current	IDD2P1	VDD1	0.4							mA
	IDD2P2	VDD2	1.8							mA
	IDD2PIN	VDDCA	0.1							mA
		VDDQ	0.2							mA
Idle power-down standby current with clock stop	IDD2PS1	VDD1	0.4							mA
	IDD2PS2	VDD2	1.8							mA
	IDD2PSIN	VDDCA	0.1							mA
		VDDQ	0.2							mA
Idle non power- down standby current	IDD2N1	VDD1	0.6							mA
	IDD2N2	VDD2	15							mA
	IDD2NIN	VDDCA	6.5							mA
		VDDQ	1							mA
Idle non power- down standby current with clock stop	IDD2NS1	VDD1	0.6							mA
	IDD2NS2	VDD2	8							mA
	IDD2NSIN	VDDCA	6.5							mA
		VDDQ	1							mA
Active power-down standby current	IDD3P1	VDD1	1							mA
	IDD3P2	VDD2	10							mA
	IDD3PIN	VDDCA	0.1							mA
		VDDQ	0.2							mA
Active power-down standby current with clock stop	IDD3PS1	VDD1	1							mA
	IDD3PS2	VDD2	10							mA
	IDD3PSIN	VDDCA	0.1							mA
		VDDQ	0.2							mA
Active non power- down standby current	IDD3N1	VDD1	1.5							mA
	IDD3N2	VDD2	20							mA
	IDD3NIN	VDDCA	6.5							mA
		VDDQ	1							mA
Active non power- down standby current with clock stop	IDD3NS1	VDD1	1.5							mA
	IDD3NS2	VDD2	15							mA
	IDD3NSIN	VDDCA	6.5							mA
		VDDQ	1							mA
Operating burst read current	IDD4R1	VDD1	2							mA
	IDD4R2	VDD2	210	200	160	140	120	85	75	mA
	IDD4RIN	VDDCA	6.5							mA
Operating burst write current	IDD4W1	VDD1	2							mA
	IDD4W2	VDD2	280	265	210	190	160	110	100	mA
	IDD4WIN	VDDCA	6.5							mA
		VDDQ	30							mA

Parameter	Symbol	Power Supply	Max							Unit
			1066	933	800	667	533	400	333	
All Bank Auto Refresh Burst Current	IDD51	VDD1	35							mA
	IDD52	VDD2	143							mA
	IDD5IN	VDDCA	6.5							mA
		VDDQ	1							mA
All Bank Auto Refresh Average Current	IDD5ab1	VDD1	2							mA
	IDD5ab2	VDD2	18							mA
	IDD5abIN	VDDCA	6.5							mA
		VDDQ	1							mA
Per Bank Auto Refresh Average Current	IDD5pb1	VDD1	2							mA
	IDD5pb2	VDD2	18							mA
	IDD5pbIN	VDDCA	6.5							mA
		VDDQ	1							mA
Self Refresh Current (Standard Temerature Range: -30°C to 85°C)	IDD61	VDD1	850							µA
	IDD62	VDD2	3.5							mA
	IDD6IN	VDDCA	100							µA
		VDDQ	200							µA
Deep Power Down Current (Standard Temerature Range: -30°C to 85°C)	IDD81	VDD1	300							µA
	IDD82	VDD2	600							µA
	IDD8IN	VDDCA	70							µA
		VDDQ	200							µA
Self Refresh Current (Extended Temerature Range: 85°C to 105°C)	IDD6ET1	VDD1	3							mA
	IDD6ET2	VDD2	10							mA
	IDD6ETIN	VDDCA	100							µA
		VDDQ	300							µA
Deep Power Down Current (Extended Temerature Range: 85°C to 105°C)	IDD8ET1	VDD1	300							µA
	IDD8ET2	VDD2	1							mA
	IDD8ETIN	VDDCA	70							µA
		VDDQ	200							µA

3.5. Advanced Data Retention Current (Self-refresh current)

(TC = -40°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter		Symbol	supply	Typical	Unit	Test Condition
+25°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	192	µA	All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
		IDD62	VDD2	600	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	10		
	1/2 Array	IDD61	VDD1	144	µA	
		IDD62	VDD2	400	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	10		
	1/4 Array	IDD61	VDD1	120	µA	
		IDD62	VDD2	300	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	10		
	1/8 Array	IDD61	VDD1	108	µA	
		IDD62	VDD2	248	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	10		
+45°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	240	µA	
		IDD62	VDD2	760	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	15		
	1/2 Array	IDD61	VDD1	176	µA	
		IDD62	VDD2	520	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	15		
	1/4 Array	IDD61	VDD1	144	µA	
		IDD62	VDD2	384	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	15		
	1/8 Array	IDD61	VDD1	128	µA	
		IDD62	VDD2	320	µA	
		IDD6IN	VDDCA	1	µA	
			VDDQ	15		
+45°C ≤ TC ≤ +85°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	0.85	mA	
		IDD62	VDD2	3.5	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	200		
	1/2 Array	IDD61	VDD1	0.75	mA	
		IDD62	VDD2	3	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	200		
	1/4 Array	IDD61	VDD1	0.65	mA	
		IDD62	VDD2	2.7	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	200		
	1/8 Array	IDD61	VDD1	0.6	mA	
		IDD62	VDD2	2.5	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	200		

Parameter		Symbol	supply	Typical	Unit	Test Condition
+85°C ≤ TC ≤ +105°C CKE ≤ 0.2V	Full Array	IDD61	VDD1	3	mA	All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
		IDD62	VDD2	10	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	300		
	1/2 Array	IDD61	VDD1	2	mA	
		IDD62	VDD2	7	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	300		
	1/4 Array	IDD61	VDD1	1.5	mA	
		IDD62	VDD2	6	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	300		
	1/8 Array	IDD61	VDD1	1.2	mA	
		IDD62	VDD2	5	mA	
		IDD6IN	VDDCA	100	µA	
			VDDQ	300		

Note:
1 This device supports both bank-masking and segment-masking. IDD6 PASR currents are measured using bank-masking only.
2 IDD6 85°C/105°C are the maximum and IDD6 25°C/45°C are typical of the distribution of the arithmetic

3.6. DC Characteristics 2

(TC = -40°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min.	max	Unit	Test Condition
Input leakage current	ILI	-2	2	µA	0 ≤ VIN ≤ VDDQ
Output leakage current	ILO	-1.5	1.5	µA	0 ≤VOUT ≤VDDQ DQ = disable
Output high voltage	VOH	0.9×VDDQ	--	V	IOH = -0.1mA
Output low voltage	VOL	--	0.1×VDDQ	V	IOL = 0.1mA

3.7. DC Characteristics 3

(TC = -40°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min.	max	Unit
AC differential input voltage	VID (AC)	-0.2	VDDQ + 0.2	V
AC differential cross point voltage	VIX (AC)	0.5 x VDDQ - 0.15	0.5 x VDDQ + 0.15	V
AC differential cross point voltage	VOX (AC)	0.5 x VDDQ - 0.2	0.5 x VDDQ + 0.2	V

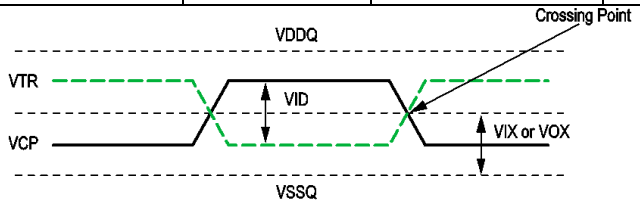


figure 3-1 Differential Signal Levels

3.8. Pin Capacitance

(TA = +25°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min/max	LPDDR2 1066-466	LPDDR2 400-200	Unit	Notes
CLK input pin capacitance: CK_t, /CK_c	CCK	min.	1		pF	1,2
		max	2			
CLK input pin capacitance Δ: CK_t, /CK_c	CDCK	min.	0		pF	1,2,3
		max	0.2	0.25		
Input pin capacitance: CA, CS_n, CKE0	CI	min.	1		pF	1,2,4
		max	2			
Input pin capacitance Δ: CA, CS_n, CKE0	CDI	min.	-0.4	-0.5	pF	1,2,5
		max	0.4	0.5		
Input/output pin capacitance: DQS_t, DQS_c, DQ, DM	CIO	min.	1.25		pF	1,2,6,7
		max	2.5			
Input/output pin capacitance Δ: DQS_t, /DQS_c	CDDQS	min.	0		pF	1,2,7,8
		max	0.25	0.3		
Input/output pin capacitance Δ : DQ, DM	CDIO	min.	-0.5	-0.6	pF	1,2,7,9
		max	0.5	0.6		
Calibration pin capacitance: ZQ	CZQ	min.	0		pF	1,2
		max	2.5			

Notes:

1. This parameter applies to die device only (does not include package capacitance)
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
3. Absolute value of CCK_t-CCK_c.
4. CI applies to /CS, CKE, CA0-CA9.
5. CDI=CI-0.5x(CCK_t+CCK_c)
6. DM loading matches DQ and DQS
7. MR3 I/O configuration DS OP3-OP0=4'b0001 (34.3Ω typical)
8. Absolute value of CDQS_t and CDQS_c.
9. CDIO=CIO-0.5x(CDQS_t+CDQS_c) in byte-lane.

3.9. Refresh Requirement Parameters (2Gb)

Parameter	Symbol	Value	Unit
Number of Banks		8	
Refresh Window Tcase ≤ 85°C	tREFW	32	ms
Refresh Window Tcase 85°C < Tcase ≤ 105°C	tREFW	8	ms
Required number of REFRESH commands (min)	R	8,192	
average time between REFRESH commands	tREFI	3.9	µs
Refresh Cycle time	tRFCab	130	ns
Per Bank Refresh Time	tRFCpb	60	ns
Burst Refresh Window = 4 x 8 x tRFC	tREFBW	4.16	µs

3.10. AC Characteristics

(TC = -40°C to +85°C, VDD1 = 1.7V to 1.95V, VDD2/VDDCA/VDDQ = 1.14V to 1.3V, VSS/VSSCA/VSSQ = 0V)

Parameter	Symbol	min/ max	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	Mbps
Max. Frequency		~		533	466	400	333	266	200	166	MHz
Clock Timing											
Average Clock Period	tCK(avg)	min		1.875	2.15	2.5	3	3.75	5	6	ns
		max		100							
Average high pulse width	tCH(avg)	min		0.45							tCK(avg)
		max		0.55							
Average low pulse width	tCL(avg)	min		0.45							tCK(avg)
		max		0.55							
Absolute Clock Period	tCK(abs)	min		tCK(avg)(min) + tJIT(per)(min)							ps
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs)	min		0.43							tCK(avg)
		max		0.57							
Absolute clock LOW pulse width (with allowed jitter)	tCH(abs)	min		0.43							tCK(avg)
		max		0.57							
Clock Period Jitter (with allowed jitter)	tJIT(per)	min		-90	-95	-100	-110	-120	-140	-150	ps
		max		90	95	100	110	120	140	150	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc)	max		180	190	200	220	240	280	300	ps
Duty cycle Jitter (with allowed jitter)	tJIT(duty) allowed	min		min((tCH(abs),min - tCH(avg),min) (tCL(abs), min - tCL(avg), min)) x tCK(avg)							ps
		max		max((tCH(abs),max - tCH(avg),max) (tCL(abs), max - tCL(avg), max))x tCK(avg)							
Cumulative error across 2 cycles	tERR(2per) allowed	min		-132	-140	-147	-162	-177	-206	-221	ps
		max		132	140	147	162	177	206	221	
Cumulative error across 3 cycles	tERR(3per) allowed	min		-157	-166	-175	-192	-210	-245	-262	ps
		max		157	166	175	192	210	245	262	
Cumulative error across 4 cycles	tERR(4per) allowed	min		-175	-185	-194	-214	-233	-272	-291	ps
		max		175	185	194	214	233	272	291	
Cumulative error across 5 cycles	tERR(5per) allowed	min		-188	-199	-209	-230	-251	-293	-314	ps
		max		188	199	209	230	251	293	314	
Cumulative error across 6 cycles	tERR(6per) allowed	min		-200	-210	-222	-244	-266	-311	-333	ps
		max		200	210	222	244	266	311	333	
Cumulative error across 7 cycles	tERR(7per) allowed	min		-209	-221	-232	-256	-279	-325	-348	ps
		max		209	221	232	256	279	325	348	
Cumulative error across 8 cycles	tERR(8per) allowed	min		-217	-229	-241	-256	-290	-338	-362	ps
		max		217	229	241	256	290	338	362	
Cumulative error across 9 cycles	tERR(9per) allowed	min		-224	-237	-249	-274	-299	-349	-374	ps
		max		224	237	249	274	299	349	374	
Cumulative error across 10 cycles	tERR(10per) allowed	min		-231	-244	-257	-282	-308	-359	-385	ps
		max		231	244	257	282	308	359	385	
Cumulative error across 11 cycles	tERR(11per) allowed	min		-237	-250	-263	-289	-316	-368	-395	ps
		max		237	250	263	289	316	368	395	
Cumulative error across 12 cycles	tERR(12per) allowed	min		-242	-256	-269	-296	-323	-377	-403	ps
		max		242	256	269	296	323	377	403	
Cumulative error across n = 13, 14 … 49, 50 cycles	tERR(nper) allowed	min		tERR(nper), allowed, min = (1 + 0.68ln(n)) x tJIT(per), allowed, min							ps
		max		tERR(nper), allowed, max = (1 + 0.68ln(n)) x tJIT(per), allowed, max							

Parameter	Symbol	min/ max	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	Mbps
Max. Frequency		~		533	466	400	333	266	200	166	MHz
ZQ Calibration Parameters											
Initialization Calibration Time	tZQINIT	min		1							µs
Long Calibration Time	tZQCL	min	6	360							ns
Short Calibration Time	tZQCS	min	6	90							ns
Calibration Reset Time	tZQRESET	min	3	50							ns
Read Parameters											
DQS output access time from CK_t/CK_c	tDQSCK	min		2500							ps
		max		5500							
DQSCK Delta Short	tDQSCKDS	max		330	380	450	540	670	900	1080	ps
DQSCK Delta Medium	tDQSCKDM	max		680	780	900	1050	1350	1800	1900	ps
DQSCK Delta Long	tDQSCKDL	max		920	1050	1200	1400	1800	2400	-	ps
DQS-DQ skew	tDQSQ	max		200	220	240	280	340	400	500	ps
Data hold skew factor	tQHS	max		230	260	280	340	400	480	600	ps
DQS Output High Pulse Width	tQSH	min		tCH(abs) - 0.05							tCK(avg)
DQS Output Low Pulse Width	tQSL	min		tCL(abs) - 0.05							tCK(avg)
Data Half Period	tQHP	min		min(tQSH, tQSL)							tCK(avg)
DQ/DQS output hold time from DQS	tQH	min		tQHP-tQHS							ps
Read preamble	tRPRE	min		0.9							tCK(avg)
Read Postamble	tRPST	min		tCL(abs) - 0.05							tCK(avg)
DQS low-Z from clock	tLZ(DQS)	min		tDQSCK(min) - 300							ps
DQ low-Z from clock	tLZ(DQ)	min		tDQSCK(min) - (1.4*tQHS(max))							ps
DQS high-Z from clock	tHZ(DQS)	max		tDQSCK(max) - 100							ps
Write Parameters											
DQ and DM input hold time (Vref based)	tDH	min		210	235	270	350	430	480	600	ps
DQ and DM input setup time (Vref based)	tDS	min		210	235	270	350	430	480	600	ps
DQ and DM input pulse width	tDIPW	min		0.35							tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min		0.75							tCK(avg)
		max		1.25							tCK(avg)
DQS input high-level width	tDQSH	min		0.4							tCK(avg)
DQS input low-level width	tDQSL	min		0.4							tCK(avg)
DQS falling edge to CK setup time	tDSS	min		0.2							tCK(avg)
DQS falling edge hold time from CK	tDSH	min		0.2							tCK(avg)
Write postamble	tWPST	min		0.4							tCK(avg)
Write preamble	tWPRE	min		0.35							tCK(avg)
CKE Input Parameters											
CKE min. pulse width (high and low pulse width)	tCKE	min	3	3							tCK(avg)
CKE input setup time	tISCKE	min		0.25							tCK(avg)
CKE input hold time	tIHCKE	min		0.25							tCK(avg)

Parameter	Symbol	min/ max	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	Mbps
Max. Frequency		~		533	466	400	333	266	200	166	MHz
Command Address Input Parameters											
Address & control input setup time (Vref based)	tIS	min		220	250	290	370	460	600	740	ps
Address & control input hold time (Vref based)	tIH	min		220	250	290	370	460	600	740	ps
Address & control input pulse width	tIPW	min		0.4							tCK(avg)
Boot Parameters (10 MHz - 55 MHz)											
Clock Cycle Time	tCKb	max		100							
		min	-	18							ns
CKE input setup time	tISCKEb	min	-	2.5							ns
CKE input hold time	tIHCKEb	min	-	2.5							ns
Address & control input setup time	tISb	min	-	1150							ps
Address & control input hold time	tIHb	min	-	1150							ps
DQS Output data access time from CK_t/CK_c	tDQSCKb	min		2							
		max	-	10							ns
Data strobe edge to output data edge tDQSQb-1.2	tDQSQb	max	-	1.2							ns
Data hold skew factor	tQHSb	max	-	1.2							ns
Mode Register Parameters											
Mode Register Write command period	tMRW	min	5	5							tCK(avg)
Mode Register Read command period	tMRR	min	2	2							tCK(avg)
LPDDR2 SDRAM Core Parameters											
Read Latency	RL	min	3	8	7	6	5	4	3	3	tCK(avg)
Write Latency	WL	min	1	4	4	3	2	2	1	1	tCK(avg)
Active to Active command period	tRC	min	-	tRAS + tRPab (with all-bank Precharge) tRAS + tRPab (with per-bank Precharge) ns							
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min	3	15							ns
Self refresh exit to next valid command delay	tXSR	min	2	tRFCab+10							ns
Exit power down to next valid command delay	tXP	min	2	7.5							ns
LPDDR2-S4 CAS to CAS delay	tCCD	min	2	2							tCK(avg)
Internal Read to Precharge command delay	tRTP	min	2	7.5							ns
RAS to CAS Delay	tRCD	min	3	18							ns
Row Precharge Time (single bank)	tRPpb	min	3	18							ns
Row Precharge Time (all banks)	tRPab	min	3	21							ns
Row Active Time	tRAS	min	3	42							ns
		max	-	70							µs
Write Recovery Time	tWR	min	3	15							ns
Internal Write to Read command delay	tWTR	min	2	7.5					10		ns
Active bank A to Active bank B	tRRD	min	2	10							ns
Four Bank Activate window	tFAW	min	8	50						60	ns
Minimum Deep Power Down time	tDPD	min		500							µs

3.11. Timing Parameters for Initialization

Symbol	Value		Unit	Test Condition
	min.	max		
tINIT0	--	20	ms	Maximum Power Ramp Time
tINIT1	100	--	ns	Minimum CKE low time after completion of power ramp
tINIT2	5	--	tCK	Minimum stable clock before first CKE high
tINIT3	200	--	µs	Minimum Idle time after first CKE assertion
tINIT4	1	--	µs	Minimum Idle time after Reset command, this time will be about 2 × tRFCab (max density) +tRP
tINIT5	--	10	µs	Maximum duration of Device Auto-Initialization
tCKBOOT	18	100	ns	Clock cycle time during boot

3.12. Mode Register Assignment

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Remark
0	00h	Device Info.	R	(RFU)						DI	DAI	See MR0
1	01h	Device Feature 1	W	nWR (for AP)			WC	BT	BL			See MR1
2	02h	Device Feature 2	W	(RFU)				RL & WL				See MR2
3	03h	I/O Config-1	W	(RFU)				DS				See MR3
4	04h	SDRAM Refresh Rate	W	TUF	(RFU)				Refresh Rate			See MR4
5	05h	Basic Config-1	R	Company ID								See MR5
6	06h	Basic Config-2	R	Revision ID1								See MR6
7	07h	Basic Config-3	R	Revision ID2								See MR7
8	08h	Basic Config -4	R	I/O Width		Density				Type		See MR8
9	09h	Test Mode	W*1	Vendor-Specific Test Mode								See MR9
10	0Ah	IO Calibration	W	Calibration Code								See MR10
11:15	0Bh TO 0Fh	Reserved		(RFU)								
16	10h	PASR_Bank	W	Bank Mask								See MR16
17	11h	PASR_Seg	W	Segment Mask								See MR17
18:23	12h TO 17h	Reserved		(RFU)								
MR No.24 to 31 are Non-Volatile Memory (NVM) specific mode registers, which LPDDR2 does not have.												
32	20h	Calibration Pattern A	R	Calibration Pattern A								See MR32
40	28h	Calibration Pattern B	R	Calibration Pattern B								See MR40
63	3FH	Reset	W	×								See MR63
MR No. 33 to 39, 41 to 62 and MR 64 to 255 are reserved.												

Note:
MR9[5] is Fail Bit, and Read-Only.
Remarks:
R = read-only , W = write-only
DAI = Device Auto-Initialization
DI = Device Information
nWR = Write Recovery for auto precharge
WC = Wrap Control
BT = Burst Type
BL = Burst Length
RL & WL = Read latency & Write latency
DS = Drive Strength
TUF = Temperature Update Flag

MR0_Device Information

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	02H	Device Info.	R	(RFU)						DI	DAI

Device Auto-Initialization	Read-only	0	DAI complete
		1	DAI still in progress
Device Information	Read-only	0	SDRAM
		1	Reserved

MR1_Device Feature 1

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
1	01h	Device Feature 1	W	nWR (for AP)			WC	BT	BL		

Burst Length	Write-only	010	BL4 (default)
		011	BL8
		100	BL16
		Other	Reserved
Burst Type	Write-only	0	Sequential (default)
		1	Interleaved
Wrap Control	Write-only	0	Wrap (default)
		1	No Wrap
Write Recovery for Autoprecharge*	Write-only	001	nWR=3 (default)
		010	nWR=4
		011	nWR=5
		100	nWR=6
		101	nWR=7
		110	nWR=8
		Other	Reserved

Note:
Programmed value in nWR register is the number of clock cycles which determined when to start internal precharge operation for a write burst with AP enabled. It is determined by RU (tWR/tCK).

MR2_Device Feature 2

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
2	02h	Device Feature 2	W	(RFU)				RL & WL			

Read latency and Write latency	Write-only	0001	RL3/WL1 (default)
		0010	RL4/WL2
		0011	RL5/WL2
		0100	RL6/WL3
		0101	RL7/WL4
		0110	RL8/WL4
		Other	Reserved

MR3_I/O Configuration1

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
3	03h	I/O Config-1	W	(RFU)				DS			

Drive Strength	Write-only	0000	Reserved
		0001	34.3Ω typical
		0010	40Ω typical (default)
		0011	48Ω typical
		0100	60Ω typical
		0101	reserved for 68.6Ω typical
		0110	80Ω typical
		0111	120Ω typical
		Other	Reserved

MR4_Device Temperature

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
4	04h	SDRAM Refresh Rate	W	TUF	(RFU)				Refresh Rate		

Refresh Rate	Read-only	000	Reserved
		001	Reserved
		010	2 × tREFI
		011	1 × tREFI
		100	Reserved
		101	0.25 × tREFI, set to 85C, do not derate
		110	0.25 × tREFI, set to 95C, de-rate
		111	temp>105C, set to 105C, stall
Temperature Update Flag	Read-only	0	OP<2:0> value has not changed since last read of MR4.
		1	OP<2:0> value has changed since last read of MR4.

MR5_Basic Configuration 1

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
5	05h	Basic Config-1	R	Wafer ID							

Wafer ID ID	Read-only	11111101

MR6_Basic Configuration 2& MR7_Basic Configuration 3

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
6	06h	Basic Config-2	R	Revision ID1							
7	07h	Basic Config-3	R	Revision ID2							

Revision ID1	Read-only	00000000	Version A
Revision ID2	Read-only	00000000	Version A

MR8_Basic Configuration 4

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
8	08h	Basic Config -4	R	I/O Width		Density				Type	

Type	Read-only	00	**S4 SDRAM**
		01	Reserved
		10	Reserved
		11	Reserved
Density	Read-only	0010	256Mb
		0011	512Mb
		0100	1Gb
		0101	**2Gb**
		0110	4Gb
		0111	8Gb
		1000	16Gb
		1001	32Gb
		Other	Reserved
I/O Width	Read-only	00	**x32**
		01	x16
		10	x8
		11	Not used

MR9_Test Mode

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
9	09h	Test Mode	W	Vendor-Specific Test Mode							

Failed Die Bit[5]	Read-only	0	Pass (default)
		1	Fail
Tested Die Bit [4]	Read-only	0	Untested
		1	Tested (default)

MR10_Calibration

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
10	0Ah	IO Calibration	W	Calibration Code							

Calibration Code	Write-only	hFF	Calibration command after initialization
		hAB	Long calibration
		h56	Short calibration
		hC3	ZQ Reset
		others	Reserved

MR16_PASR_Bank Mask

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10h	PASR_Bank	W	Bank Mask(4-Bank or 8 Bank)							

Bank [7:0] Mask	Write-only	0	Refresh enable to the bank (=unmasked, default)
		1	Refresh blocked (=masked)

MR17_PASR_Segment Mask

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
17	11h	PASR_Seg	W	Segment Mask							

Seg [7:0] Mask	Write-only	0	Refresh enable to the segment (=unmasked, default)
		1	Refresh blocked (=masked)

MR32_DQ calibration A& MR40_DQ calibration B

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20h	Calibration Pattern A	R	Calibration Pattern A							
40	28h	Calibration Pattern B	R	Calibration Pattern B							

	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
DQ outputs pattern A	1	0	1	0
DQ outputs pattern B	0	0	1	1

NAND Flash

4. Addressing

Address Cycle Map

Bus cycle	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	L	L	L	L	
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	
5th Cycle	A28	A29	L	L	L	L	L	L	

NOTE :
Column Address : Starting Address of the Register.
A0 - A11 : column address in the page
A12 - A17 : page address in the block
A18 : plane address
A19 – A29 : block address
L must be set to "Low".

Block Arrangement

Row Address	Block Number	DQ2
000000h ~ 00003Fh	Block 0 (Plane 0)	Main Block (4,096Blocks)
000040h ~ 00007Fh	Block 1 (Plane 1)	
000080h ~ 0000BFh	Block 2 (Plane 0)	
0000C0h ~ 0000FFh	Block 3 (Plane 1)	
000100h ~ 00013Fh	Block 4 (Plane 0)	
000140h ~ 00017Fh	Block 5 (Plane 1)	
...	...	
03FF00h ~ 03FF3Fh	Block 4092 (Plane 0)	
03FF40h ~ 03FF7Fh	Block 4093 (Plane 1)	
03FF80h ~ 03FFBFh	Block 4094 (Plane 0)	
03FFC0h ~ 03FFFFh	Block 4095 (Plane 1)	

5. Command Sets

Command Sets

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h			
READ FOR COPY-BACK	00h	35h			
READ ID	90h	-			
RESET	FFh	-			Yes
READ CACHE (START)	31h				
READ CACHE (END)	3Fh	-			
PAGE PGM (start) / CACHE PGM (end)	80h	10h			
CACHE PGM (Start/continue)	80h	15h			
PAGE RE-PROGRAM	8Bh	10h			
COPY BACK PGM	85h	10h			
BLOCK ERASE	60h	D0h			
READ STATUS REGISTER	70h	-			Yes
RANDOM DATA INPUT	85h	-			
RANDOM DATA OUTPUT	05h	E0h			
READ CACHE ENHANCED (RANDOM)	00h	31h			
READ PARAMETER PAGE	ECh	-			
READ STATUS ENHANCED	78h	-			Yes

Extended Command Set

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
(Traditional)MULTI-PLANE PROGRAM	80h	11h	81h	10h	No
ONFI MULTI-PLANE PROGRAM	80h	11h	80h	10h	No
MULTI-PLANE PAGE RE-PROGRAM	8Bh	11h	8Bh	10h	No
(Traditional)MULTI-PLANE CACHE PGM(start/cont)	80h	11h	81h	15h	No
ONFI MULTI-PLANE CACHE PGM(start/cont)	80h	11h	80h	15h	No
(Traditional)MULTI -PLANE CACHE PGM(end)	80h	11h	81h	10h	No
ONFI MULTI-PLANE CACHE PGM(end)	80h	11h	80h	10h	No
(Traditional) MULTI-PLANE COPY-BACK PROGRAM	85h	11h	81h	10h	No
ONFI MULTI -PLANE COPY-BACK PROGRAM	85h	11h	85h	10h	No
(Traditional) MULTI -PLANE BLOCK ERASE	60h	60h	D0h	-	No
ONFI MULTI-PLANE BLOCK ERASE	60h	D1h	60h	D0h	No

5.1. Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 45nsec (1.8V version) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.
After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.

5.2. Page Program

A page program cycle consists of a serial data loading period in which up to 2112 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropri- ate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multi- ple times regardless of how many times it is done in a page.
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the sys- tem controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issu ed to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. The device is programmed basically by page, but it also allows multiple partial page programming.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

5.3. Page Re-program

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. On the other hand, if the pattern bound for the target page is differ- ent from that of the previous page, data in cycles can be issued before program confirm “10h”

The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multi- ple times regardless of how many times it is done in a page. The “program confirm” command (10h) initiates the re- programming process.

The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register. The system controller can detect the completion of a pro- gram cycle by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status com- mand and Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

5.4. Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A18 to A29 is valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/B output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress.When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

5.5. Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations.
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for tRST after the Reset command is written.

5.6. Copy-back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112 bytes(x8 Device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in "Copy Back Program with Random Data Input". "When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, four bit error correction is recommended for the use of Copy-Back operation. shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy back, while it must be set to Vcc When performing the program.

5.7. Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs . This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to "**Table 8-2 Status Register Coding**" for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

5.8. Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the follow- ing cases:
- on a specific die of a multi-dice stack configurations (single CE), in case of concurrent operations.
When 4Gbit dice are stacked(*) to form 8Gbit DDP or 16Gbit QDP (single CE), it is possible to run a first operation on the first 4Gbit, then activate a concurrent operation on the second (or third or fourth) device. (examples: Erase while Read, Read while Program, etc.)
- on a specific plane in case of multi-plane operations in the same die.

Status register is dynamic in other words, user is not required to toggle RE / CE to update it.

Status Register Coding

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program/ Cache reprogram	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Not use	Pass/Fail(N)	N Page Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Not use	Pass/Fail(N-1)	N-1 Page Pass : "0" Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 3	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 4	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 5	Ready/Busy	Ready/Busy	Ready/Busy	P/E/R Controller Bit	Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	N/A	Write Protect	Protected : "0" Not Protected : "1"

Notes:
1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2. I/O1: This bit is only valid for cache program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache program sequence. When Cache program is not supported, this bit is not used.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4. I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the operation is complete.

5.9. Cache Read (available only within a block)

The Cache read function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence. The Cache read function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache read function. Issuing an additional Cache read function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command.
The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.
The host shall not issue a sequential Cache read (31h) command after the page of the device is read.

5.10. Cache Program (available only within a block)

Cache Program is used to improve the program throughput by programing data using the cache register. The cache program operation can only be used within one block. The cache register allows new data to be input while the previous data that was transffered to the page buffer is programmed into the memory array. Cache program is available only within a block. After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state For a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h). The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is conse quently processed through a pipeline model. In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCB-SYW). Read Status commands (70h) may be issued to check the status of the different registers, and the pass/ fail status of the cached program operations. More in detail: a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data. b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete. c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1" . d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while pro-gramming page N. The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the page of the target program sequence must be programmed with Page

Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the programming is finished before starting any other operation.
More in detail:

a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete.
c) the Cache Program error bit I/O<1> can be used to identify if the previous page(page N-1) has been successfully programmed or not in Cache Program operation. The latter can be polled upon I/O<6> status bit changing to "1" .
d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while pro-gramming page N. The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

5.11. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

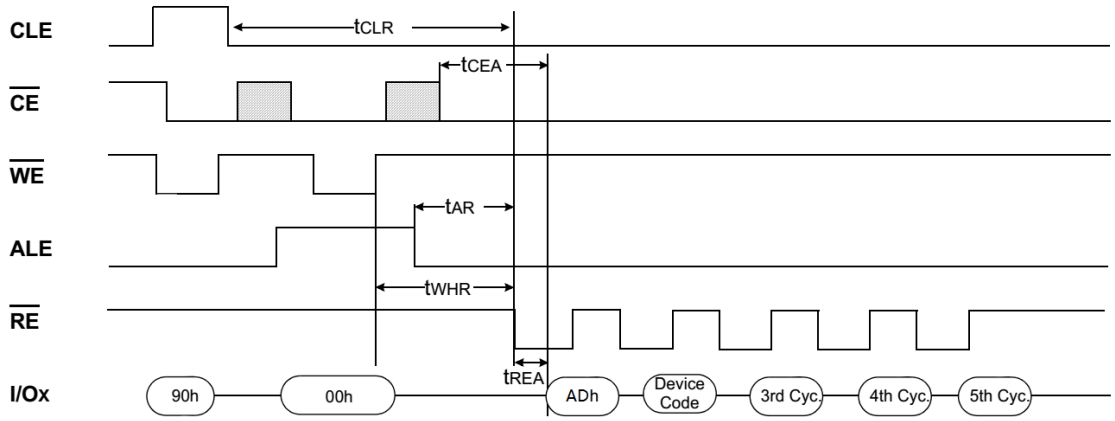


Figure 5-1 Read ID Sequence

00h Address ID cycle

Part Number	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
FS704B2R1CH6A2KDE	ADh	ACh	90h	15h	56h

3rd ID Data

	Description	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between multiple chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Redundant Area Size (byte/512byte)	16 32						0 1		
Organization	x8 x16		0 1						
Serial Access Minimum	45ns 25ns Reserved Reserved	0 0 1 1				0 1 0 1			

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1bit/512Bytes 2bit/512Bytes 4bit/512Bytes 8bit/512Bytes							0 0 1 1	0 1 0 1
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size (W/O redundant Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved		0							

5.12. Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values.

5.13. Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. This data structure enables the host processor to automatically recognize the Nand Flash configuration of a device. The whole data structure is repeated at least three times.
The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.
The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.
Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

Parameter Page Data Structure Definition

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache command 0 1 = supports Page Cache Program command
10-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)

	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1

131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	tPROG Maximum page program time (µs)
135-136	M	tBERS Maximum block erase time (µs)
137-138	M	tR Maximum page read time (µs)
139-163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Note:
"O" Stands for Optional, "M" for Mandatory

5.14. Multi-plane program

Device supports multi-plane program: it is possible to program 2 pages in parallel, one per each plane.
A multi-plane program cycle consists of a double serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. Address for this page must be in the 1st plane(A18=0 for x8 devices). The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (tDBSY).

Once it has become ready again, either the traditional "81h" or the ONFI 1.0 "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be in the 2nd plane (A18=1 for x8 devices).Program Confirm command (10h) makes parallel programming of both pages to start.

User can check operation status by monitoring R/B pin or reading status register commands (70h or 78h), as if it were a normal page program: read status register command is also available during Dummy Busy time (tDBSY).
In case of fail in any of 1st and 2nd page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "Read Status Enhanced" command must be issued. The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

5.15. Multi-plane copy-back Program

As for page program, device supports Multi-plane copy back program with exactly same sequence and limitations. Multi-plane copy back program must be preceded by 2 single page read for copy back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).
Multi-plane copy back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.
Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) , and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h).

5.16. Multi-plane Block Erase

Multi-plane erase, allows parallel erase of two blocks in parallel, one per each memory plane. Two different command sequences are allowed in these case, traditional and ONFI 1.0. In traditional case, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start. In this case, multi-plane erase does not need any Dummy Busy Time between 1st and 2nd block insertion.

As an alternative, the ONFI 1.0 multi-plane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multi-plane confirm). Between the two block-related sequences, a short busy time tIEBSY will occur.

Address limitation required for multi-plane program applies also to multi-plane erase. Also operation progress can be checked like in the multi-plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced. As for multi-plane page program, the address of the first second page must be within the first plane (A18=0 for x8 devices) and second plane (A18 = 1 for devices), respectively.

5.17. Multi-plane Cache Program

The device supports multi-plane cache program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache.
The device supports both the traditional and ONFI 1.0 command sets.

The command sequence can be summarized as follows:
a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A18=0 for x8 devices. The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.
b)The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).
c)Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A18=1 for x8 devices). The data of 2nd page other than those to be programmed do not need to be loaded.
d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence.

The sequence 80h-...- 11h...-...81h...-...15h (or the corresponding ONFI 80h-...- 11h...-...80h...-...15h) can be iter- ated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.

The sequence to end multi-plane cache program is 80h-...- 11h...-...81h...-...10h (or 80h-...- 11h...-...80h...-...10h for the ONFI 1.0 case). Multi-plane Cache program is available only within two paired blocks belonging to the two planes..

User can check operation status by R/B pin or read status register commands (70h or 78h)
If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes. More in detail:

a) I/O<6> indicates when both cache registers are ready to accept new data.
b) I/O<5> indicates when the cell programming of the current data registers is complete
c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1".
d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".

If the system monitor the progress of the operation only with R/B, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

6. Electrical Characteristic

6.1. Valid Block

The Number of Valid Block

Part Number	Symbol	Min	Typ.	Max	Unit
FS704B2R1CH6A2KDE	NVB	4,016	-	4,096	Blocks

Notes:
1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

6.2. Recommended Operating Conditions

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	VCC	1.7	1.8	1.95	V
Ground Supply Voltage	VSS	0	0	0	V

6.3. Absolute Maximum DC Ratings

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	VCC	-0.6 to + 2.6	V
	VIN	-0.6 to + 2.6	
	VI/O	-0.6 to +2.6	
Ambient Operating Temperature	TA	-40 to +85	℃

NOTE :
Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -1.0V for periods <30ns.
Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+1.0V for periods <20ns.
tablePermanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet.
Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.4. DC Operating Characteristics

DC & Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power on reset current	ICC0	FFh command input after power on			50 per device	mA
Page Read Access Operation Current	ICC1	tRC=45ns CE#=VIL, IOUT=0mA	-	10	20	mA
Program Operation Current	ICC2	Normal	-	-	20	
		Cache		-	30	
Erase Operation Current	ICC3	-		10	20	
Stand-by Current (TTL)	ICC4	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)	ICC5	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	µA
Input Leakage Current	ILI	VIN=0 to VCC(max)	-	-	±10	
Output Leakage Current	ILO	VOUT=0 to VCC(max)	-	-	±10	
Input High Voltage	VIH1)	-	0.8xVCC	-	VCC+0.3	V
Input Low Voltage, All inputs	VIL1)	-	-0.3	-	0.2xVCC	
Output High Voltage Level	VOH	IOH=-100µA	VCC-0.1	-	-	
Output Low Voltage Level	VOL	IOL=100µA	-	-	0.1	
Output Low Current (R/B#)	IOL(R/B#)	VOL=0.1V	3	4	-	mA

6.5. Input / Output Capacitance (TA=25℃, VCC=1.8V, f=1.0Mhz)

Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE :
Capacitance is periodically sampled and not 100% tested.

6.6. Read / Program / Erase Characteristics

NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	tR	-		30	μs
Read Cache busy time	tCBSYR	-	5	tR	μ s
Program Time	tPROG	-	300	700	μs
Cache Program short busy time	tCBSYW	-	5	tPROG	μs
Number of Partial Program Cycles	Nop	-	-	4	cycles
Block Erase Time	tBERS	-	3.5	10	ms

NOTE :
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.
Typical value is measured at Vcc=1.8 V, TA=25℃ (1.8V Device).Not 100% tested.

6.7. AC Timing Parameters Table

AC Timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS[1)]	25	-	ns
CLE Hold Time	tCLH	10	-	ns
CE# Setup Time	tCS[1)]	35	-	ns
CE# Hold Time	tCH	10	-	ns
WE# Pulse Width	tWP	25	-	ns
ALE Setup Time	tALS[1)]	25	-	ns
ALE Hold Time	tALH	10	-	ns
Data Setup Time	tDS[1)]	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	45	-	ns
WE# High Hold Time	tWH	15	-	ns
Address to Data Loading Time	tADL[2)]	100	-	ns
ALE toRE# Delay	tAR	10	-	ns
CLE to RE# Delay	tCLR	10	-	ns
Ready to RE# Low	tRR	20	-	ns
RE# Pulse Width	tRP	25	-	ns
WE# High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	45	-	ns
RE# Access Time	tREA	-	30	ns
RE# High to Output Hi-Z	tRHZ	-	100	ns
CE# High to Output Hi-Z	tCHZ	-	50	ns
CE# High to ALE or CLE Don't Care	tCSD	10	-	ns
RE# High to Output Hold	tRHOH	15	-	ns
RE# Low to Output Hold	tRLOH	0		ns
Data Hold Time after CE# Disable	tCOH	15	-	ns
RE# High Hold Time	tREH	15	-	ns
Output Hi-Z to RE# Low	tIR	0	-	ns
RE# High to WE# Low	tRHW	100	-	ns
WE# High to RE# Low	tWHR	60	-	ns
WE# high to RE# low for Random data out	tWHR2	200		ns
CE# low to RE# low	tCR	10		
Device Resetting Time (Read/Program/Erase)	tRST	-	5/10/500 [1)]	μs
Write protection time	tWW	100		

NOTE :
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. In case of first reset after initial powering up, it takes max 5ms.

7. NAND FLASH TECHNICAL NOTES

7.1. Initial Invalid Block(s)

The initial invalid blocks are included in the device while it gets shipped called. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. During the time of using the device, the additional invalid blocks might be increasing; therefore, it is recommended to check the invalid block marks and avoid using the invalid blocks. Furthermore, please read out the initial invalid block and the increased invalid block information before any erase operation since it may be cleared by any erase operation.

7.2. Identifying Initial Invalid Block(s)

While the device is shipped, the value of all data bytes of the good blocks are FFh. The initial invalid block(s) status is defined by the 1st byte in the spare area. Longsys makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart (**Figure 11-1**). The erase operation at the invalid block is not recommended.

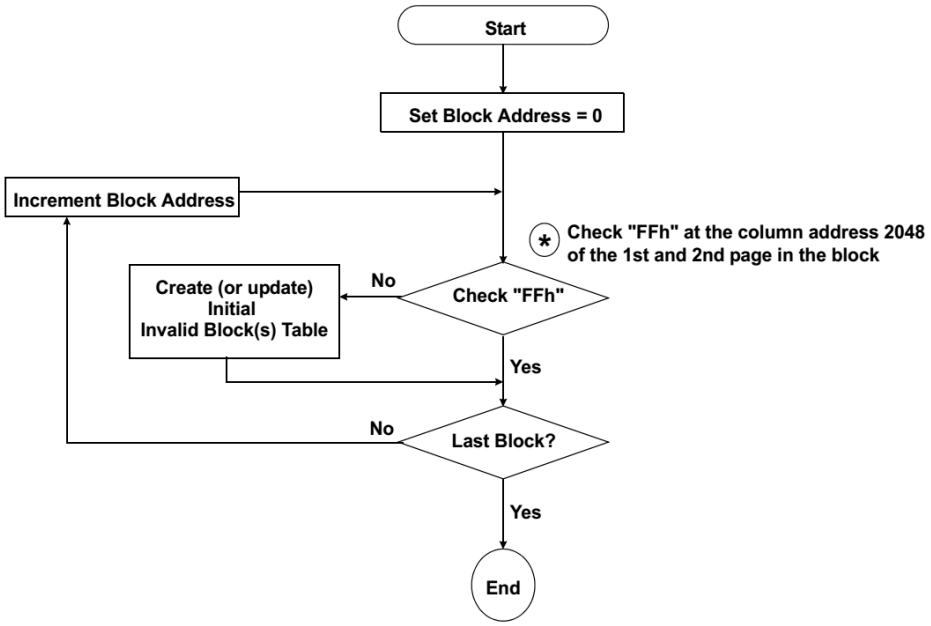


Figure 7-1 Flow Chart to Create Initial Invalid Block Table

Notes:
1. Do not try to erase the detected blocks, because the bock information will be lost.
2. Do not perform program and erase operation in invalid block, it is impossible to guarantee the Input data and to ensure that the function is normal.

7.3. Error in Write or Read Operation

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.Block replacement should be done while status read failure after erase or program. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Cases

	Failure Mode	**Detection and Countermeasure Sequence**
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

ECC:

Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

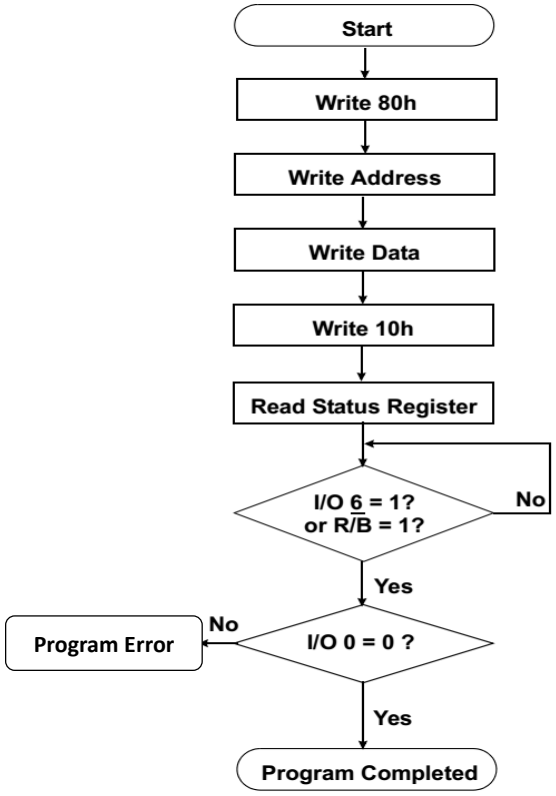
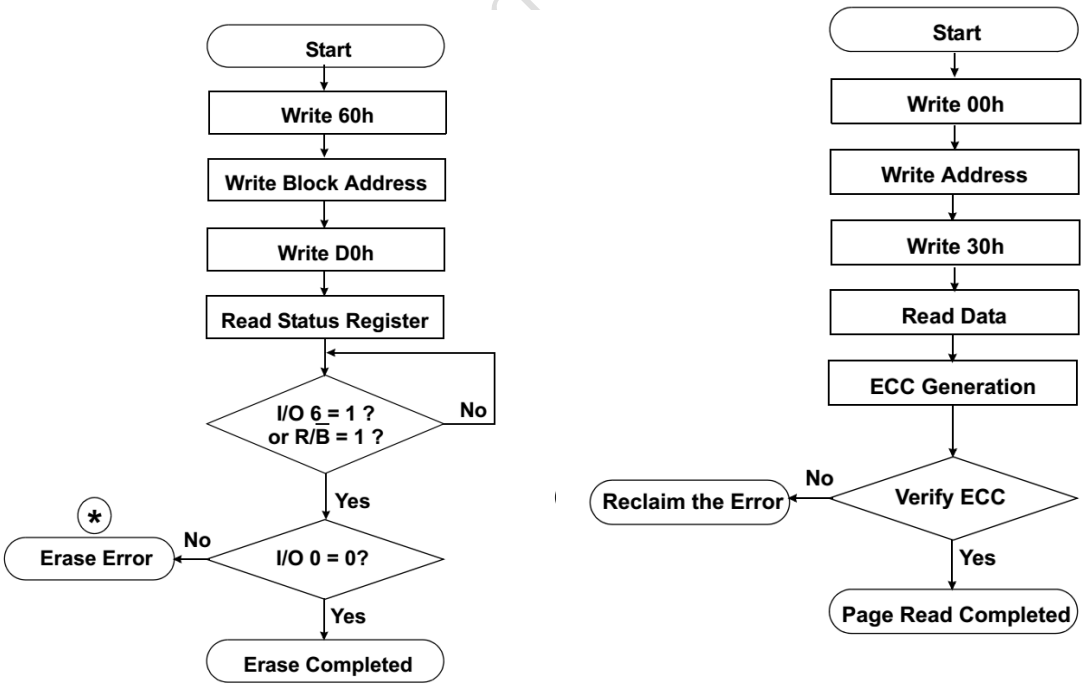


Figure 7-2 Program Flow Chart

If program operation results in an error, map out the block including the page in error and copy the target data to another block.



*If erase operation results in an error, map out the failing block and replace it with another block.

Figure 7-3 Erase Flow Chart& Read Flow Chart

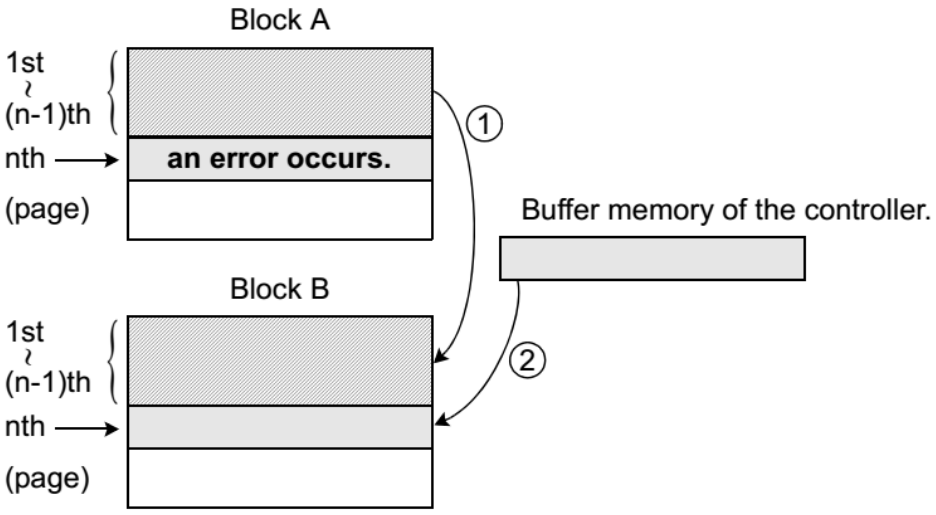


Figure 7-4 Block Replacement

1.When an error happens in the nth page of the Block 'A' during erase or program operation.
2.Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block'B')
3. Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block'B'.
4. Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

8. Nand Flash Timing

8.1. Data Protection & Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.1V(1.8V device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences. The two step command sequence for program/erase provides additional software protection.

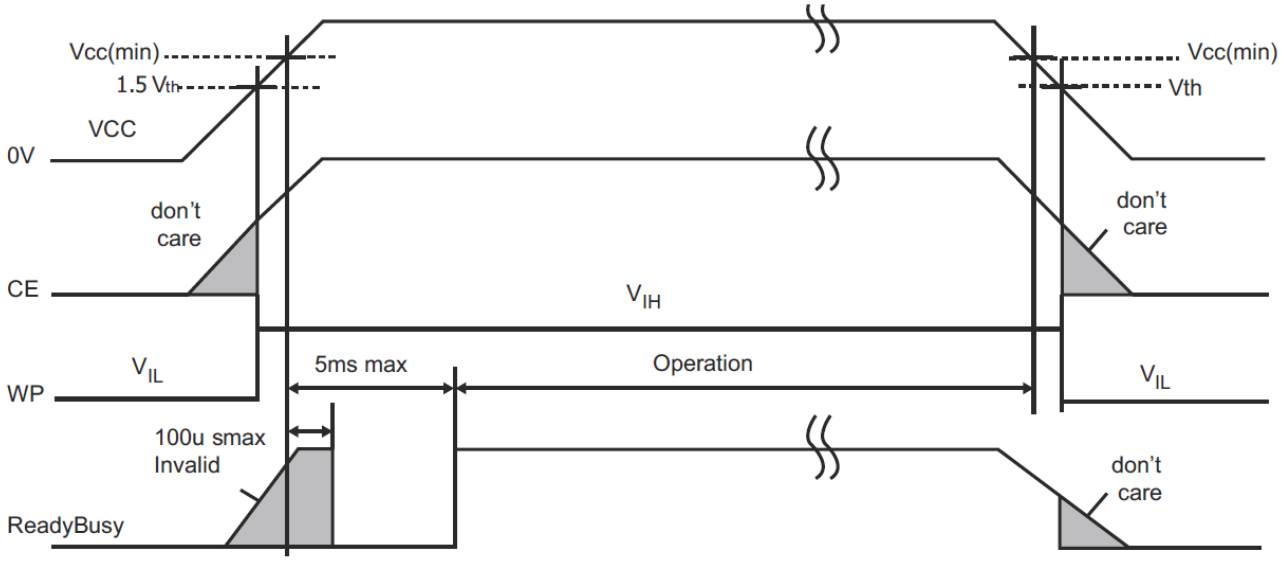


Figure 8-1 AC Waveforms for Power Transition

NOTE :
1) During the initialization, the device consumes a maximum current of 30mA (ICC1).
2) Once Vcc drops under 1.5V, Vcc is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc power up.

8.2. Mode Selection

Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(4cycles)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(4cycles)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1)]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/VCC[2)]	Stand-by	

NOTE :
1) X can be VIL or VIH.
2) WP should be biased to CMOS high or CMOS low for standby.

8.3. Command Latch Cycle

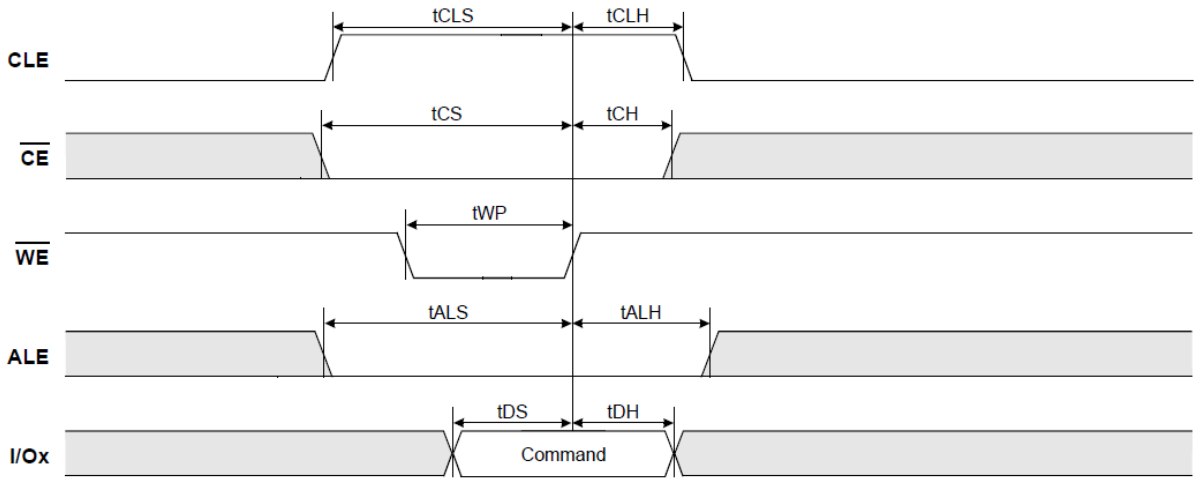


Figure 8−2 Command Latch Cycle

8.4. Address Latch Cycle

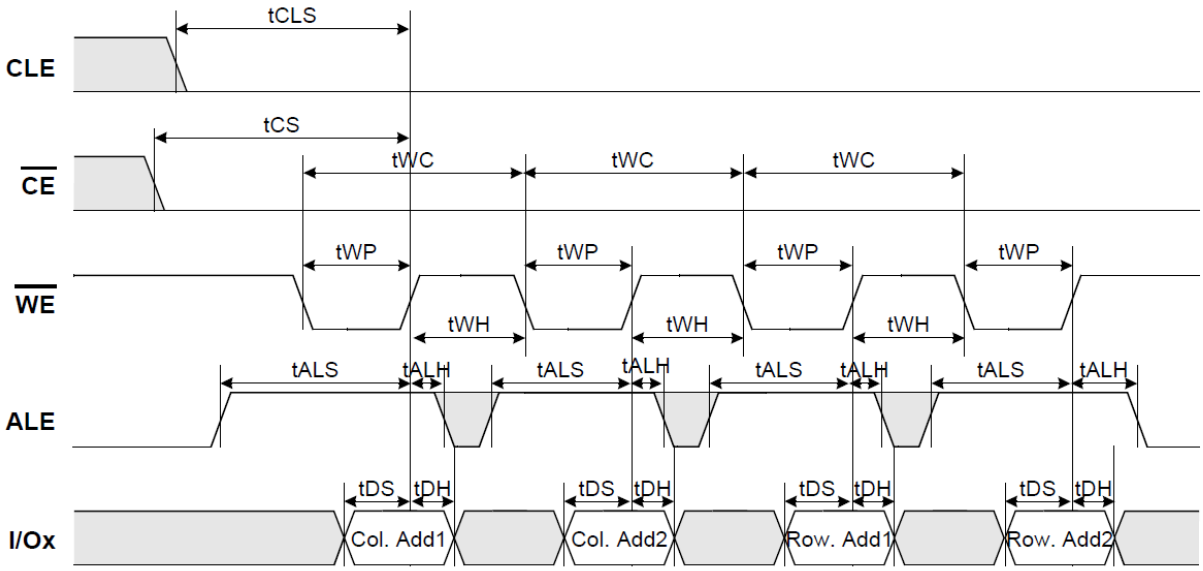


Figure 8-3 Address Latch Cycle

Note:
All command except Reset, Read Status is issued to command register on the rising edge of /WE, when CLE is high,CE# and ALE is low, and device is not busy state.

8.5. Input Data Latch Cycle

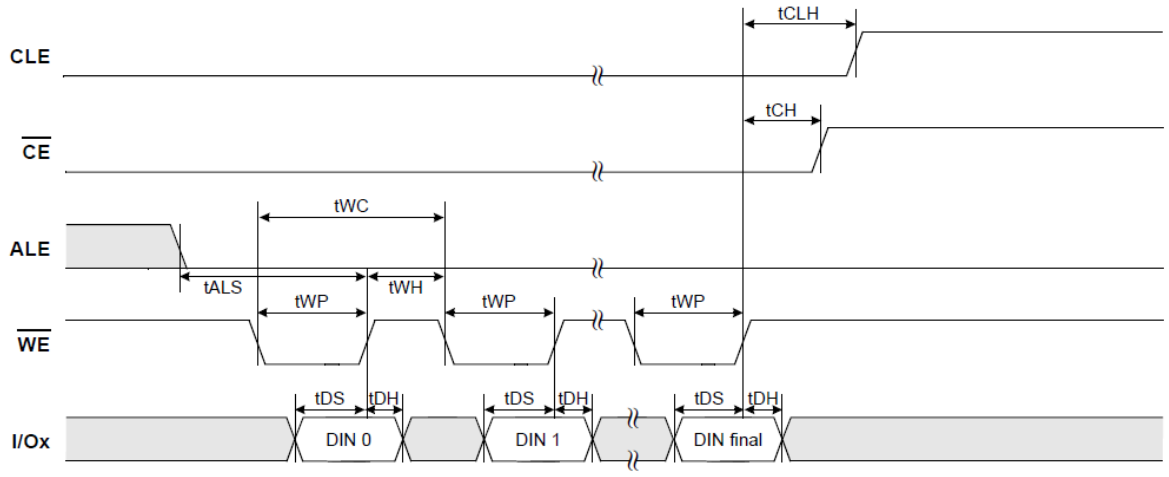


Figure 8-4 Input Data Latch Cycle

Note:
Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

8.6. Data Output Cycle Timings (CLE=L, WE#=H, ALE=L)

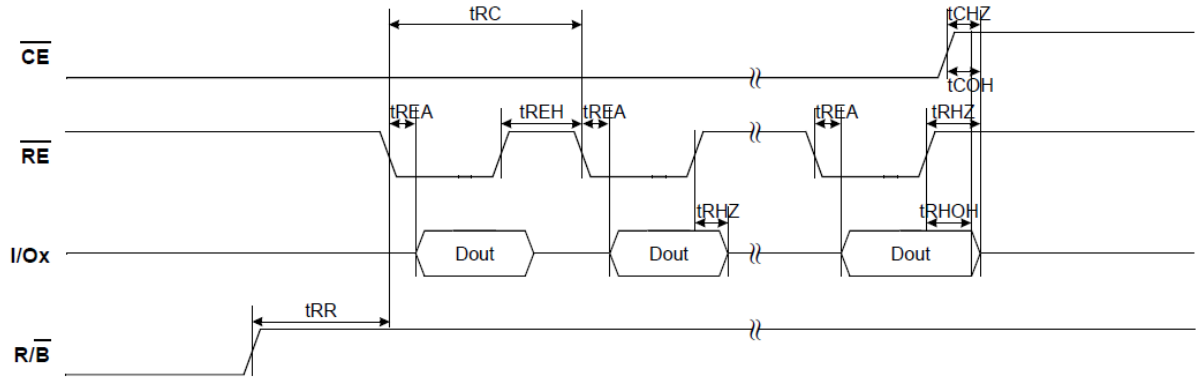


Figure 8-5 Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

NOTE :
1) Transition is measured at 200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
2) tRHOH starts to be valid when frequency is lower than 33Mhz.

9. Package Information

Unit :mm

162 Ball FBGA, 8mm x 10.5mmx1.0mm

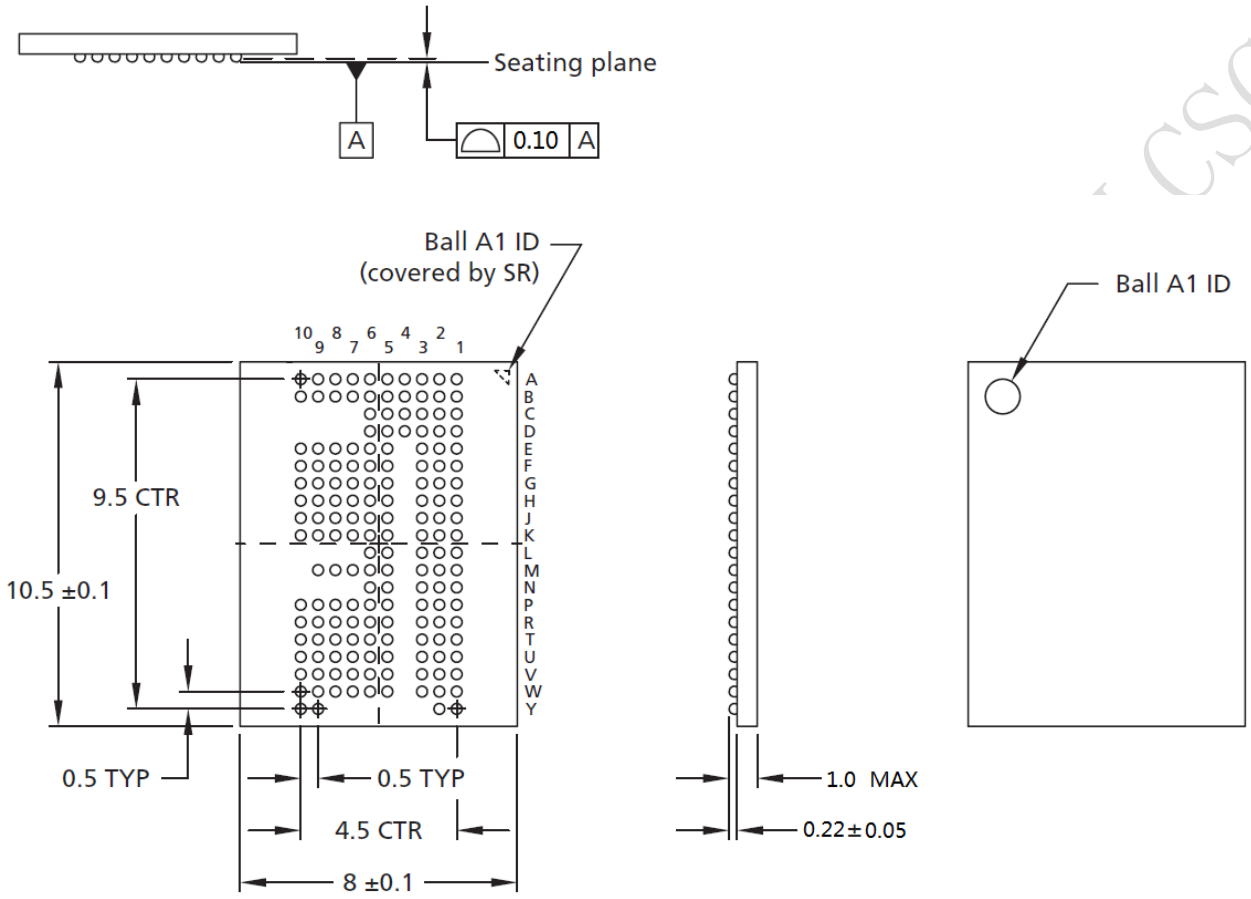


Figure 9-1 162 Ball Grid Array (BGA)