HiMARK
the wireless IC company

FS8108 Low Power Phase-Locked Loop IC

Description

The FS8108 is a serial data input, phase-locked loop IC with programmable input and reference frequency dividers. When combined with a VCO, the FS8108 becomes the core of a very low power frequency synthesizer well-suited for mobile communication applications such as paging systems. The FS8108 includes an 18-bit programmable input frequency divider and also implements a separate pin for stand-by control.

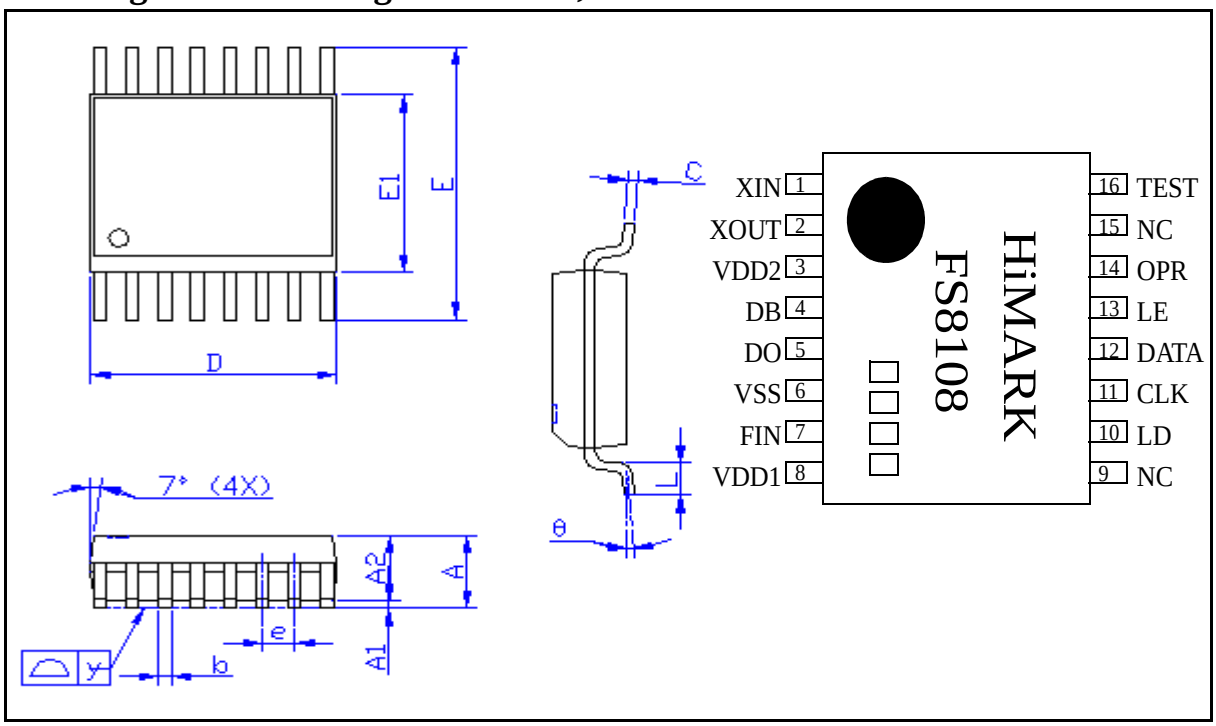
Features

- High maximum input operating frequency — 185 MHz at V_{DD1} = 1.0 V
- Up to 22 MHz internal crystal oscillator reference frequency at V_{DD1} = 1.0 V
- Extremely low current consumption ($I_{DD,total}$ typically 0.4 mA at f_{FIN} = 90 MHz)
- 18-bit programmable input frequency divider (including a ÷ 64/65 prescaler) with divide ratio range from 4032 to 262143
- 13-bit programmable reference frequency divider (including a ÷ 8 prescaler) with divide ratio range from 40 to 65528
- Optional lock detector output
- Charge pump output for passive low-pass filter
- Quick-lock signal output for faster locking
- Separate pin for stand-by control
- TSSOP 16L package (0.65mm pitch)

Applications

- Pager
- Wireless communication system

Package and Pin Assignment: 16L, TSSOP



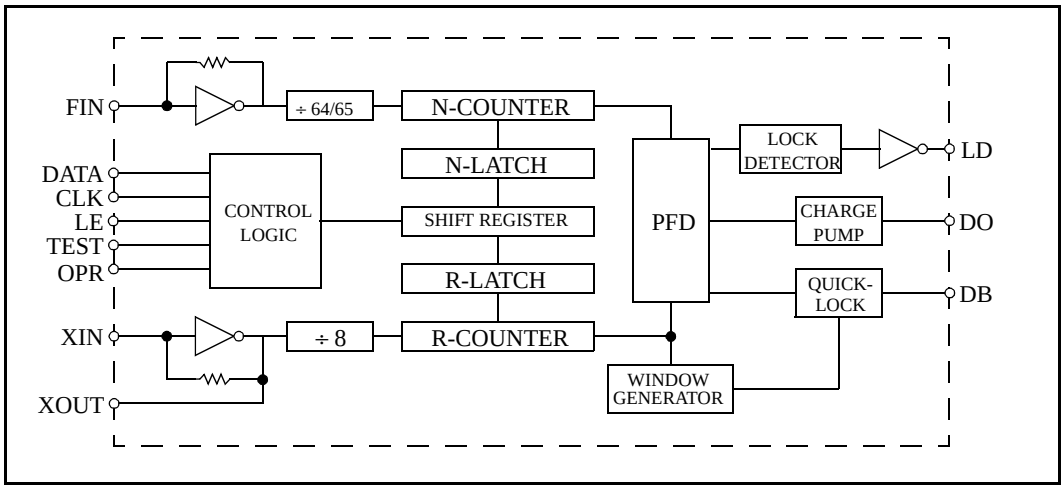
Symbols	Dimensions in mm			Dimensions in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.048
A1	0.05	---	0.15	0.002	---	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	---	0.30	0.007	---	0.012
C	0.09	---	0.20	0.004	---	0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	---	6.40	---	---	0.252	---
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	---	0.65	---	---	0.026	---
L	0.45	0.60	0.75	0.018	0.024	0.030
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

Note: Tolerance ± 0.1mm unless otherwise specified

Pin Descriptions

Number	Name	I/O	Description
1	XIN	I	Reference crystal oscillator or external clock input with internally biased amplifier (any external input to XIN must be ac-coupled)
2	XOUT	O	Reference crystal oscillator or external clock output
3	VDD2	POWER	Nominal 3.0 V supply voltage
4	DB	O	Single-ended quick-lock output for faster locking
5	DO	O	Single-ended charge pump output for passive low pass filter
6	VSS	GND	Ground
7	FIN	I	VCO frequency input with internally biased input amplifier (any external input to FIN must be ac-coupled)
8	VDD1	POWER	Nominal 1.0 V supply voltage
9	NC	NC	No connection
10	LD	O	Lock detector output (high when PLL is locked)
11	CLK	I	Shift register clock input
12	DATA	I	Serial data input
13	LE	I	Latch enable input
14	OPR	I	Battery-save control input; normal operation when high, stand-by mode when low
15	NC	NC	No connection
16	TEST	I	Test mode control input with internal pull-down resistor

Block Diagram



Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD1}	V_{SS} – 0.3 to V_{SS} + 2.0	V
	V_{DD2}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Input voltage range	V_{FIN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	–10 to 60	°C
Storage temperature range	T_{STG}	–40 to 125	°C
Soldering temperature range	T_{SLD}	255	°C
Soldering time range	t_{SLD}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Value			Unit
		min.	typ.	max.	
Supply voltage range	V_{DD1}	0.95	1.0	2.0	V
	V_{DD2}	2.0	3.0	3.3	V
Operating temperature	T_A	–10	25	60	°C

Electrical Characteristics

(V_{DD1} = 0.95 to 2.0 V, V_{DD2} = 2.7 to 3.3 V, V_{SS} = 0 V, T_A = 0 to 60°C unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
Current consumption	$I_{DD,total}$	V_{DD1} = 1.0 V, OPR="H", V_{FIN} = 0.3 V_{pk-pk} sinusoid, f_{FIN} = 100 MHz, V_{XIN} = 0.3 V_{pk-pk} sinusoid, f_{XIN} = 12.8 MHz		0.40	1.10	mA
Standby current consumption (I_{DD2})	$I_{DD,standby}$	V_{DD1} = 0 V, OPR="L"			10	µA
FIN max. operating frequency	$f_{FIN,max}$	V_{FIN} = 0.3 V_{pk-pk} sinusoid	100			MHz
FIN min. operating frequency	$f_{FIN,min}$	V_{FIN} = 0.3 V_{pk-pk} sinusoid			40	MHz
XIN max. operating frequency	$f_{XIN,max}$	V_{XIN} = 0.3 V_{pk-pk} sinusoid	22			MHz
XIN min. operating frequency	$f_{XIN,min}$	V_{XIN} = 0.3 V_{pk-pk} sinusoid			7	MHz
FIN input voltage swing	V_{FIN}		0.3			V_{pk-pk}
XIN input voltage swing	V_{XIN}		0.3			V_{pk-pk}
CLK, DATA, LE logic LOW input voltage	V_{IL}				0.3	V
CLK, DATA, LE logic HIGH input voltage	V_{IH}		V_{DD}-0.3			V
XIN logic LOW input current	$I_{IL,XIN}$	V_{IL} = 0 V			10	µA
XIN logic HIGH input current	$I_{IH,XIN}$	V_{IH} = V_{DD1}			10	µA
FIN logic LOW input current	$I_{IL,FIN}$	V_{IL} = 0 V			60	µA
FIN logic HIGH input current	$I_{IH,FIN}$	V_{IH} = V_{DD1}			60	µA
DO logic LOW output current	$I_{OL,DOP}$	V_{OL} = 0.4 V	1.0			mA
DO logic HIGH output current	$I_{OH,DOP}$	V_{OH} = V_{DD2} – 0.4 V	1.0			mA
LD, FV, FR logic LOW output current	I_{OL}	V_{OL} = 0.4 V	0.1			mA
LD, FV, FR logic HIGH output current	I_{OH}	V_{OH} = V_{DD2} – 0.4 V	0.1			mA
DATA to CLK setup time	t_{SU1}		2			µs
CLK to LE setup time	t_{SU2}		2			µs
Hold time	t_{HOLD}		2			µs

Functional Description

Programmable Input Frequency Divider

The VCO input to the FIN pin is divided by the programmable divider and then internally output to the phase/frequency detector (PFD) as f_V. The programmable input frequency divider consists of a ÷ 64/65 (P/P+1) dual-modulus prescaler and a 18-bit (N) counter, which is further comprised of a 6-bit swallow (A) counter, and a 12-bit main (B) counter. The total divide ratio, M, is related to values for P, A, and B through the relation

$$M = (P + 1) \times A + P \times (B - A) = P \times B + A,$$

with $B \geq A$. The minimum programmable divisor for continuous counting is given by $P \times (P - 1) = 64 \times 63 = 4032$, and the valid total divide ratio range for the input divider is $M = 4032$ to 262143.

Programmable Reference Frequency Divider

The crystal oscillator output is divided by the programmable divider and then internally output to the PFD as f_R. The programmable reference frequency divider consists of a fixed ÷ 8 (S) prescaler and a 13-bit reference (R) counter. The total divide ratio, T, is related to values for S and R through the relation

$$T = S \times R = 8 \times R.$$

The usable divisior range of the reference counter is $R = 5$ to 8191, and therefore, the valid total divide ratio range for the reference divider is $T = 40$ to 65528 (in steps of 8.)

Serial Input Data Format

The divide ratios for the input and reference dividers are input using a 19-bit serial interface consisting of separate clock (CLK), data (DATA), and latch enable (LE) lines. The format of the serial data is shown in Fig. 1. The data on the DATA line is written to the shift register on the rising edge of the CLK signal and is input with MSB first, and the last bit is used as the latch select control bit. The data on the DATA line should be changed on the falling edge of CLK, and LE should be held low while data is being written to the shift register. Data is transferred from the shift register to one of the frequency divider latches when LE is set high. When the latch select control bit is set low, data is loaded to the 18-bit N-counter latch, and when the latch select control bit is set high, the 2 MSBs are

ignored, the next 13 data bits are loaded to the 13-bit *R*-counter latch and the remaining 3 LSBs are used to control testing modes and should be set as follows for normal operation: R14 = high, R15 = low, R16 = low. To disable LD output (*i.e.* set LD low), R14 should be set low.

Serial input data timing waveforms are shown in Fig. 2.

Fig. 1 – Serial input data format

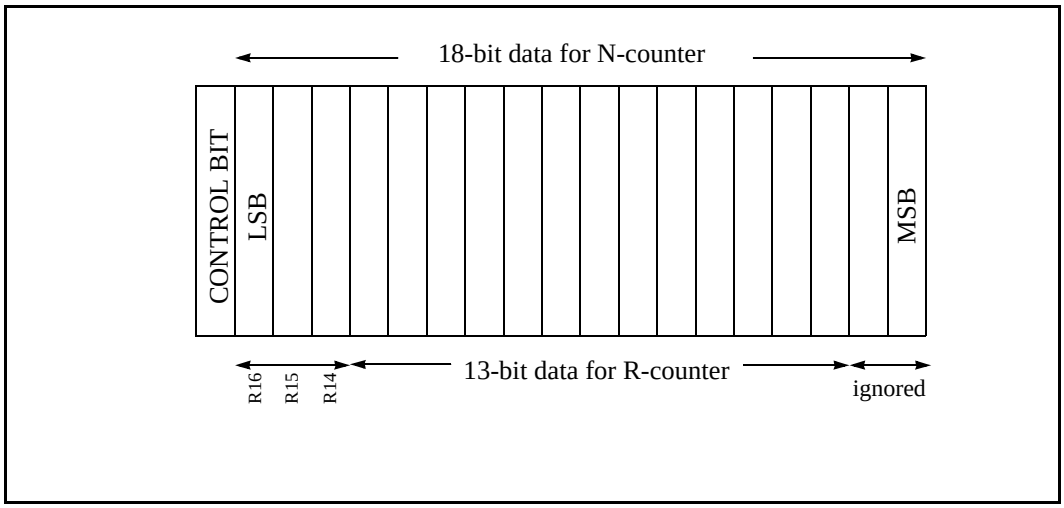
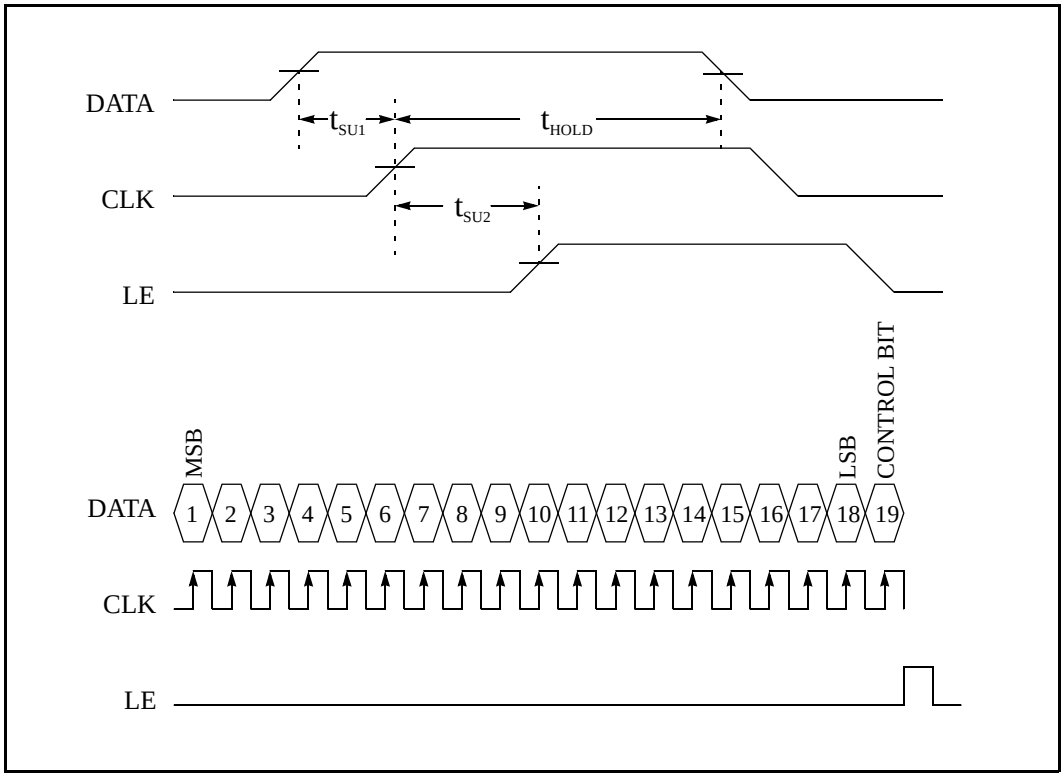


Fig. 2 – Serial input data timing waveforms



Phase/Frequency Detector (PFD)

The PFD compares an internal input frequency divider output signal, f_V, with an internal reference frequency divider output signal, f_R, and generates an error signal, DO, which is proportional to the phase error between f_V and f_R. The DO output is intended for use with a passive filter as shown in Fig. 3.

The input/output waveforms for the PFD are shown in Fig. 4.

Fig. 3 – Passive low-pass filter circuit

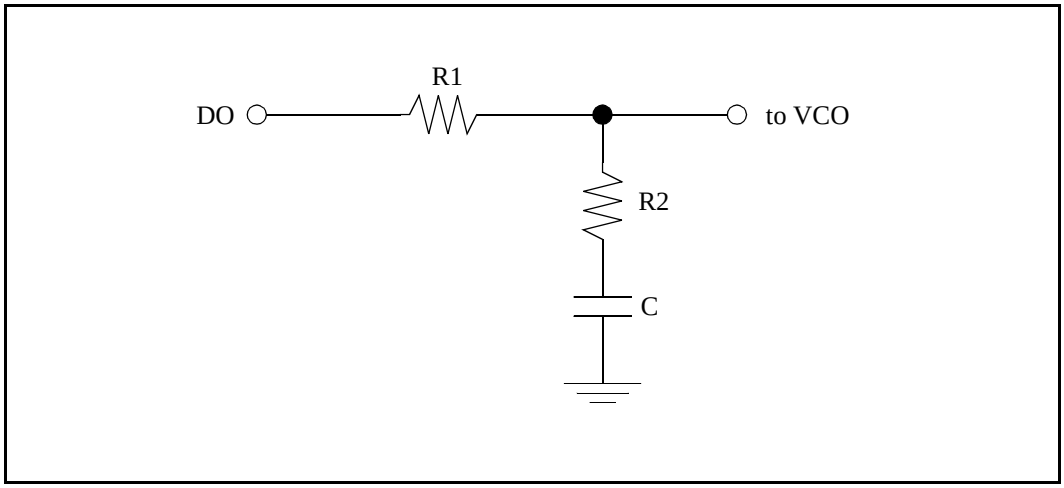
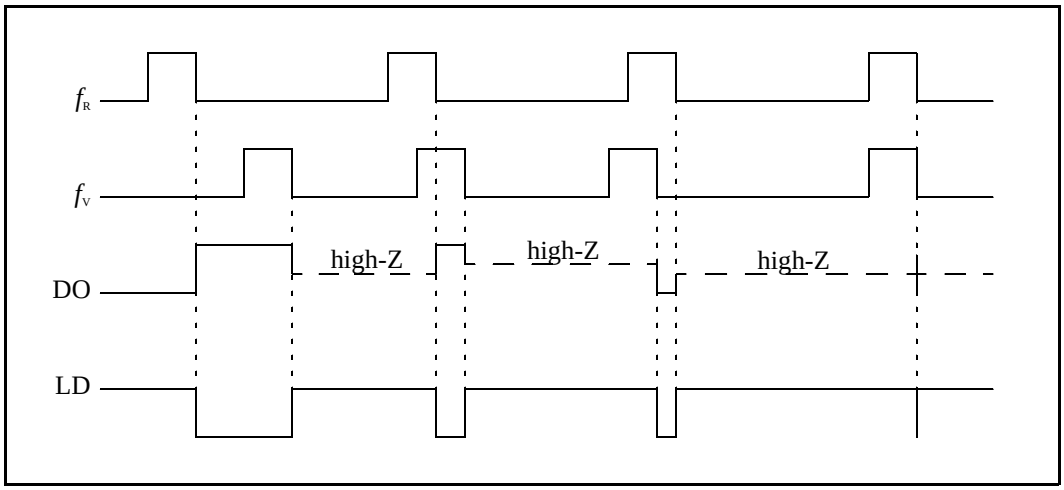


Fig. 4 – PFD input/output waveforms



Quick-lock Signal (DB)

The quick-lock output signal, DB, is provided so that the PLL may achieve higher speed locking. When connected, the DB output effectively doubles the charge pump current output to the loop filter during the initial start-up of the PLL (when OPR first goes high). Once the PLL phase error is within a specific tolerance, the quick-lock circuitry sets the DB output to a high impedance state and the PLL continues toward lock with its normal charge pump current.

Stand-by Mode

The stand-by mode for the PLL is entered by setting the OPR pin low and V_{DD1} to 0 V while the circuit is in operation. In the stand-by mode, the XIN and FIN amplifiers, *N*-counter, and *R*-counter are stopped, the *N*- and *R*-counters are also reset, and the DO and DB outputs are set to the high impedance state. As long as voltage is supplied to V_{DD2}, data loaded to the latches is kept. To exit from stand-by mode to normal operation, the OPR pin must be set high and voltage must again be supplied to V_{DD1}.

Application Circuit