



January 2000  
Revised June 2003

## NC7SB3157 • FSA3157

### TinyLogic® Low Voltage UHS SPDT Analog Switch or 2:1 Multiplexer/Demultiplexer Bus Switch

#### General Description

The NC7SB3157 or FSA3157 is a high performance, single-pole/double-throw (SPDT) Analog Switch or 2:1 Multiplexer/Demultiplexer Bus Switch from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance. The break before make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V  $V_{CC}$  operating range. The control input tolerates voltages up to 5.5V independent of the  $V_{CC}$  operating range.

#### Features

- Useful in both analog and digital applications
- Space saving SC70 6-lead surface mount package
- Ultra small MicroPak™ leadless package
- Low On Resistance; < 10Ω on typ @ 3.3V  $V_{CC}$
- Broad  $V_{CC}$  operating range; 1.65V to 5.5V
- Rail-to-Rail signal handling
- Power down high impedance control input
- Overvoltage tolerance of control input to 7.0V
- Break before make enable circuitry
- 250 MHz - 3dB bandwidth

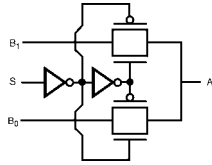
#### Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SB3157P6X	MAA06A	B7A	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SB3157L6X	MAC06A	BB	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel
FSA3157P6X	MAA06A	B7A	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
FSA3157L6X	MAC06A	BB	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

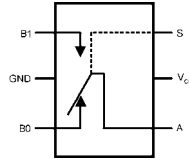
TinyLogic® is a registered trademark and MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

NC7SB3157 • FSA3157 TinyLogic® Low Voltage UHS SPDT Analog Switch or 2:1 Multiplexer/Demultiplexer Bus Switch

### Logic Symbol



### Analog Symbol



### Function Table

Input (S)	Function
L	B <sub>0</sub> Connected to A
H	B <sub>1</sub> Connected to A

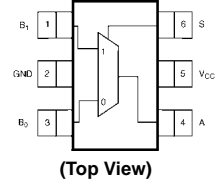
H = HIGH Logic Level      L = LOW Logic Level

### Pin Descriptions

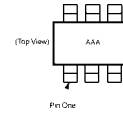
Pin Names	Description
A, B <sub>0</sub> , B <sub>1</sub>	Data Ports
S	Control Input

### Connection Diagrams

#### Pin Assignments for SC70



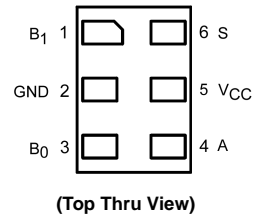
#### Pin One Orientation Diagram



AAA = Product Code Top Mark - see ordering code.

**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

#### Pad Assignments for MicroPak



### Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ ) (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) @ ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA
DC Output Current ( $I_{OUT}$ )	128 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}/I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature under Bias ( $T_J$ )	150°C
Junction Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C
Power Dissipation ( $P_D$ ) @ +85°C	180 mW

### Recommended Operating Conditions (Note 3)

Supply Voltage Operating ( $V_{CC}$ )	1.65V to 5.5V
Control Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$
Switch Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
Control Input $V_{CC} = 2.3V - 3.6V$	0 ns/V to 10 ns/V
Control Input $V_{CC} = 4.5V - 5.5V$	0 ns/V to 5 ns/V
Thermal Resistance ( $\theta_{JA}$ )	350°C/W

**Note 1:** Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 3:** Control input must be held HIGH or LOW, it must not float.

### DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	1.65 - 1.95 2.3 - 5.5	0.75 $V_{CC}$ 0.7 $V_{CC}$			0.75 $V_{CC}$ 0.7 $V_{CC}$		V	
$V_{IL}$	LOW Level Input Voltage	1.65 - 1.95 2.3 - 5.5		0.25 $V_{CC}$ 0.3 $V_{CC}$		0.25 $V_{CC}$ 0.3 $V_{CC}$		V	
$I_{IN}$	Input Leakage Current	0 - 5.5		$\pm 0.05$ $\pm 0.1$		$\pm 1$		$\mu A$	$0 \leq V_{IN} \leq 5.5V$
$I_{OFF}$	OFF State Leakage Current	1.65 - 5.5		$\pm 0.05$ $\pm 0.1$		$\pm 1$		$\mu A$	$0 \leq A, B \leq V_{CC}$
$R_{ON}$	Switch On Resistance (Note 4)	4.5		3	7		7	$\Omega$	$V_{IN} = 0V, I_O = 30$ mA
				5	12		12	$\Omega$	$V_{IN} = 2.4V, I_O = -30$ mA
				7	15		15	$\Omega$	$V_{IN} = 4.5V, I_O = -30$ mA
		3.0		4	9		9	$\Omega$	$V_{IN} = 0V, I_O = 24$ mA
				10	20		20	$\Omega$	$V_{IN} = 3V, I_O = -24$ mA
				5	12		12	$\Omega$	$V_{IN} = 0V, I_O = 8$ mA
		1.65		13	30		30	$\Omega$	$V_{IN} = 2.3V, I_O = -8$ mA
				6.5	20		20	$\Omega$	$V_{IN} = 0V, I_O = 4$ mA
			17	50		50	$\Omega$	$V_{IN} = 1.65V, I_O = -4$ mA	
$I_{CC}$	Quiescent Supply Current All Channels ON or OFF	5.5		1		10		$\mu A$	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$
	Analog Signal Range	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$		V	
$R_{RANGE}$	On Resistance	4.5				25		$\Omega$	$I_A = -30$ mA, $0 \leq V_{Bn} \leq V_{CC}$
	Over Signal Range (Note 4)(Note 8)	3.0				50		$\Omega$	$I_A = -24$ mA, $0 \leq V_{Bn} \leq V_{CC}$
		2.3				100		$\Omega$	$I_A = -8$ mA, $0 \leq V_{Bn} \leq V_{CC}$
		1.65				300		$\Omega$	$I_A = -4$ mA, $0 \leq V_{Bn} \leq V_{CC}$
$\Delta R_{ON}$	On Resistance Match Between Channels (Note 4)(Note 5)(Note 6)	4.5		0.15				$\Omega$	$I_A = -30$ mA, $V_{Bn} = 3.15$
		3.0		0.2				$\Omega$	$I_A = -24$ mA, $V_{Bn} = 2.1$
		2.3		0.5				$\Omega$	$I_A = -8$ mA, $V_{Bn} = 1.6$
		1.65		0.5				$\Omega$	$I_A = -4$ mA, $V_{Bn} = 1.15$

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
R <sub>flat</sub>	On Resistance Flatness (Note 4)(Note 5)(Note 7)	5.0	6					Ω	I <sub>A</sub> = -30 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>
		3.3	12						I <sub>A</sub> = -24 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>
		2.5	28						I <sub>A</sub> = -8 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>
		1.8	125						I <sub>A</sub> = -4 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>

**Note 4:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

**Note 5:** Parameter is characterized but not tested in production.

**Note 6:** ΔR<sub>ON</sub> = R<sub>ON</sub> max – R<sub>ON</sub> min measured at identical V<sub>CC</sub>, temperature and voltage levels.

**Note 7:** Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

**Note 8:** Guaranteed by Design.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t <sub>PHL</sub>	Propagation Delay	1.65 – 1.95			3.5			ns	V <sub>I</sub> = OPEN	Figures 1, 2
t <sub>PLH</sub>	Bus to Bus (Note 10)	2.3 – 2.7			1.2		1.2			
		3.0 – 3.6			0.8		0.8			
		4.5 – 5.5			0.3		0.3			
t <sub>PZL</sub>	Output Enable Time	1.65 – 1.95	7		23	7	24	ns	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PZL</sub> V <sub>I</sub> = 0V for t <sub>PZH</sub>	Figures 1, 2
t <sub>PZH</sub>	Turn on Time (A to B <sub>n</sub> )	2.3 – 2.7	3.5		13	3.5	14			
		3.0 – 3.6	2.5		6.9	2.5	7.6			
		4.5 – 5.5	1.7		5.2	1.7	5.7			
t <sub>PLZ</sub>	Output Disable Time	1.65 – 1.95	3		12.5	3	13	ns	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>I</sub> = 0V for t <sub>PHZ</sub>	Figures 1, 2
t <sub>PHZ</sub>	Turn Off Time (A Port to B Port)	2.3 – 2.7	2		7	2	7.5			
		3.0 – 3.6	1.5		5	1.5	5.3			
		4.5 – 5.5	0.8		3.5	0.8	3.8			
t <sub>B-M</sub>	Break Before Make Time (Note 9)	1.65 – 1.95	0.5			0.5		ns		Figure 3
		2.3 – 2.7	0.5			0.5				
		3.0 – 3.6	0.5			0.5				
		4.5 – 5.5	0.5			0.5				
Q	Charge Injection (Note 9)	5.0		7				pC	C <sub>L</sub> = 0.1 nF, V <sub>GEN</sub> = 0V R <sub>GEN</sub> = 0Ω	Figure 4
		3.3		3						
OIRR	Off Isolation (Note 11)	1.65 – 5.5		-57				dB	R <sub>L</sub> = 50Ω f = 10MHz	Figure 5
Xtalk	Crosstalk	1.65 – 5.5		-54				dB	R <sub>L</sub> = 50Ω f = 10MHz	Figure 6
BW	-3dB Bandwidth	1.65 – 5.5		250				MHz	R <sub>L</sub> = 50Ω	Figure 9
THD	Total Harmonic Distortion (Note 9)	5		.011				%	R <sub>L</sub> = 600Ω 0.5 V <sub>P-P</sub> f = 600 Hz to 20 KHz	

**Note 9:** Guaranteed by Design.

**Note 10:** This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

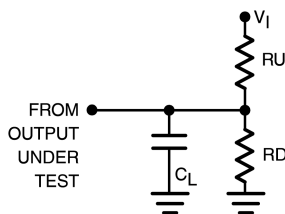
**Note 11:** Off Isolation = 20 log<sub>10</sub> [V<sub>A</sub> / V<sub>Bn</sub>]

## Capacitance (Note 12)

Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
$C_{IN}$	Control Pin Input Capacitance	2.3		pF	$V_{CC} = 0V$	
$C_{IO-B}$	B Port Off Capacitance	6.5		pF	$V_{CC} = 5.0V$	Figure 7
$C_{IOA-ON}$	A Port Capacitance When Switch Is Enabled	18.5		pF	$V_{CC} = 5.0V$	Figure 8

**Note 12:**  $T_A = +25^\circ C$ ,  $f = 1$  MHz, Capacitance is characterized but not tested in production.

## AC Loading and Waveforms

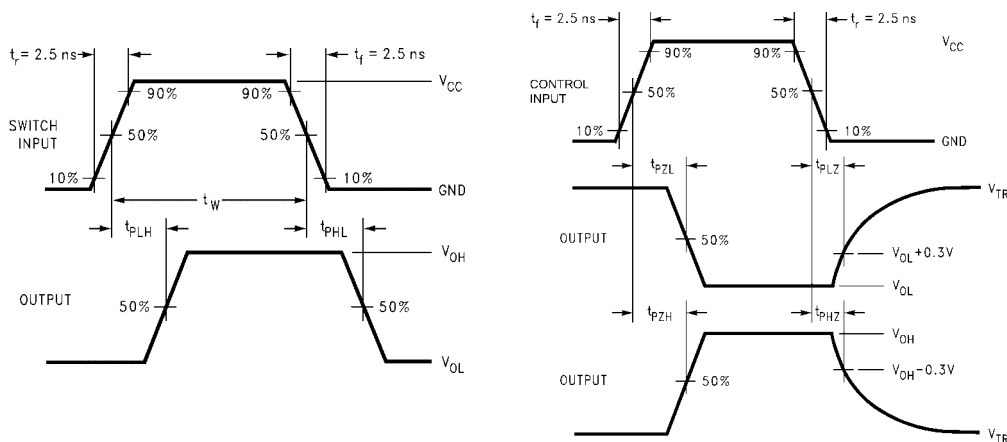


**Note:** Input driven by  $50\Omega$  source terminated in  $50\Omega$

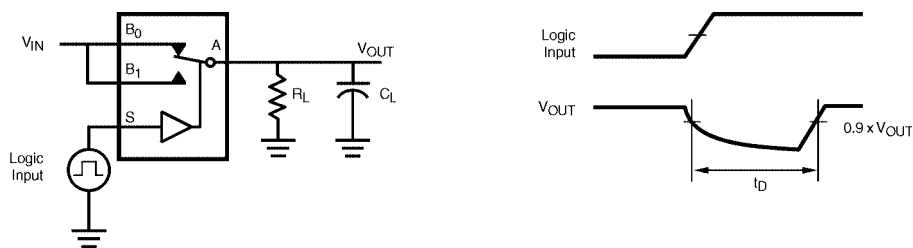
**Note:**  $C_L$  includes load and stray capacitance

**Note:** Input PRR = 1.0 MHz;  $t_W = 500$  ns

**FIGURE 1. AC Test Circuit**



**FIGURE 2. AC Waveforms**



**FIGURE 3. Break Before Make Interval Timing**

AC Loading and Waveforms (Continued)

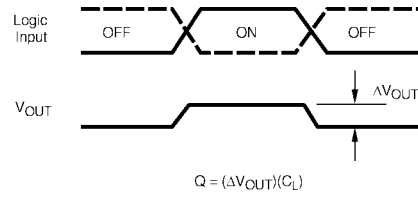
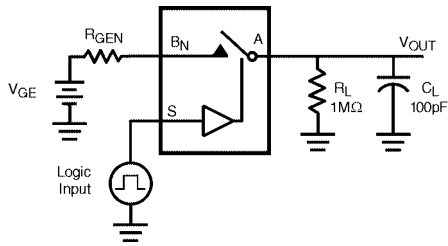


FIGURE 4. Charge Injection Test

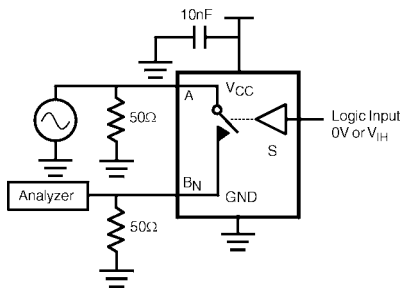


FIGURE 5. Off Isolation

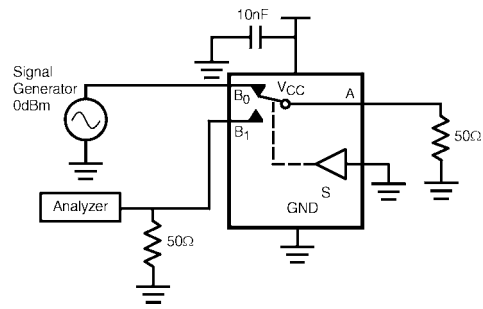


FIGURE 6. Crosstalk

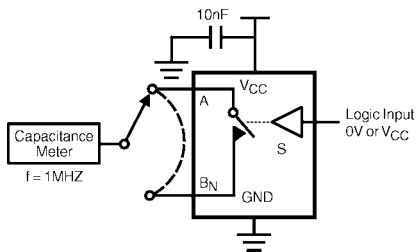


FIGURE 7. Channel Off Capacitance

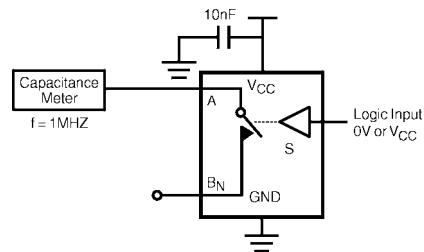


FIGURE 8. Channel On Capacitance

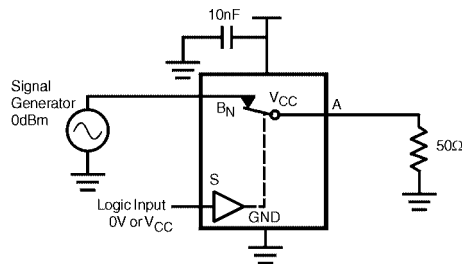


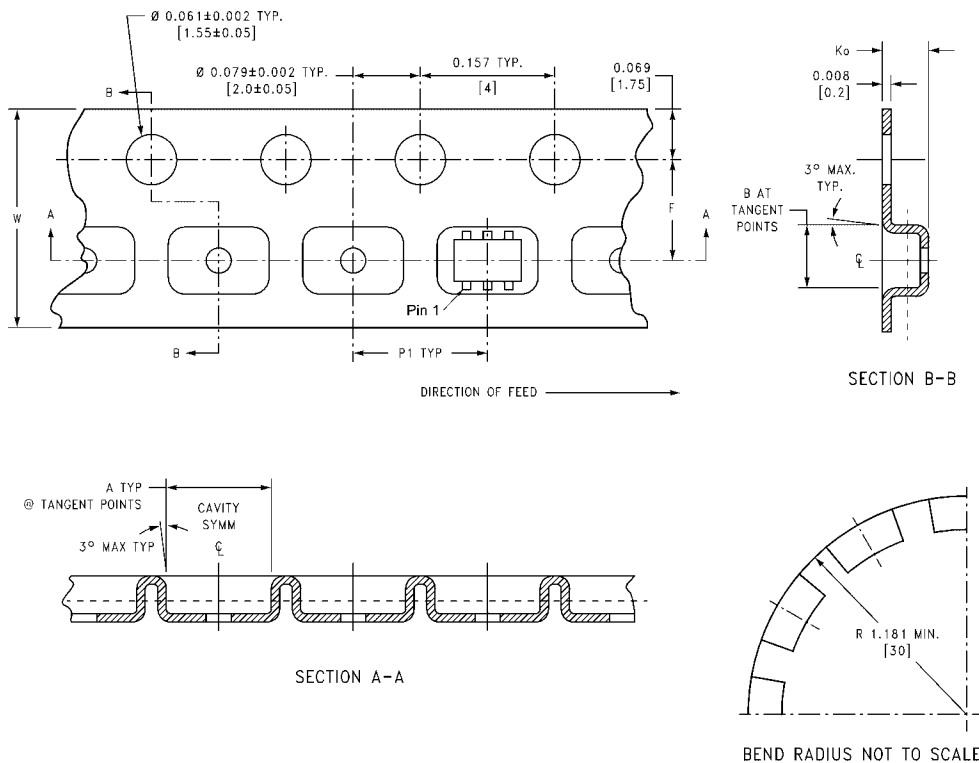
FIGURE 9. Bandwidth

## Tape and Reel Specification

### TAPE FORMAT for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### TAPE DIMENSIONS inches (millimeters)

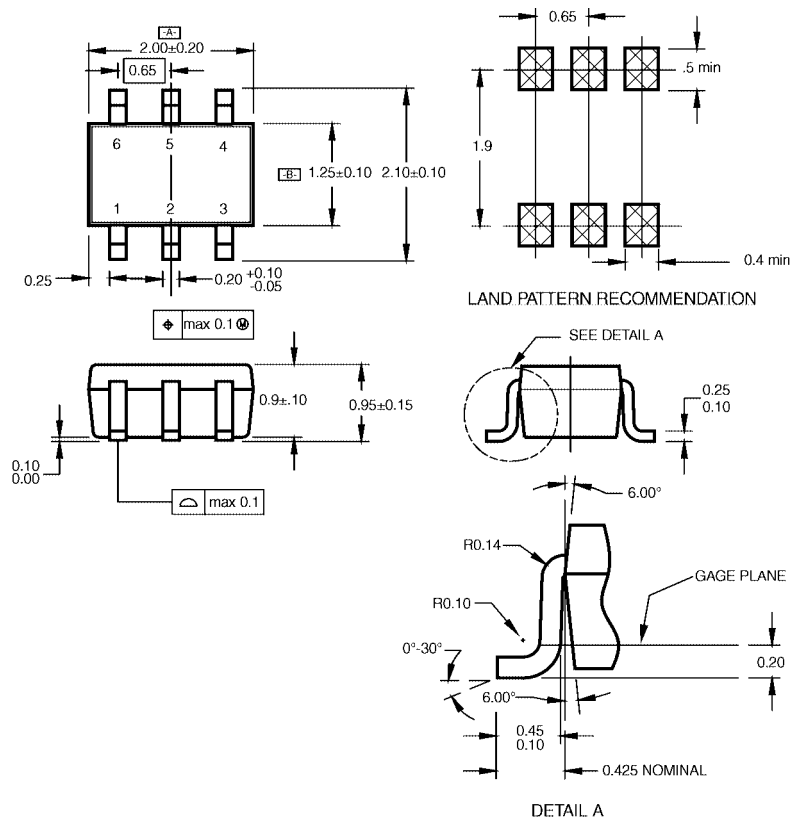


Package	Tape Size	DIM A	DIM B	DIM F	DIM K <sub>o</sub>	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)





**Physical Dimensions** inches (millimeters) unless otherwise noted



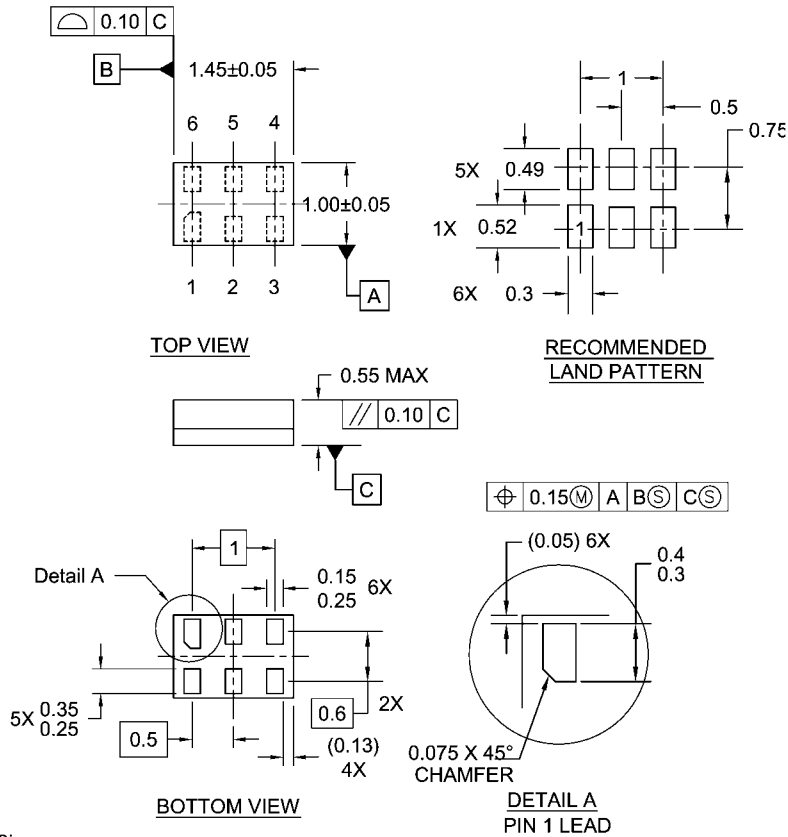
NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

**6-Lead SC70, EIAJ SC88, 1.25mm Wide  
Package Number MAA06A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**Notes:**

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**6-Lead MicroPak, 1.0mm Wide  
Package Number MAC06A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)