FAIRCHILD SEMICONDUCTOR®

September 2010

FSAV330 — 4-Channel, 2:1 Video Switch

Features

- Replacement for the P15V330
- Wide Bandwidth: 300MHz
- 4Ω Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low I_{CC}
- Zero Bounce in Flow-through Mode
- Control Inputs Compatible with TTL Level

Applications

- Set-Top Boxes
- Flat Panel Displays
- CRT Displays
- DVD - RW

Description

The FSAV330 video switch is a quad, single-pole / double-throw, high-speed CMOS TTL-compatible video switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When /OE is LOW, the select pin connects the A port to the selected B port output. When /OE is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FSAV330MX	-40 to +85°C	16-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 inch Narrow	Tape and Reel
FSAV330MTCX	-40 to +85°C	16-, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel
FSAV330QSCX	-40 to +85°C	16-Lead, Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 inch Wide	Tape and Reel

The Fairchild switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

Pin Configurations

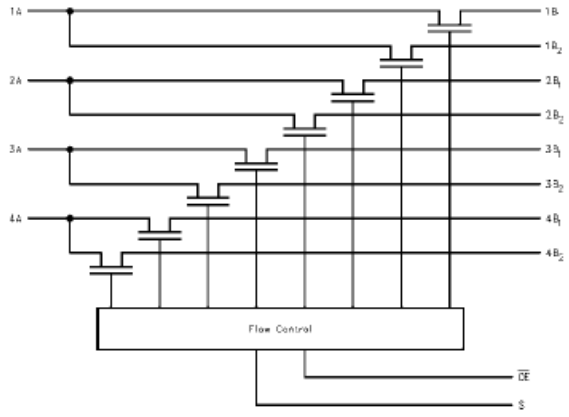


Figure 1. Logic Diagram

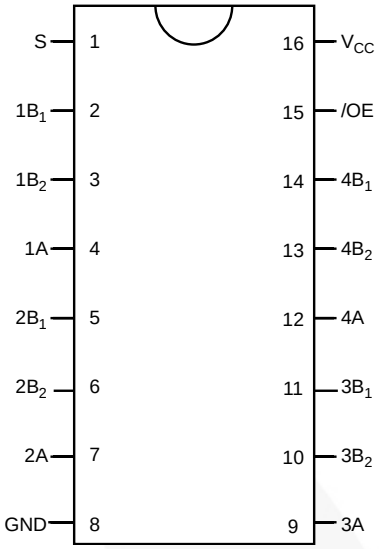


Figure 2. Pin Assignments

Pin Descriptions

Pin #	Name	Description
15	/OE	Bus Switch Enabled
1	S	Select Input
4,7,9,12	A	Bus A
2,3,5,6,10,11,13,14	B_1-B_2	Bus B
8	GND	Ground
16	V_{CC}	Supply Voltage

Truth Table

S	/OE	Function
Don't Care	HIGH	Disconnected
LOW	LOW	A=B_1
HIGH	LOW	A=B_2

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+7.0	V
V_S	DC Switch Voltage	-0.5	+7.0	V
V_{IN}	DC Input Voltage[1]	-0.5	+7.0	V
I_{IK}	DC Input Diode Current	-50		mA
I_{OUT}	DC Output Sink Current		128	mA
I_{CC}/I_{GND}	DC V_{CC} / GND Current		±100	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
ESD	Human Body Model, JESD22-A114		4000	V

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Power Supply		4.0	5.5	V
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
t_r, t_f	Input Rise and Fall Time	Switch Control Input	0	5	ns/V
		Switch I/O	0	DC	
T_A	Operating Temperature, Free Air		-40	+85	°C

Note:

2. Unused control inputs must be held HIGH or LOW; they may not float.

DC Electrical Characteristics

Typical values are at V_{CC}=5.0V and T_A= +25°C. Minimum and maximum values are at T_A= -40 to +85°C.

Symbol	Parameter	Conditions	V_{CC} (V)	Min.	Typ.	Max.	Units
V_{ANALOG}	Analog Signal Range		5.0	0		2	V
V_{IK}	Clamp Diode Voltage	I_{IN}=-18mA	4.5			-1.2	V
V_{IH}	High-Level Input Voltage		4.0 to 5.5	2.0			V
V_{IL}	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I_I	Input Leakage Current	$0 \le V_{IN} \le 5.5V$	5.5			±1.0	µA
I_{OZ}	Off-State Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	µA
R_{ON}	Switch On Resistance[3]	V_{IN}=1.0V, R_I=75Ω, I_{ON}=13mA	4.5		3	7	Ω
		V_{IN}=2.0V, R_I=75Ω, I_{ON}=26mA	4.5		7	10	
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND, I_{OUT}=0	5.5			3	µA
ΔI_{CC}	Increase in I_{CC} per Input	One Input at 3.4V Other Inputs at V_{CC} or GND	5.5			2.5	mA

Note:

3. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the A or B pins.

AC Electrical Characteristics

T_A=-40 to +85°C, C_L=50pF, $R_U=R_D$=500Ω.

Symbol	Parameter	Conditions	V_{CC}=4.5 – 5.5V			V_{CC}=4.0V		Units	Figure
			Min.	Typ.	Max.	Min.	Max.		
t_{PZH}, t_{PZL}	Output Enable Time, Select to Bus B	V_I=7V for t_{PZL} V_I=Open for t_{PZH}			5.2		5.7	ns	Figure 3 Figure 4
	Output Enable Time, /OE to Bus A, B				5.1		5.6		
t_{PHZ}, t_{PLZ}	Output Disable Time, Select to Bus B	V_I=7V for t_{PLZ} V_I=Open for t_{PHZ}			5.2		5.5	ns	Figure 3 Figure 4
	Output Disable Time, Output Enable Time /OE to Bus A, B				5.5		5.5		
B_W	-3dB Bandwidth[4]	R_L=150Ω, T_A=25°C	300					MHz	
X_{TALK}	Crosstalk	R_{IN}=10Ω, R_L=150Ω, f=10MHz		-58				dB	
D_G	Differential Gain	R_L=150Ω, f=3.58MHz		0.64				%	
D_P	Differential Phase	R_L=150Ω, f=3.58MHz		0.1				°	
O_{IRR}	Off Isolation	R_L=150Ω, f=10MHz		-60				dB	

Note:

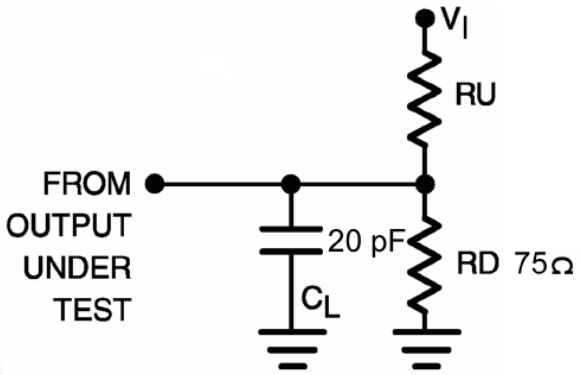
4. This parameter is guaranteed by device characterization, not production tested.

Capacitance

T_A=+25°C, f=1MHz. Capacitance is characterized, not production tested.

Symbol		Parameter	Conditions	Typ.	Units
C_{IN}		Control Pin Input Capacitance	V_{CC}=5.0V	3	pF
$C_{I/O}$	A Port	Input / Output Capacitance	V_{CC}, /OE=5.0V	7	pF
	B Port			5	
C_{ON}		Switch On Capacitance	V_{CC}=5.0V, /OE=0V	12	pF

AC Loadings and Waveforms



Notes:

5. Input drive by 50Ω source terminated in 50Ω.
6. C_L includes load and stray capacitance.
7. Input PRR=1.0MHz, t_W=500ns.

Figure 3. AC Test Circuit

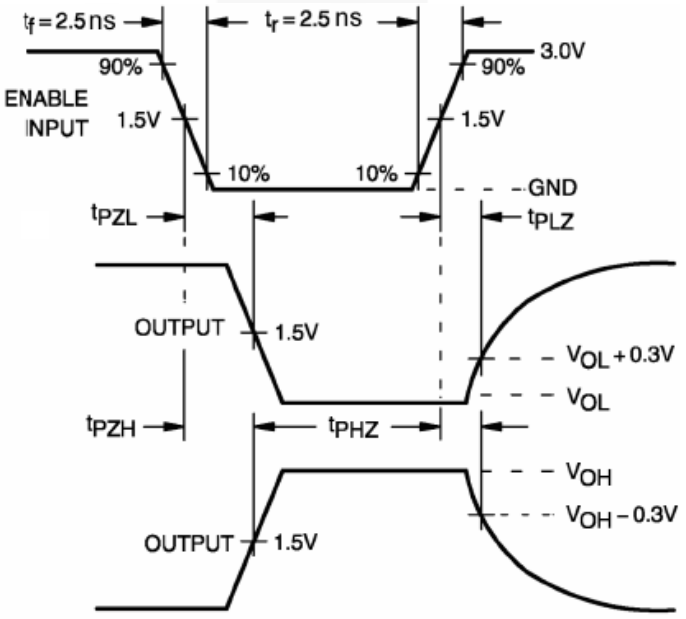


Figure 4. AC Waveforms

Physical Dimensions

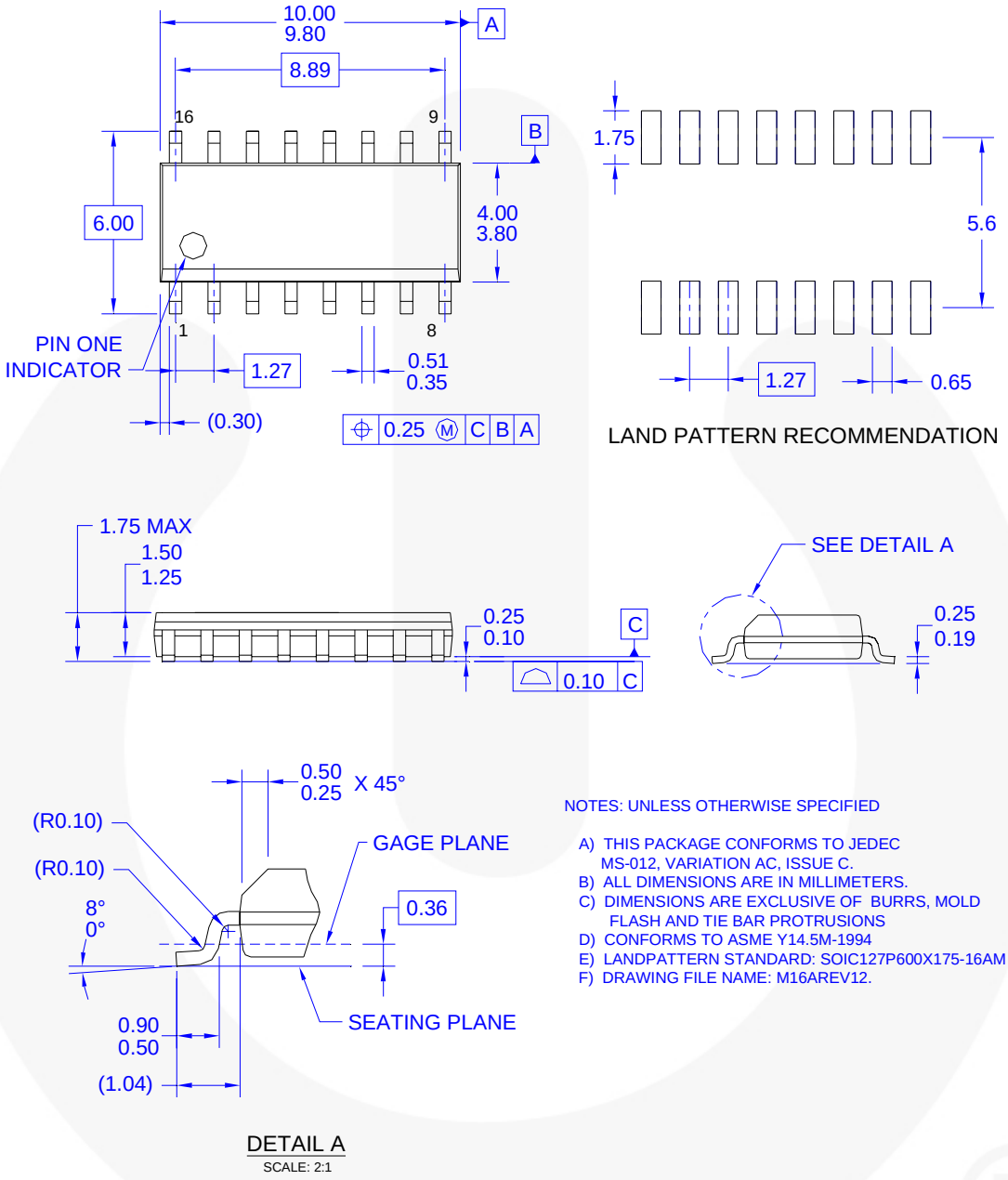


Figure 5. 16-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150-inch Narrow

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Physical Dimensions

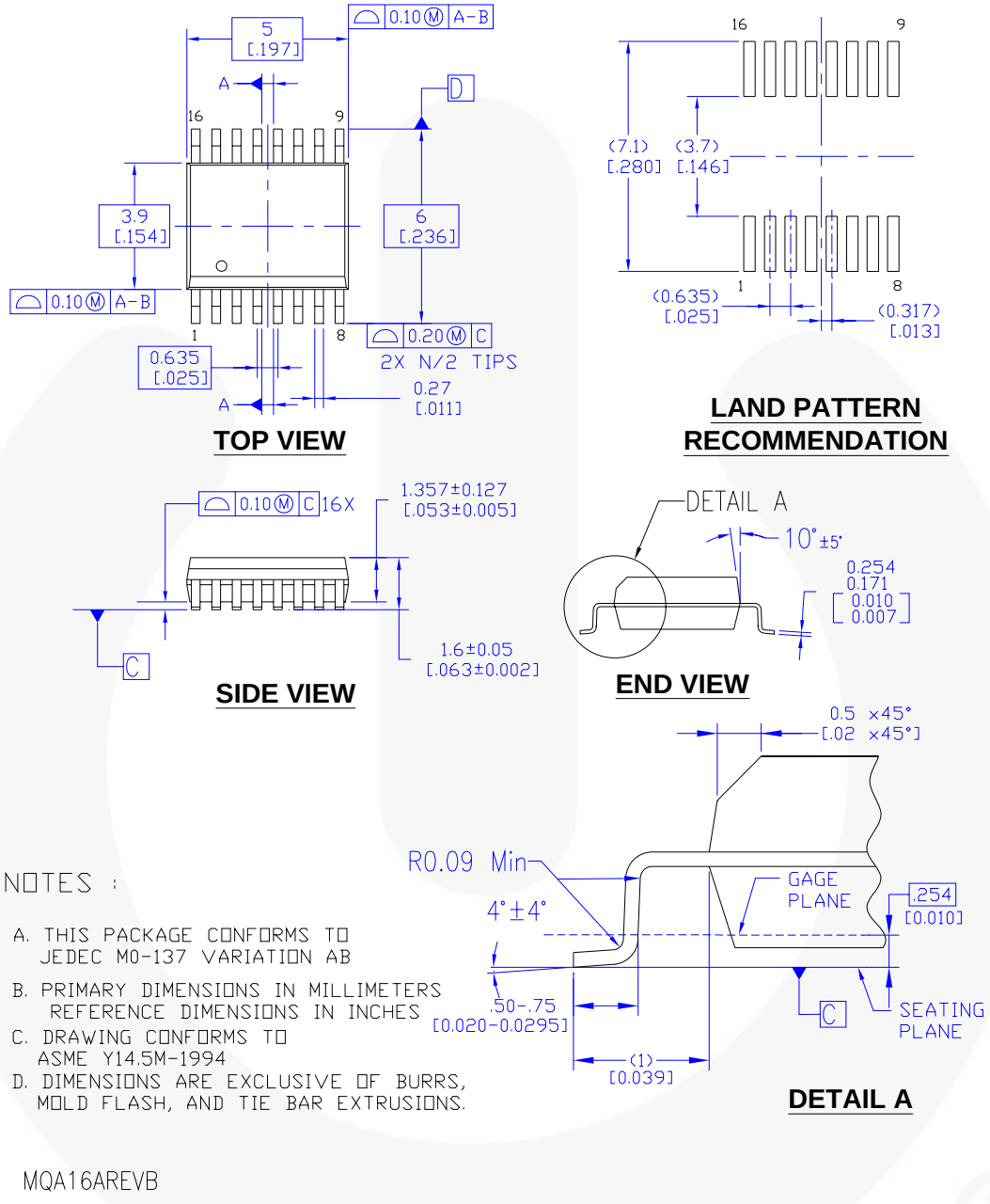

Figure 6. 16-Lead, Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150-inch Wide

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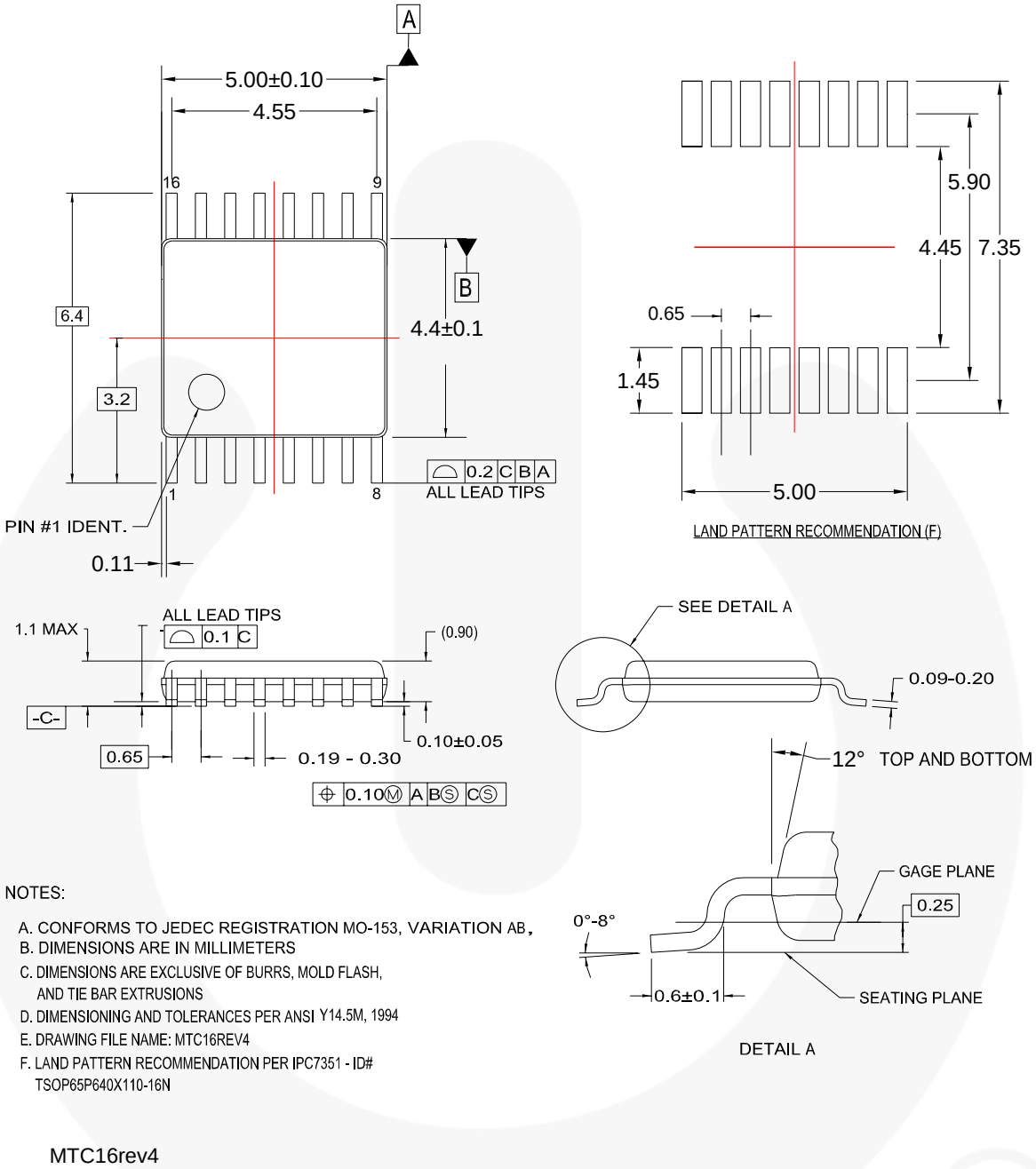

Figure 7. 16-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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