FSC-BW236

Single-Chip Low Power Dual Bands WLAN and Bluetooth Low Energy Module Datasheet

(WLAN 802.11 a/b/g/n , 1T1R & BT5.0)

Version 1.2

Revision History

Version	Data	Notes	
1.0	2019/09/07	Initial Version	Devin Wan
1.1	2019/09/29	Update image: Restricted Area	Devin Wan
1.2	2019/10/10	Update: Module photo, Module pin definition, Application circuit diagram	Devin Wan

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1. INTRODUCTION

Overview

FSC-BW236 is a highly integrated single-chip low power dual bands (2.4GHz and 5GHz) Wireless LAN (WLAN) and Bluetooth Low Energy (v5.0) communication controller. It consists of a high-performance MCU (ARM v8m, Cortex-M4F instruction compatible) named KM4, a low power MCU (v8m, Cortex-M0 instruction compatible) named KM0, WLAN (802.11 a/b/g/n) MAC, an 1T1R capable WLAN baseband, RF, Bluetooth and peripherals.

FSC-BW236 is an appropriate product for designers who want to add wireless capability to their products. Support for external antennas and increase wireless coverage.

Features

- COMS MAC,Baseband PHY,and RF in a single-Chip for 802.11 a/b/g/n compatible WLAN
- Support BLE 5.0
- UART programming and data interface (baudrate can up to 6000000bps)
- I2C/AIO/PIO/PWM control interfaces
- Postage stamp sized form factor
- WiFi Maximum data rate 54Mbps in 802.11g , 150Mbps in 802.11n, 54Mbps in 802.11a
- WiFi : Light Weight TCP/IP protocol
- Support External Antenna-Postage stamp or ipex
- RoHS compliant

Application

- Wireless POS
- Measurement and monitoring systems
- Industrial sensors and controls
- Asset Tracking
- Wireless printer

Module picture as below showing

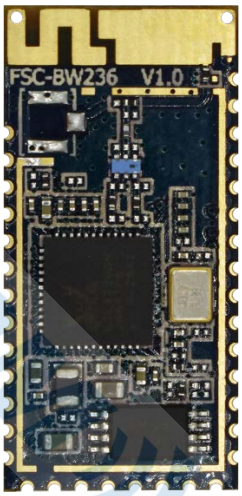


Figure 1: FSC-BW236 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth	Version : V5.0
		Frequency : 2.402 - 2.480 GHz
		Transmit Power: +8 dBm (Maximum)
	WiFi	802.11 a/b/g/n 1x1, 2.4GHz & 5GHz
		Frequency : 2.400 ~ 2.484GHz; 5.18 ~ 5.825GHZ.
		Transmit Power(2.4GHZ): 17.5 dBm(11 b),15.5 dBm(11 g), 13.5 dBm(11 n)
		Transmit Power(5GHZ): 8dBm(11 a)
		Support 20MHz/40MHz up to MCS7
		Low power architecture
		Support low power Tx/Rx for short range application
		Low power beacon listen mode
		Low power Rx mode
		Very low power suspends mode (DLPS)
		AES/DES/SHA hardware engine
Host Interface and Peripherals	UART Interface	TX, RX (Auto Flow Control)
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 110 to 6000000
		7, 8 data bit character
	GPIO	16 (maximum – configurable) lines
		O/P drive strength (4 mA)
		Pull-up resistor (33 KΩ) control
		Read pin-level
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps(standard) /3.33Mbps(high speed)
	SPI Interface	Support Master/Slave mode
	PWM	16-bit resolution
		8-bit prescaler and clock divider
		Supports PWM interrupts
		supports input capture function
Profiles	Classic Bluetooth	No Supports
	Bluetooth Low Energy	Support both central and peripheral modes
	WiFi	WiFi-AP(access point), WiFi-Station
Maximum Connections	Classic Bluetooth	No Supports
	Bluetooth Low Energy	5 Clients(MAX)(TBD)
FW upgrade		Via UART(TBD)
		J-link
Supply Voltage	Supply	3.0-3.6V

Power Consumption	Bluetooth	Max Peak Current(TX Power @ +8dBm TX): 84mA(TBD)
		Standby Doze (Wait event) - 19mA (TBD)
		Deep Sleep – (TBD)
	WiFi	3.3V Rating Current(with internal regulator and integrated COMS PA: 450mA (MAX)
		IO Rating Current(including VDD_IO): 200mA
Physical	Dimensions	13mm X 26.9mm X 2.2mm; Pad Pitch 1.5mm
Environmental	Operating	-20°C to +85°C
	Storage	-55°C to +125°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class-2 Machine Model: Class-B

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

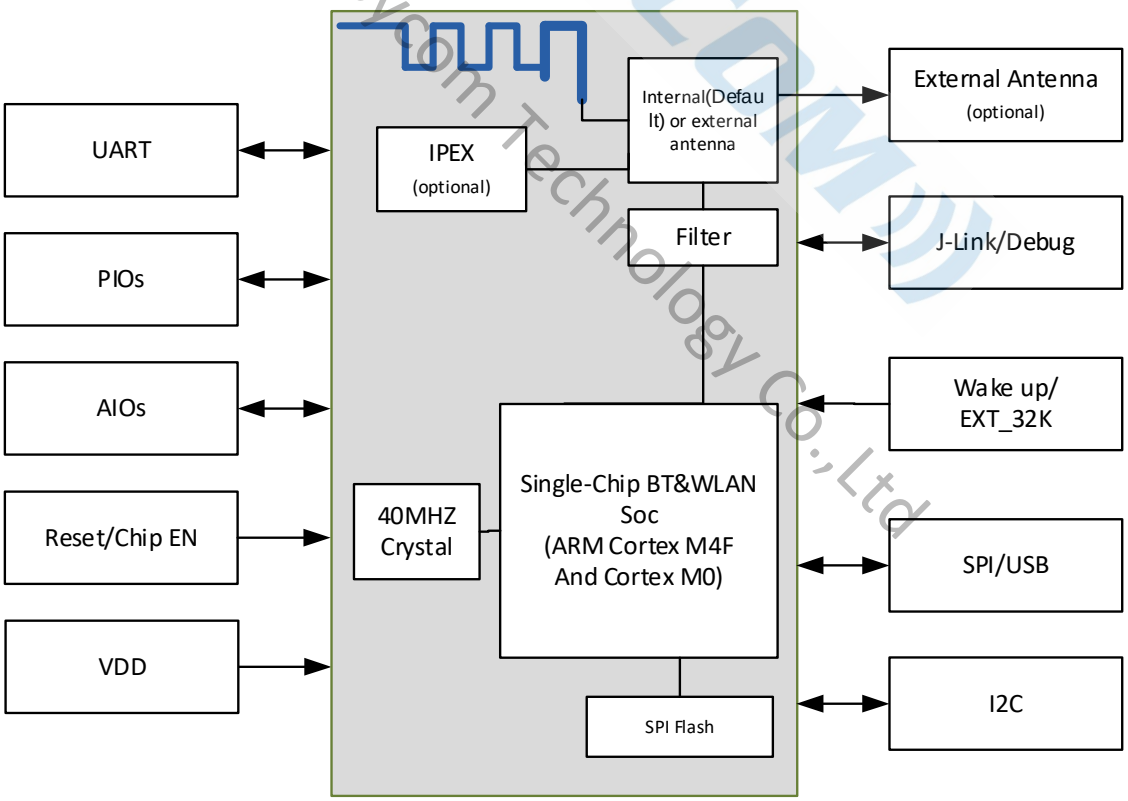


Figure 2: Block Diagram

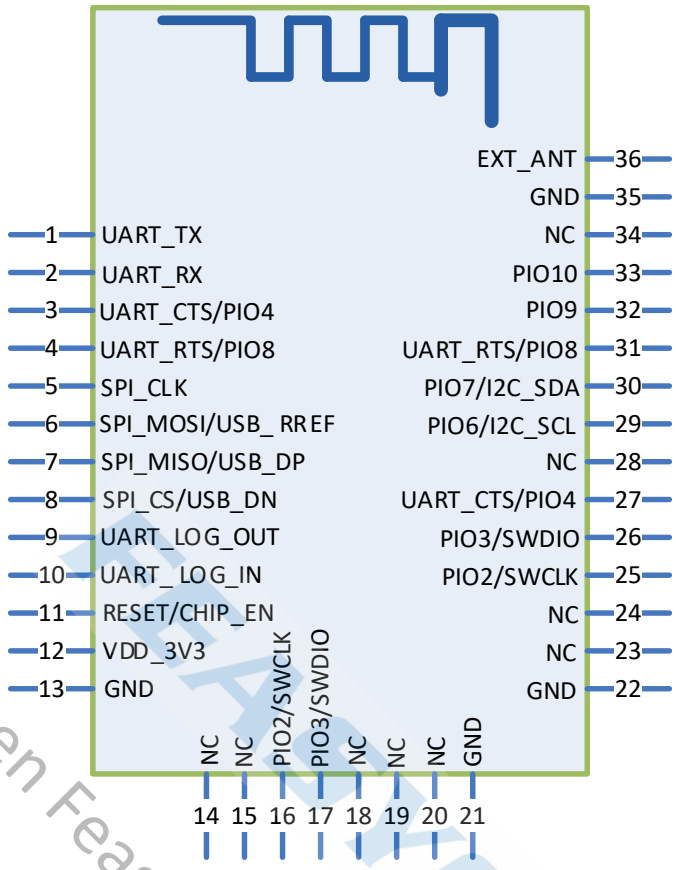


Figure 3: FSC-BW236 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_TX	O	UART Data output	Note 1
2	UART_RX	I	UART Data input	Note 1
3	UART_CTS/PIO4	I/O	UART Clear to Send (active low) Alternative Function 1: Programmable input/output line	Note 1
4	UART_RTS/PIO8	I/O	UART Request to Send (active low) Alternative Function 1: Programmable input/output line	Note 1
5	SPI_CLK		SPI_CLK Alternative Function 1: Programmable input/output line	
6	SPI_MOSI/USB_ RREF		SPI_MOSI Alternative Function 1: Programmable input/output line Alternative Function 2: USB_PREF ***(External reference resistor for USB analog, pull down to ground through the resistor -- 12KΩ 1%)***	
7	SPI_MISO/USB_DP		SPI_MISO Alternative Function 1: Programmable input/output line Alternative Function 2: USB_DP	
8	SPI_CS/USB_DN		SPI_CS Alternative Function 1: Programmable input/output line Alternative Function 2: USB_DN	

9	UART_LOG_OUT	O	Debug Interface (Data OUT)	
10	UART_ LOG_IN	I	Debug Interface (Data IN)	
11	RESET/CHIP_EN	I	External reset input: Active LOW, Set this pin low reset the module. (With Internal pull-up 100K resistor.)	
12	VDD_3V3	Vdd	Power supply voltage 3.3V	
13	GND	Vss	Power Ground	
14	NC		NC	
15	NC		NC	
16	PIO2/SWCLK	I/O	Debugging through the clk line(Default) Alternative Function: Programmable input/output line	
17	PIO3/SWDIO	I/O	Debugging through the data line(Default) Alternative Function 1: Programmable input/output line	
18	NC		NC	
19	NC		NC	
20	NC		NC	
21	GND	Vss	Power Ground	
22	GND	Vss	Power Ground	
23	NC		NC	
24	NC		NC	
25	PIO2/SWCLK	I/O	Debugging through the clk line(Default) Alternative Function: Programmable input/output line	
26	PIO3/SWDIO	I/O	Debugging through the data line(Default) Alternative Function 1: Programmable input/output line	
27	UART_CTS/PIO4	I/O	UART Clear to Send (active low) Alternative Function 1: Programmable input/output line	Note 1
28	NC		NC	
29	PIO6/I2C_SCL	I/O	Programmable input/output line	Note 2
30	PIO7/I2C_SDA	I/O	Programmable input/output line	Note2
31	UART_RTS/PIO8	I/O	UART Request to Send (active low) Alternative Function: Programmable input/output line	Note 1
32	PIO9	I/O	BT LED(Default) /Status or Programmable input/output line	Note 3
33	PIO10	I/O	WIFI LED (Default) / Status or Programmable input/output line	Note4
34	NC		NC	
35	GND	Vss	RF Ground	
36	EXT_ANT	O	RF signal output	Note5

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 3	BT LED(Default) /Status – LED Power On: Light Slow Shinning ; Connected: Steady Lighting. Status Disconnected: Low Level; Connected: High Level
Note 4	WIFI LED(Default) /Status -- LED Power On: Light Slow Shinning ; Connected: Steady Lighting. Status Disconnected: Low Level; Connected: High Level.

Note 5	By default, this PIN is an empty feet. This PIN can connect to an external antenna to improve the Bluetooth/WIFI signal coverage. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna; Or contact Feasycom for modification.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

4.3 General Purpose Digital IO

- GPO and GPI function
- Support interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

4.4 RF Interface

For This Module, the default mode for antenna is internal , it also has the interface for external antenna, or use an IPEX interface to connect an external antenna. If you need to use an external antenna, by modifying the module on the 0R resistance to block out the on-board antenna. Or indicate your request when placing an order.

The user can connect a 50 ohm antenna directly to the RF port.

Bluetooth basic parameter：

- 2402–2480 MHz Bluetooth 5.0 Mode (BLE); 1 Mbps over the air data rate.
- TX output power of +8dBm.
- Receiver to achieve maximum sensitivity -85dBm @ 1 Mbps BLE.

WiFi basic parameter：

- 2412–2484 MHz IEEE 802.11 b/g/n compatible WLAN
- Transmit Power(2.4GHZ): 17.5dBm(11 b), 15.5dBm(11 g), 13.5dBm(11 n).
- Transmit Power(5GHZ): 8dBm(11 a)
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Receiver to achieve maximum sensitivity(2.4GHZ)： -80dBm(11 b), -75dBm(11 g), -70dBm(11 n).
- Receiver to achieve maximum sensitivity(5GHZ)： -72dBm(11 a).

4.5 Serial Interfaces

4.5.1 UART

- Support 1 HS-UART
- UART(RS232 Standard) Serial Data Format
- Transmit and Receive data FIFO
- Programmable asynchronous clock support
- Auto flow control
- Programmable Receive data FIFO trigger level
- UART signal level ranges 3.3V

Table 3: Possible UART Settings

Parameter	Possible Values	
Baudrate	Minimum	110 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	6000000bps(≤1%Error)
Flow control		RTS/CTS
Parity		None, Odd or Even
Number of stop bits		1 /2
Bits per channel		7/8

When connecting the module to a host, please make sure to follow .

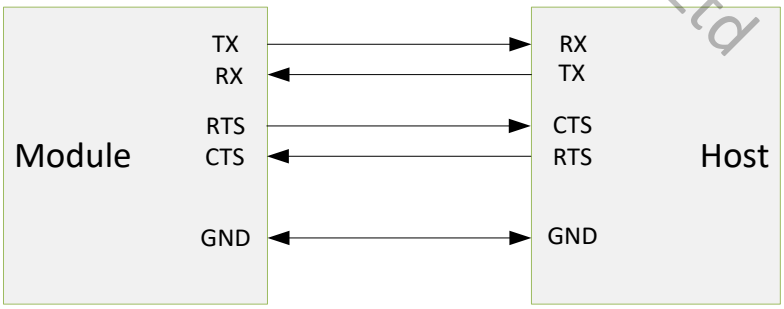


Figure 4: UART Connection

4.5.2 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

- Three speeds: Standard mode(0 to 100Kb/S); Fast mode(<400 Kb/S); High-speed mode(<3.4Mb/S)
- Master or slave I2C operation
- 7- or 10-bit addressing
- Transmit and receive buffers

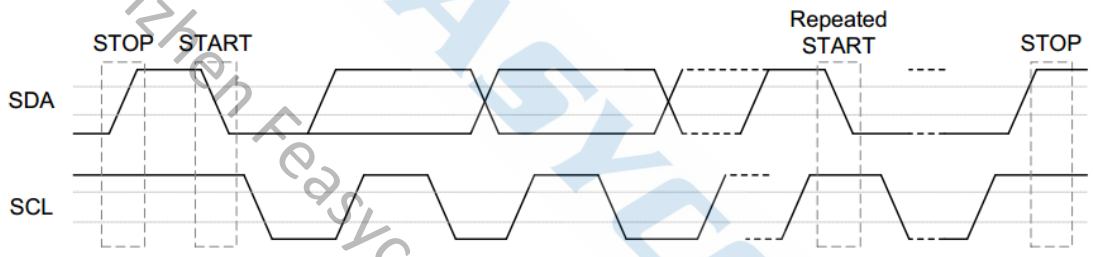


Figure 5: I2C Bus Timing

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

4.6 PWM Generator and Capture Timer (PWM)

FSC-BW236 has **8** PWM generator. The PWM generator has a 16-bit PWM counter and comparator, and the PWM generator supports two standard PWM output modes: Independent output mode and Complementary output mode with 8-bit Dead-time generator. Each mode can be used as a timer and issues interrupt independently. In addition, It also has an 8-bit prescaler and clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16) to support wide range clock frequency of PWM counter. For PWM output control unit, it supports polarity output function.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

4.7 SPI

- Support Motorola SPI Serial interface operation
- Support master or slave operation mode

- Provide two SPI ports: configured as master with Max. baud rate: 25MHz.
- Support DMA interface for DMA transfer
- Independent masking of interrupts
- FIFO depth – The transmit and receive FIFO buffers 64 words deep. The FIFO width is fixed at 16 bits.
- Hardware/software slave-select – Dedicated hardware slave-select lines can be used or software control can be used to target the serial-slave device
- Programmable features:

--Clock bit-rate – Dynamic control of the serial bit rate of the data transfer; used in only serial- master mode of operation.

--Data item size (4 to 16 bits) – Item size of each data transfer under the control of the programmer.

--Configurable clock polarity and phase

--Programmable delay on the sample time of the received serial data bit (rxd), when configured in Master Mode; enables programmable control of routing delays resulting in higher serial data-bit rates.

4.9 USB

- Support USB 2.0
- Support HS/FS/LS mode
- Internal DMA support, DMA works based on register settings
- 1.5KByte bulk-in buffer and 1.5KByte bulk-out buffer

4.8 IR (Infra Ray)

- Support carrier frequency from 25KHz to 500KHz
- Support Duty from 1/2 to 1/5
- Support IR diode input
- Support IR receiver module input
- 32*4 bytes Tx FIFO
- 32*4 bytes Rx FIFO
- Tx carrier frequency can be configured
- Tx carrier duty cycle can be configured

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.
The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 4: Absolute Maximum Rating

Parameter	Min	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	-0.3	+3.6	V
V_{IN} - Input Voltage	Vss-0.3	Vdd+0.3	V

T_A - Operating Temperature	-20	+85	°C
T_{ST} - Storage Temperature	-55	+125	°C
T_{JT} - Junction Temperature	0	+125	°C
I_{IO} - Maximum Current sunk by a I/O pin		4	mA
I_{IO} - Maximum Current sourced by a I/O pin		4	mA

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	3	3.3	3.6	V
V_{IN} - Input Voltage	Vss-0.3	3.3	Vdd+0.3	V
T_A - Operating Temperature	-20	25	+85	°C
T_{ST} - Storage Temperature	-55	25	+125	°C
T_{JT} - Junction Temperature	0	-	+125	°C
I_{IO} - Maximum Current sunk by a I/O pin	2	3	4	mA
I_{IO} - Maximum Current sourced by a I/O pin	2	3	4	mA
IDD- 3.3V Rating Current (With internal regulator and integrated COMS PA) (Wifi only)	-	-	450	mA

5.3 Input/output Terminal Characteristics

Table 6: DC Characteristics (V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
V_{DD} - Operation Voltage	3	3.3	3.6	V
V_{SS} - Power Ground	-0.3	-	-	V
V_{DD12} - Core Logic and I/O Buffer Pre-Driver Voltage	1.08	1.2	1.32	V
V_{OH} - High Level Output Voltage	2.4	-	-	V
V_{OL} - Low Level Output Voltage	-	-	0.4	V
V_{IH} - Input High Voltage	2.0	-	-	V
V_{IL} - Input Low Voltage	-	-	0.8	V
V_{TH} - Switch Threshold(Schmitt-falling-trigger)	1.36	1.45	1.56	V
V_{TH} - Switch Threshold(Schmitt-rising-trigger)	1.78	1.87	1.97	V
R_{PU} - Input Pull-up Resist(V_{IN}=V_{SS})	32	53	120	KΩ
R_{PD} - Input Pull-down Resist(V_{IN}=V_{DD})	37	49	120	KΩ
I_L - Input Leakage Current	-10	-	10	uA
I_{OZ} - Tri-State Output Leakage Current	-10	-	10	uA
I_{OL} - Low level sink current(V_{OL}=0.4V)	4	-	-	mA
I_{OH} - High level source current (V_{OH}=2.4V)	4	-	-	mA

5.4 Power State and Power Sequence

Table 7: Timing specification of power sequence

Parameter	Min	Type	Max	Unit
T_{PRDY} - VDDx ready time	0.6	0.6	1	ms
T_{clk} - Internal ring clock stable time after VDD1833 ready	1	-	-	ms
T_{core} - LP core power ready time	1.5	1.5	-	ms
T_{boot} - HS MCU boot time	200	200	-	ms
V_{rst} - Shutdown occurs after CHIP_EN lower than this voltage	0	0	0.5 * VDDx	V
T_{rst} - The required time that CHIP_EN lower than V_{RST}	1	1	-	ms

Note: VDD*x* is the supply power of VDD_3V3

5.5 Power on or Resuming from Deep sleep Sequence

Note: VDD*x* is the supply power of VDD_3V3

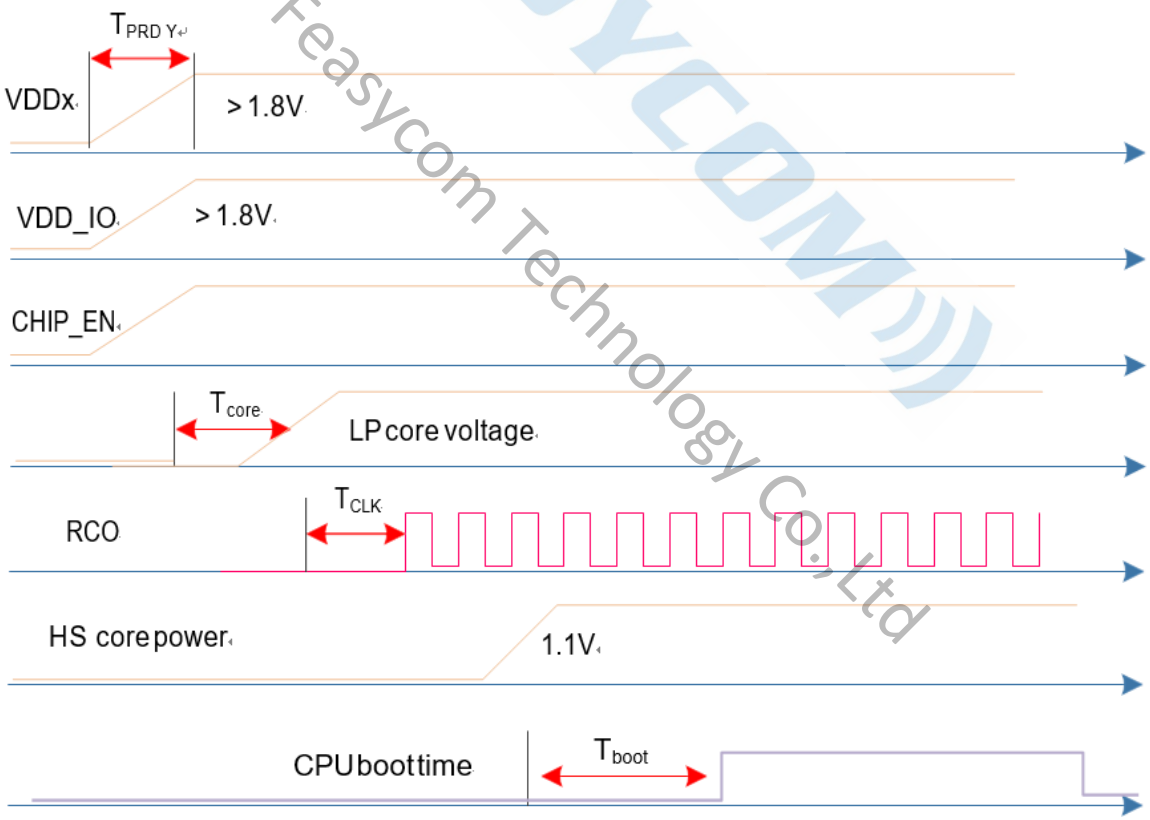


Figure 6: Timing sequence of power on or resuming from deepsleep

5.6 Shutdown Sequence

Note: VDD*x* is the supply power of VDD_3V3

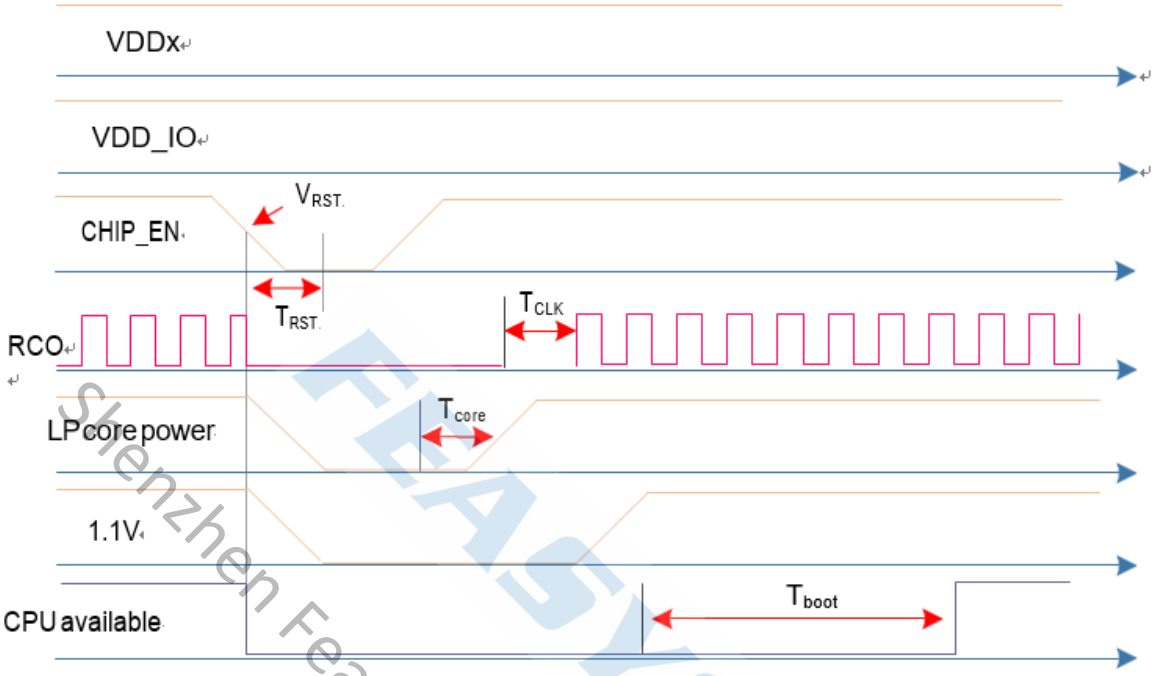


Figure 7: Timing sequence of shutdown

5.7 I2C Dynamic Characteristics

Table 8: I2C Dynamic Characteristics

Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
	Min	Max	Min	Max	
t_{LOW} - SCL low period	4.7	-	1.2	-	uS
T_{HIGH} - SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$ - Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$ - START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$ - STOP condition setup time	4	-	0.6	-	uS
t_{BUF} - Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$ - Data setup time	250	-	100	-	uS
$t_{HD;DAT}$ - Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r - SCL/SDA rise time	-	1000	20+0.1CB	300	uS
t_f- SCL/SDA fall time	-	300	-	300	uS
C_b - Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

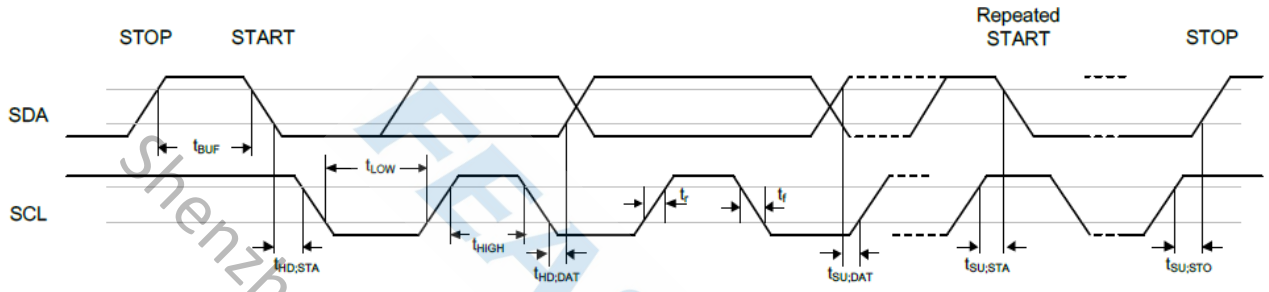


Figure 8: I2C Timing Diagram

5.8 Power consumptions

Table 9: Power consumptions(TBD)

Parameter	Test Conditions	Type	Unit
Bluetooth			
Search		~35	mA
Unconnected (Deep Sleep Idle Mode)	No support	-	mA
Connected Idle		~19	mA
Shutdown		<50	uA
WLAN			
3.3V Rating Current (With internal regulator and integrated COMS PA)		450	mA
Shutdown		<50	uA

6. MSL & ESD

Table 10: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	Human Body Model: Class-2 Machine Model: Class-B

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 11: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

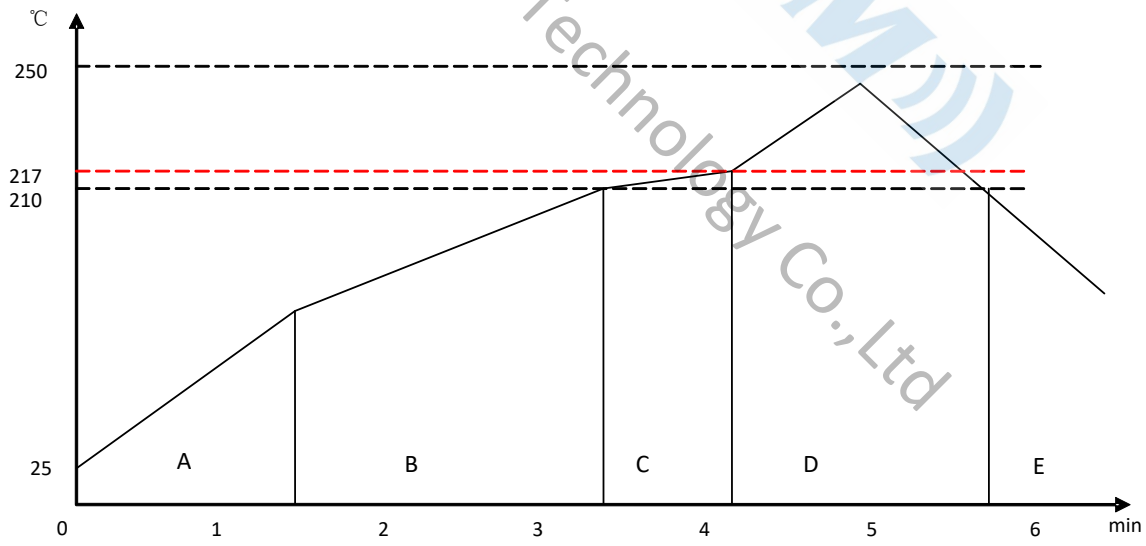


Figure 9: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 13mm(W) x 26.9mm(L) x 2.0mm(H) Tolerance: ±0.1mm
- Module size: 13mm X 26.9mm Tolerance: ±0.2mm
- Pad size: 1mmX0.8mm Tolerance: ±0.2mm
- Pad pitch: 1.5mm Tolerance: ±0.1mm

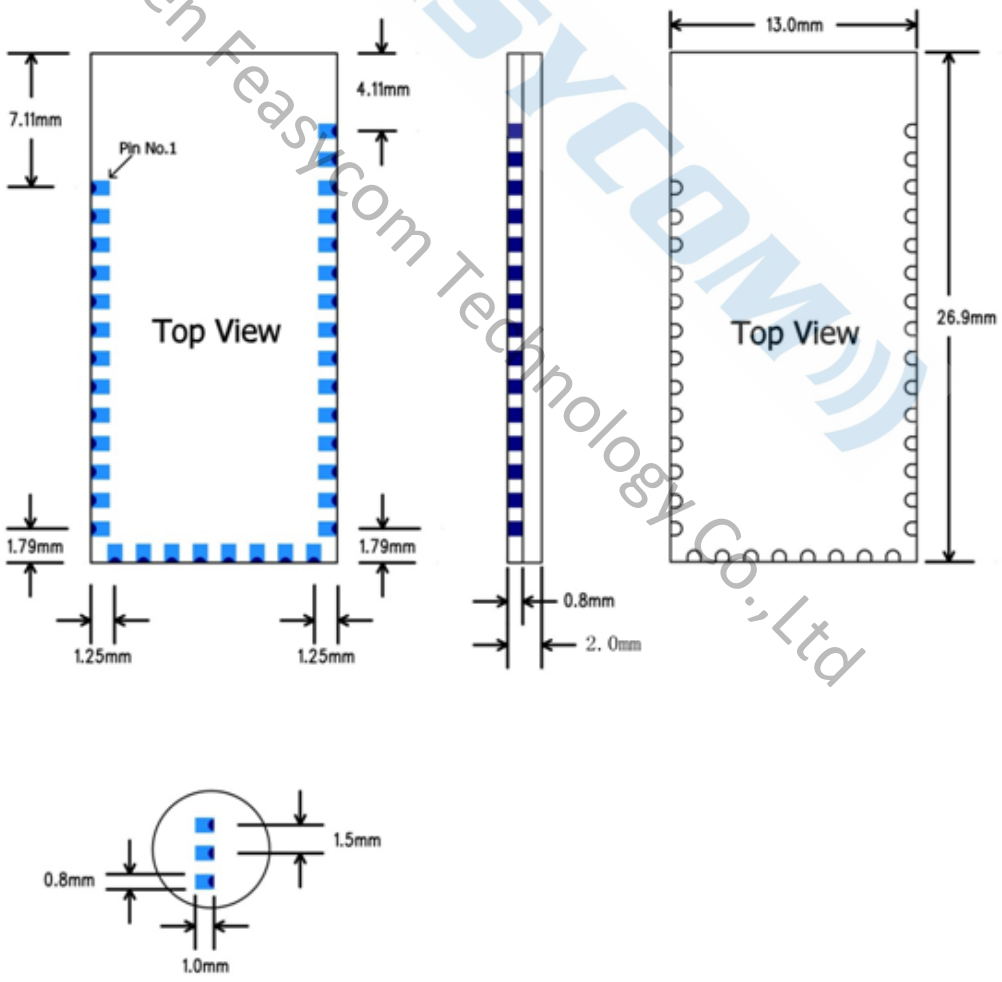


Figure 10: FSC-BW236 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BW236 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

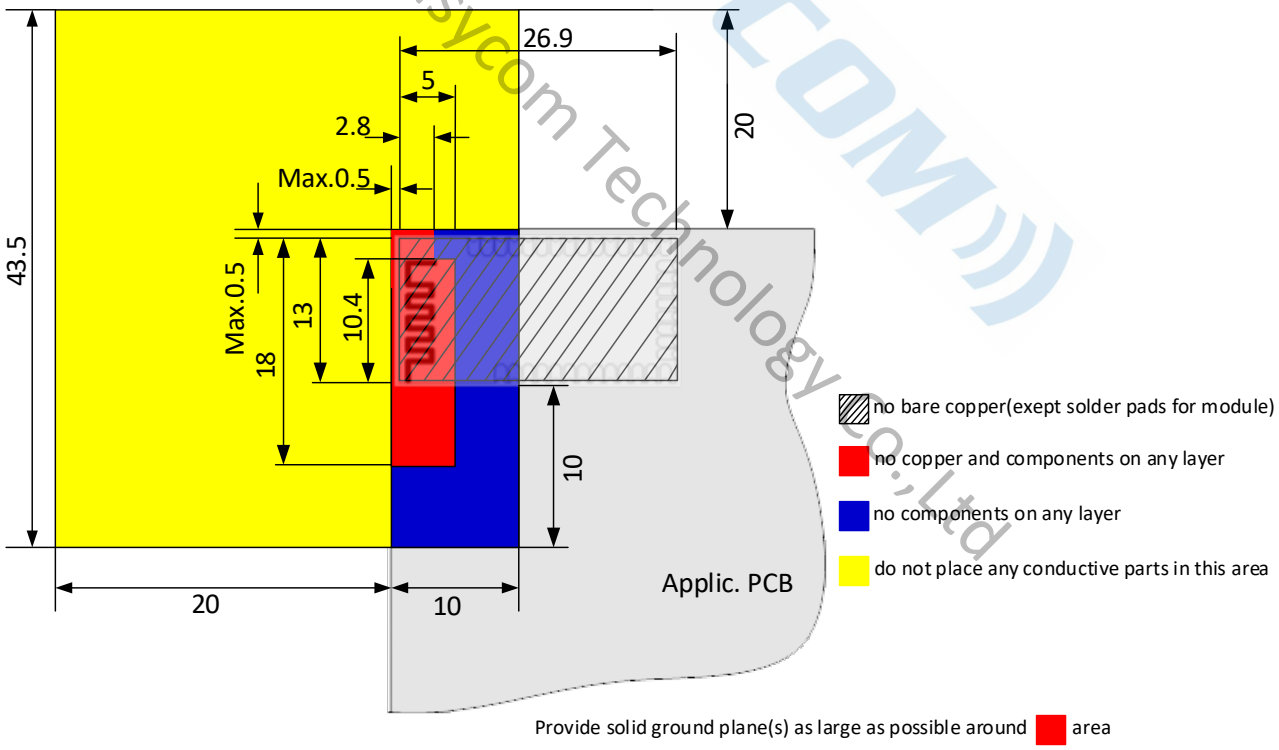


Figure 11: FSC-BW236 Restricted Area（Unit：mm）

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via,

always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

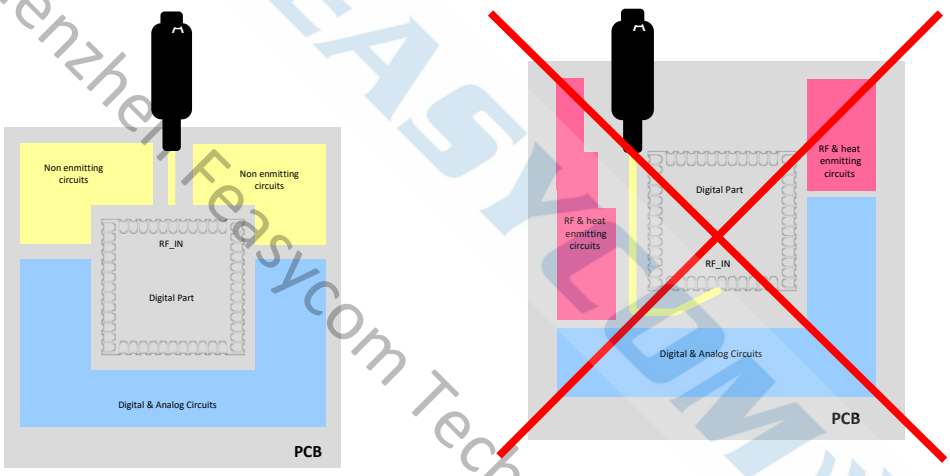


Figure 12: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

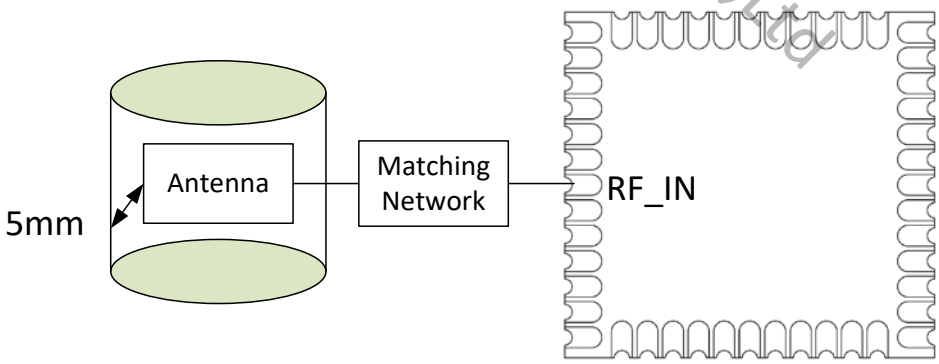


Figure 13: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

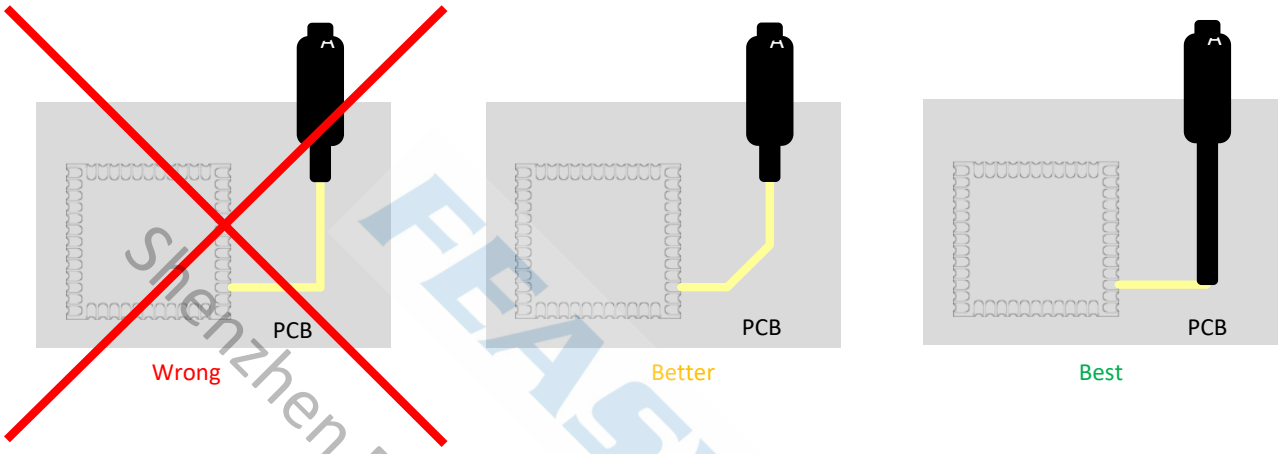


Figure 14: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

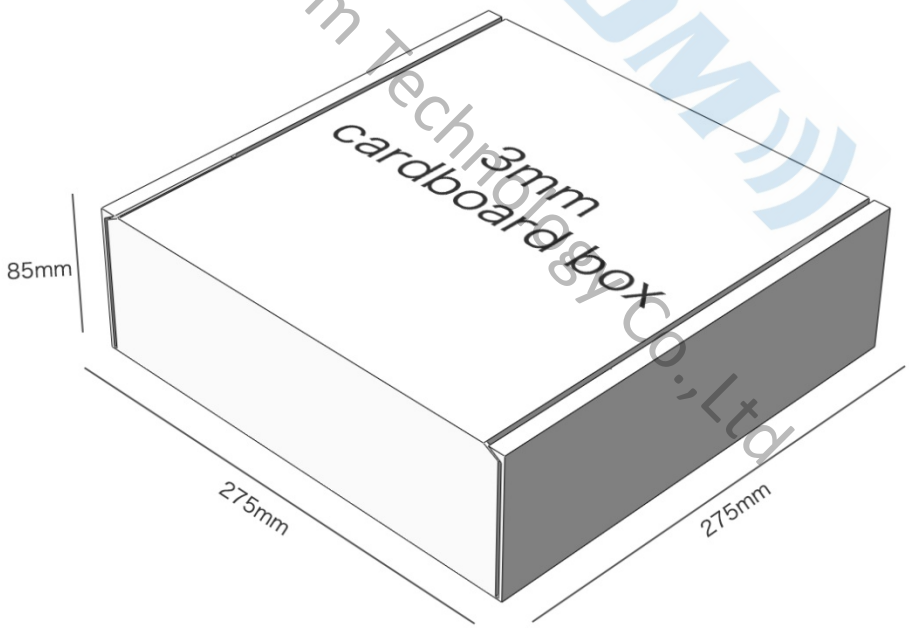
10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 15: Tray vacuum

10.2 Packing box(Optional)



* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 16: Packing Box

11. APPLICATION SCHEMATIC