

**Radiation Hardened, SEGR Resistant N-Channel Power MOSFETs**



Fairchild Star\*Power™ Rad Hard MOSFETs have been specifically developed for high performance applications in a commercial or military space environment.

Star\*Power MOSFETs offer the system designer both extremely low  $r_{DS(ON)}$  and Gate Charge allowing the development of low loss Power Subsystems. Star\*Power Gold FETs combine this electrical capability with total dose radiation hardness up to 100K RADs while maintaining the guaranteed performance for Single Event Effects (SEE) which the Fairchild FS families have always featured.

The Fairchild family of Star\*Power FETs includes a series of devices in various voltage, current and package styles. The portfolio consists of Star\*Power and Star\*Power Gold products. Star\*Power FETs are optimized for total dose and  $r_{DS(ON)}$  while exhibiting SEE capability at full rated voltage up to an LET of 37. Star\*Power Gold FETs have been optimized for SEE and Gate Charge combining SEE performance to 80% of the rated voltage for an LET of 82 with extremely low gate charge characteristics.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specifically designed and processed to be radiation tolerant. The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, power distribution, motor drives and relay drivers as well as other power control and conditioning applications. As with conventional MOSFETs these Radiation Hardened MOSFETs offer ease of voltage control, fast switching speeds and ability to parallel switching devices.

Reliability screening is available as either TXV or Space equivalent of MIL-PRF-19500.

Formerly available as type TA45228W.

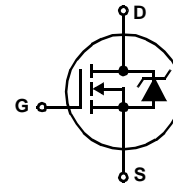
**Ordering Information**

RAD LEVEL	SCREENING LEVEL	PART NUMBER/BRAND
10K	Engineering samples	FSGL134D1
100K	TXV	FSGL134R3
100K	Space	FSGL134R4

**Features**

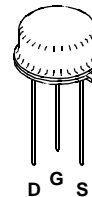
- 10A, 150V,  $r_{DS(ON)} = 0.125\Omega$
- UIS Rated
- Total Dose
  - Meets Pre-RAD Specifications to 100K RAD (Si)
- Single Event
  - Safe Operating Area Curve for Single Event Effects
  - SEE Immunity for LET of 82MeV/mg/cm<sup>2</sup> with  $V_{DS}$  up to 80% of Rated Breakdown and  $V_{GS}$  of 5V Off-Bias
- Dose Rate
  - Typically Survives 3E9 RAD (Si)/s at 80%  $BV_{DSS}$
  - Typically Survives 2E12 if Current Limited to  $I_{AS}$
- Photo Current
  - 2nA Per-RAD (Si)/s Typically
- Neutron
  - Maintain Pre-RAD Specifications for 1E13 Neutrons/cm<sup>2</sup>
  - Usable to 1E14 Neutrons/cm<sup>2</sup>

**Symbol**



**Packaging**

TO-205AF



# FSGL134R

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	FSGL134R	UNITS
Drain to Source Voltage $V_{DS}$	150	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) $V_{DGR}$	150	V
Continuous Drain Current		
$T_C = 25^\circ\text{C}$ $I_D$	10	A
$T_C = 100^\circ\text{C}$ $I_D$	6	A
Pulsed Drain Current $I_{DM}$	40	A
Gate to Source Voltage $V_{GS}$	$\pm 30$	V
Maximum Power Dissipation		
$T_C = 25^\circ\text{C}$ $P_T$	25	W
$T_C = 100^\circ\text{C}$ $P_T$	10	W
Linear Derating Factor	0.20	W/ $^\circ\text{C}$
Single Pulsed Avalanche Current, $L = 100\mu\text{H}$ , (See Test Figure) $I_{AS}$	40	A
Continuous Source Current (Body Diode) $I_S$	10	A
Pulsed Source Current (Body Diode) $I_{SM}$	40	A
Operating and Storage Temperature $T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$
Lead Temperature (During Soldering) $T_L$ (Distance $>0.063\text{in}$ (1.6mm) from Case, 10s Max)	300	$^\circ\text{C}$
Weight (Typical)	1.0 (Typical)	g

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 1\text{mA}, V_{GS} = 0\text{V}$	150	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 1\text{mA}$	$T_C = -55^\circ\text{C}$	-	-	5.5	V
			$T_C = 25^\circ\text{C}$	2.0	-	4.5	V
			$T_C = 125^\circ\text{C}$	1.0	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 120\text{V}, V_{GS} = 0\text{V}$	$T_C = 25^\circ\text{C}$	-	-	25	$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 30\text{V}$	$T_C = 25^\circ\text{C}$	-	-	100	nA
			$T_C = 125^\circ\text{C}$	-	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	$V_{GS} = 12\text{V}, I_D = 10\text{A}$	-	-	1.30	V	
Drain to Source On Resistance	$r_{DS(ON)12}$	$I_D = 6\text{A}, V_{GS} = 12\text{V}$	$T_C = 25^\circ\text{C}$	-	0.110	0.125	$\Omega$
			$T_C = 125^\circ\text{C}$	-	-	0.219	$\Omega$
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 75\text{V}, I_D = 10\text{A}, R_L = 7.5\Omega, V_{GS} = 12\text{V}, R_{GS} = 7.5\Omega$	-	-	20	ns	
Rise Time	$t_r$		-	-	40	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	35	ns	
Fall Time	$t_f$		-	-	25	ns	
Total Gate Charge	$Q_g(12)$		$V_{GS} = 0\text{V to } 12\text{V}$	-	26	28	nC
Gate Charge Source	$Q_{gs}$	$75\text{V} \leq V_{DD} \leq 120\text{V}, I_D = 10\text{A}$	-	10	12	nC	
Gate Charge Drain	$Q_{gd}$		-	8	10	nC	
Gate Charge at 20V	$Q_g(20)$	$V_{GS} = 0\text{V to } 20\text{V}$	-	40	-	nC	
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V to } 2\text{V}$	-	3	-	nC	
Plateau Voltage	$V_{(PLATEAU)}$	$I_D = 10\text{A}, V_{DS} = 15\text{V}$	-	7	-	V	
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	1200	-	pF	
Output Capacitance	$C_{OSS}$		-	275	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	16	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5.0	$^\circ\text{C/W}$	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	$V_{SD}$	$I_{SD} = 10A$	-	-	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 10A, dI_{SD}/dt = 100A/\mu s$	-	-	190	ns
Reverse Recovery Charge	$Q_{RR}$		-	1.0	-	$\mu C$

Electrical Specifications up to 100K RAD  $T_C = 25^\circ C$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts	(Note 3) $BV_{DSS}$	$V_{GS} = 0, I_D = 1mA$	150	-	V
Gate to Source Threshold Volts	(Note 3) $V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 1mA$	2.0	4.5	V
Gate to Body Leakage	(Notes 2, 3) $I_{GSS}$	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	100	nA
Zero Gate Leakage	(Note 3) $I_{DSS}$	$V_{GS} = 0, V_{DS} = 120V$	-	25	$\mu A$
Drain to Source On-State Volts	(Notes 1, 3) $V_{DS(ON)}$	$V_{GS} = 12V, I_D = 10A$	-	1.30	V
Drain to Source On Resistance	(Notes 1, 3) $r_{DS(ON)12}$	$V_{GS} = 12V, I_D = 6$	-	0.125	$\Omega$

NOTES:

1. Pulse test, 300 $\mu s$  Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both  $V_{GS} = 12V, V_{DS} = 0V$  and  $V_{GS} = 0V, V_{DS} = 80\% BV_{DSS}$ .

Single Event Effects (SEB, SEGR) Note 4

TEST	SYMBOL	ENVIRONMENT (NOTE 5)		APPLIED $V_{GS}$ BIAS (V)	(Note 7) MAXIMUM $V_{DS}$ BIAS (V)
		(Note 6) TYPICAL LET (MeV/mg/cm <sup>2</sup> )	TYPICAL RANGE ( $\mu$ )		
Single Event Effects Safe Operating Area	SEESOA	37	36	-20	150
		60	32	-10	150
		82	28	-5	120
		82	28	-10	90

NOTES:

4. Testing conducted at Brookhaven National Labs or Texas A&M.
5. Fluence = 1E5 ions/cm<sup>2</sup> (typical), T = 25 $^\circ C$ .
6. Ion Species: LET = 37, Br or Kr; LET = 60, I or Xe; LET = 82, Au
7. Does not exhibit Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR).

Performance Curves Unless Otherwise Specified

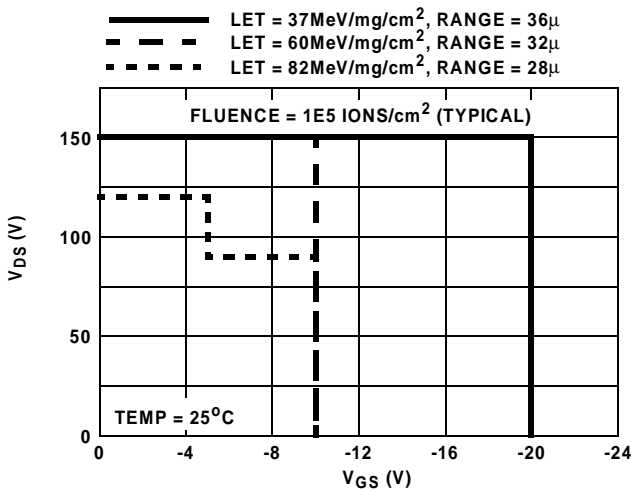


FIGURE 1. SINGLE EVENT EFFECTS SAFE OPERATING AREA

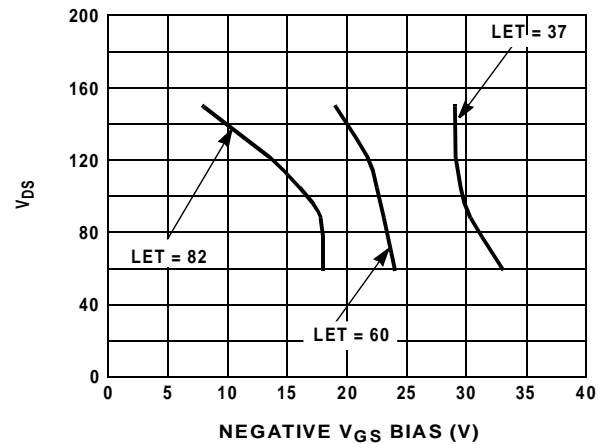


FIGURE 2. TYPICAL SEE SIGNATURE CURVE

Performance Curves Unless Otherwise Specified (Continued)

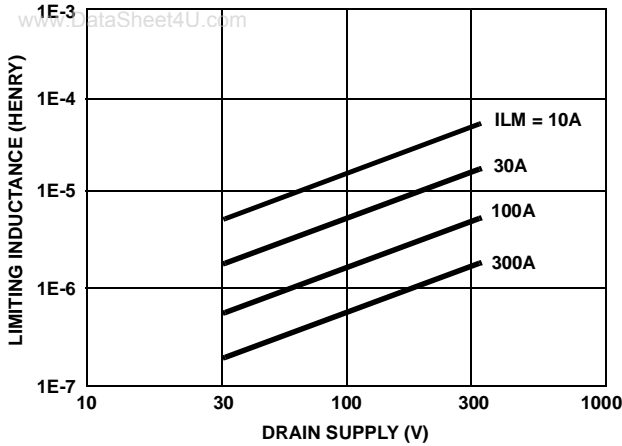


FIGURE 3. TYPICAL DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO  $I_{AS}$

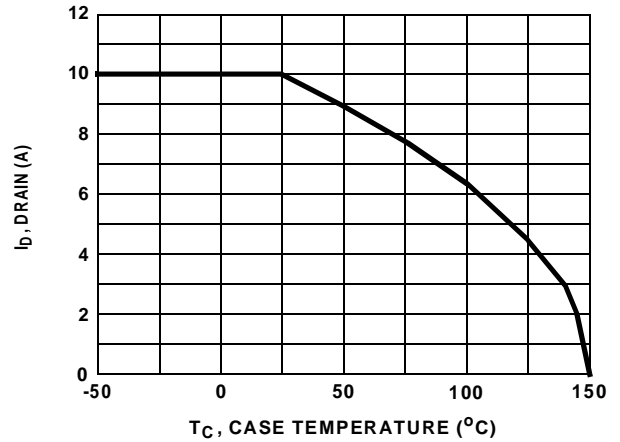


FIGURE 4. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

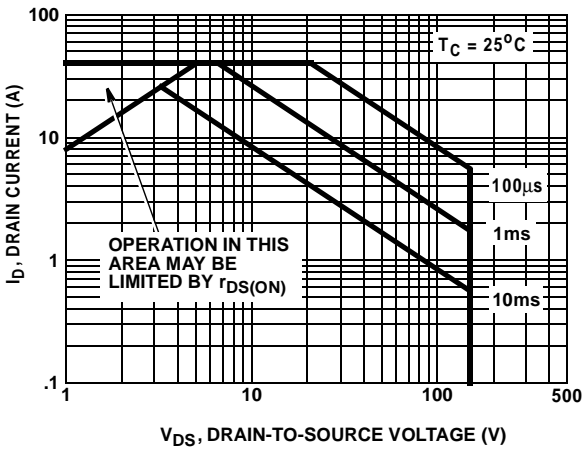


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

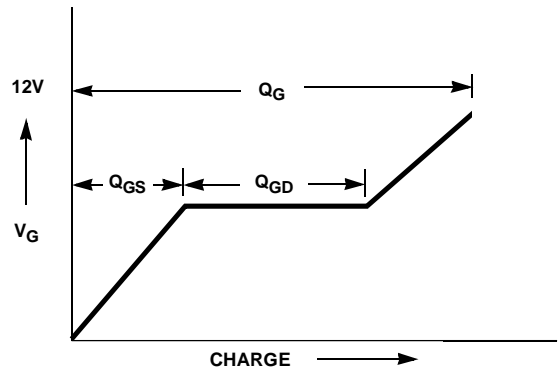


FIGURE 6. BASIC GATE CHARGE WAVEFORM

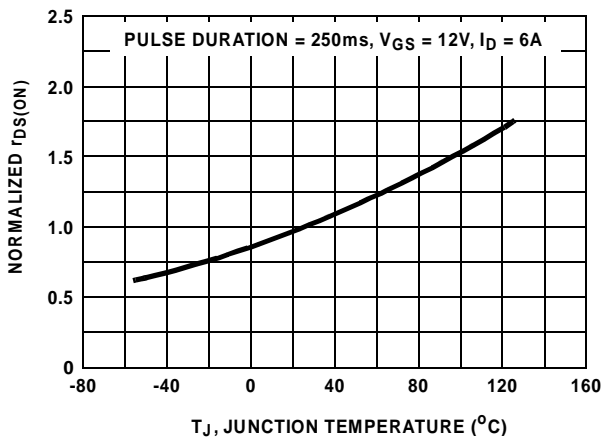


FIGURE 7. TYPICAL NORMALIZED  $r_{DS(ON)}$  vs JUNCTION TEMPERATURE

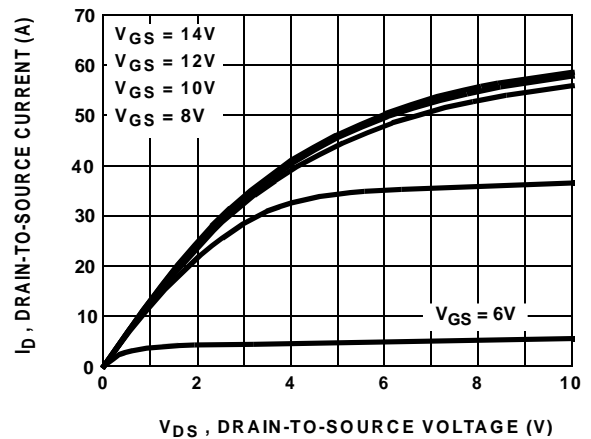


FIGURE 8. TYPICAL OUTPUT CHARACTERISTICS

Performance Curves Unless Otherwise Specified (Continued)

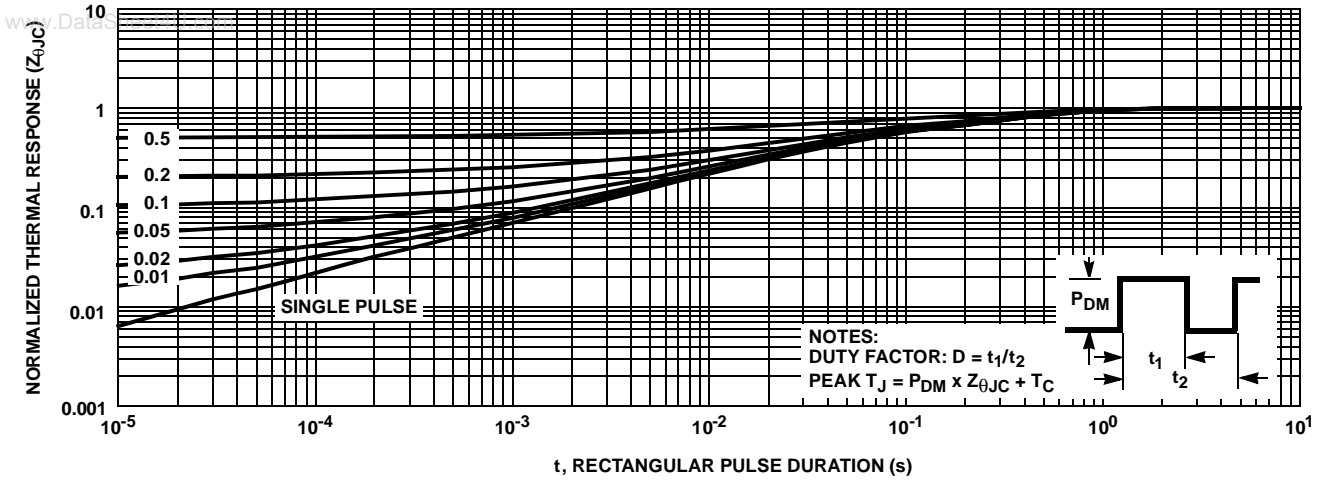


FIGURE 9. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

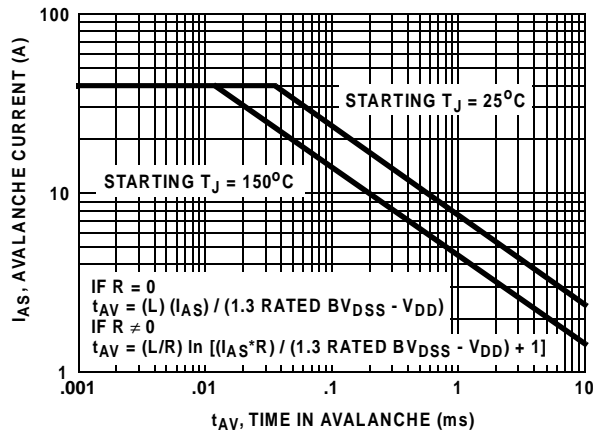


FIGURE 10. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

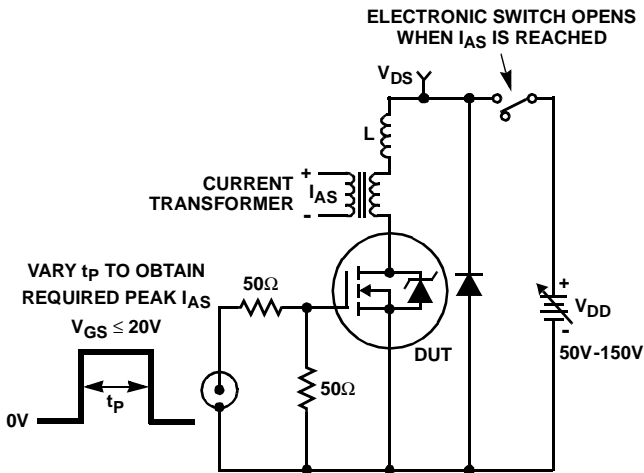


FIGURE 11. UNCLAMPED ENERGY TEST CIRCUIT

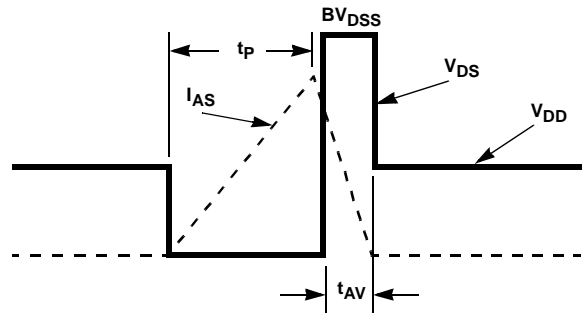


FIGURE 12. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms

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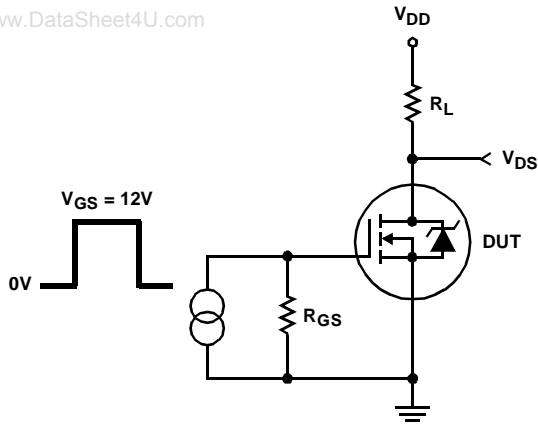


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT

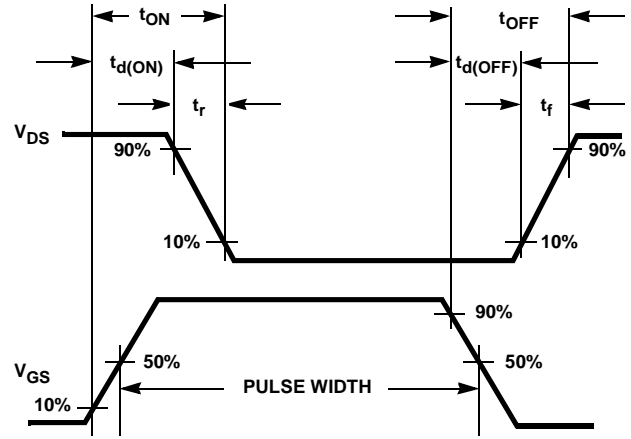


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-PRF-19500, (Screening Information Table).

Delta Tests and Limits (JANTXV Equivalent, JANS Equivalent)  $T_C = 25^{\circ}C$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 30V$	$\pm 20$ (Note 8)	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\%$ Rated Value	$\pm 25$ (Note 8)	$\mu A$
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 25^{\circ}C$ at Rated $I_D$	$\pm 20\%$ (Note 9)	$\Omega$
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0mA$	$\pm 20\%$ (Note 9)	V

NOTES:

- 8. Or 100% of Initial Reading (whichever is greater).
- 9. Of Initial Reading.

Screening Information

TEST	JANTXV EQUIVALENT	JANS EQUIVALENT
Unclamped Inductive Switching	$V_{GS(PEAK)} = 20V$ , $L = 0.1mH$ ; Limit = 40A	$V_{GS(PEAK)} = 20V$ , $L = 0.1mH$ ; Limit = 40A
Thermal Response	$t_H = 10ms$ ; $V_H = 25V$ ; $I_H = 1A$ ; LIMIT = 60mV	$t_H = 10ms$ ; $V_H = 25V$ ; $I_H = 1A$ ; LIMIT = 60mV
Gate Stress	$V_{GS} = 45V$ , $t = 250\mu s$	$V_{GS} = 45V$ , $t = 250\mu s$
Pind	Optional	Required
Pre Burn-In Tests (Note 10)	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at $25^{\circ}C$ )	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at $25^{\circ}C$ )
Steady State Gate Bias (Gate Stress)	MIL-PRF-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^{\circ}C$ , Time = 48 hours	MIL-PRF-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^{\circ}C$ , Time = 48 hours
Interim Electrical Tests (Note 10)	All Delta Parameters Listed in the Delta Tests and Limits Table	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-PRF-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^{\circ}C$ , Time = 160 hours	MIL-PRF-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^{\circ}C$ , Time = 240 hours
PDA	10%	5%
Final Electrical Tests (Note 10)	MIL-PRF-19500, Group A, Subgroup 2	MIL-PRF-19500, Group A, Subgroups 2 and 3

NOTE:

- 10. Test limits are identical pre and post burn-in.

Additional Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 120V$ , $t = 10ms$	0.7	A
Thermal Impedance	$\Delta V_{SD}$	$t_H = 500ms$ ; $V_H = 25V$ ; $I_H = 1A$	230	mV

**Rad Hard Data Packages - Fairchild Power Transistors**

**TXV Equivalent**

**1. RAD HARD TXV EQUIVALENT - STANDARD DATA PACKAGE**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
- F. Group C - Attributes Data Sheet
- G. Group D - Attributes Data Sheet

**2. RAD HARD TXV EQUIVALENT - OPTIONAL DATA PACKAGE**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
  - Pre and Post Burn-In Read and Record Data
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
  - Bond Strength Data (Subgroup B3)
  - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
- F. Group C - Attributes Data Sheet
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
  - Bond Strength Data (Subgroup C6)
- G. Group D - Attributes Data Sheet
  - Pre and Post RAD Read and Record Data

**Class S - Equivalents**

**1. RAD HARD "S" EQUIVALENT - STANDARD DATA PACKAGE**

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- F. Group A - Attributes Data Sheet
- G. Group B - Attributes Data Sheet
- H. Group C - Attributes Data Sheet
- I. Group D - Attributes Data Sheet

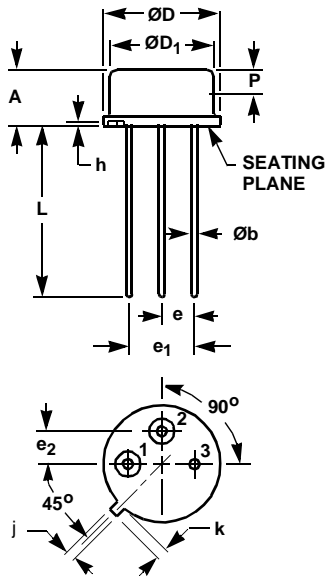
**2. RAD HARD MAX. "S" EQUIVALENT - OPTIONAL DATA PACKAGE**

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
  - X-Ray and X-Ray Report
- F. Group A - Attributes Data Sheet
  - Subgroups A2, A3, A4, A5 and A7 Data
- G. Group B - Attributes Data Sheet
  - Subgroups B1, B3, B4, B5 and B6 Data
- H. Group C - Attributes Data Sheet
  - Subgroups C1, C2, C3 and C6 Data
- I. Group D - Attributes Data Sheet
  - Pre and Post Radiation Data

**TO-205AF**

**3 LEAD JEDEC TO-205AF HERMETIC METAL CAN PACKAGE**

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SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.160	0.180	4.07	4.57	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
ØD <sub>1</sub>	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e <sub>1</sub>	0.190	0.210	4.83	5.33	4
e <sub>2</sub>	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.560	12.70	14.22	3
P	0.075	-	1.91	-	5

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AF outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inches (0.254mm).
6. Lead no. 3 butt welded to stem base.
7. Controlling dimension: Inch.
8. Revision 3 dated 6-94.



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CoolFET <sup>TM</sup>	FRFET <sup>TM</sup>	POP <sup>TM</sup>	SuperSOT <sup>TM</sup> -3
CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	Power247 <sup>TM</sup>	SuperSOT <sup>TM</sup> -6
DenseTrench <sup>TM</sup>	GTO <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8
DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	QFET <sup>TM</sup>	SyncFET <sup>TM</sup>
EcoSPARK <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	QS <sup>TM</sup>	TinyLogic <sup>TM</sup>
E <sup>2</sup> CMOS <sup>TM</sup>	LittleFET <sup>TM</sup>	QTOptelectronics <sup>TM</sup>	TruTranslation <sup>TM</sup>
Ensigna <sup>TM</sup>	MicroFET <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>
FACT <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENTSWITCHER <sup>®</sup>	UltraFET <sup>®</sup>
FACT Quiet Series <sup>TM</sup>	OPTOLOGIC <sup>TM</sup>	SMART START <sup>TM</sup>	VCX <sup>TM</sup>

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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