FAIRCHILD SEMICONDUCTOR®

January 2014

FSQ510 / FSQ510MX
Green Mode Fairchild Power Switch (FPS™)
for Valley Switching Converter – *Low EMI and High Efficiency*

Features

- Uses an LDMOS Integrated Power Switch
- Optimized for Valley Switching Converter (VSC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High Efficiency through Minimum Drain Voltage Switching
- Extended Valley Switching for Wide Load Ranges
- Small Frequency Variation for Wide Load Ranges
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Protection Functions: Overload Protection (OLP), Internal Thermal Shutdown (TSD) with Hysteresis
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Startup Circuit
- Internal High-Voltage SenseFET: 700 V
- Built-in Soft-Start: 5 ms

Applications

- Auxiliary Power Supplies for LCD TV, LCD Monitor, Personal Computer, and White Goods

Description

A Valley Switching Converter (VSC) generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ510 is an integrated Valley Switching Pulse Width Modulation (VS-PWM) controller and SenseFET specifically designed for offline Switch-Mode Power Supplies (SMPS) for valley switching with minimal external components. The VS-PWM controller includes an integrated oscillator, under-voltage lockout (UVLO), leading-edge blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry.

Compared with discrete MOSFET and PWM controller solutions, the FSQ510 can reduce total cost, component count, size and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a platform for cost-effective designs of a valley switching flyback converters.

Ordering Information

Part Number	Package	Operating Junction Temperature	Current Limit	$R_{DS(ON)}$ (Max.)	Output Power Table[1]				Packing Method
					230 V_{AC} ± 15%[2]		85-265 V_{AC}		
					Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]	
FSQ510	7-DIP	-40 to +130°C	320 mA	32 Ω	5.5 W	9 W	4 W	6 W	Rail
FSQ510MX	7-MLSOP								Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Notes:

1. The junction temperature can limit the maximum output power.
2. 230 V_{AC} or 100/115 V_{AC} with voltage doubler.
3. Typical continuous power with a Fairchild charger evaluation board described in this datasheet in a non-ventilated, enclosed adapter housing, measured at 50°C ambient temperature.
4. Maximum practical continuous power for auxiliary power supplies in an open-frame design at 50°C ambient temperature.

Application Circuit

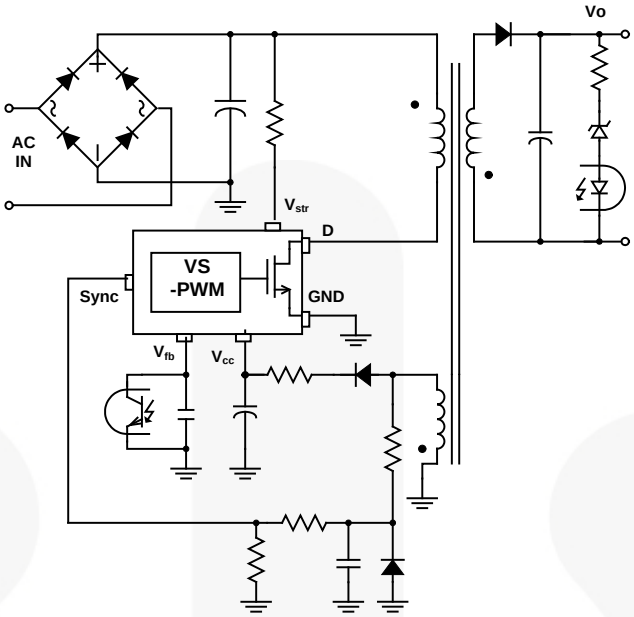


Figure 1. Typical Application Circuit

Internal Block Diagram

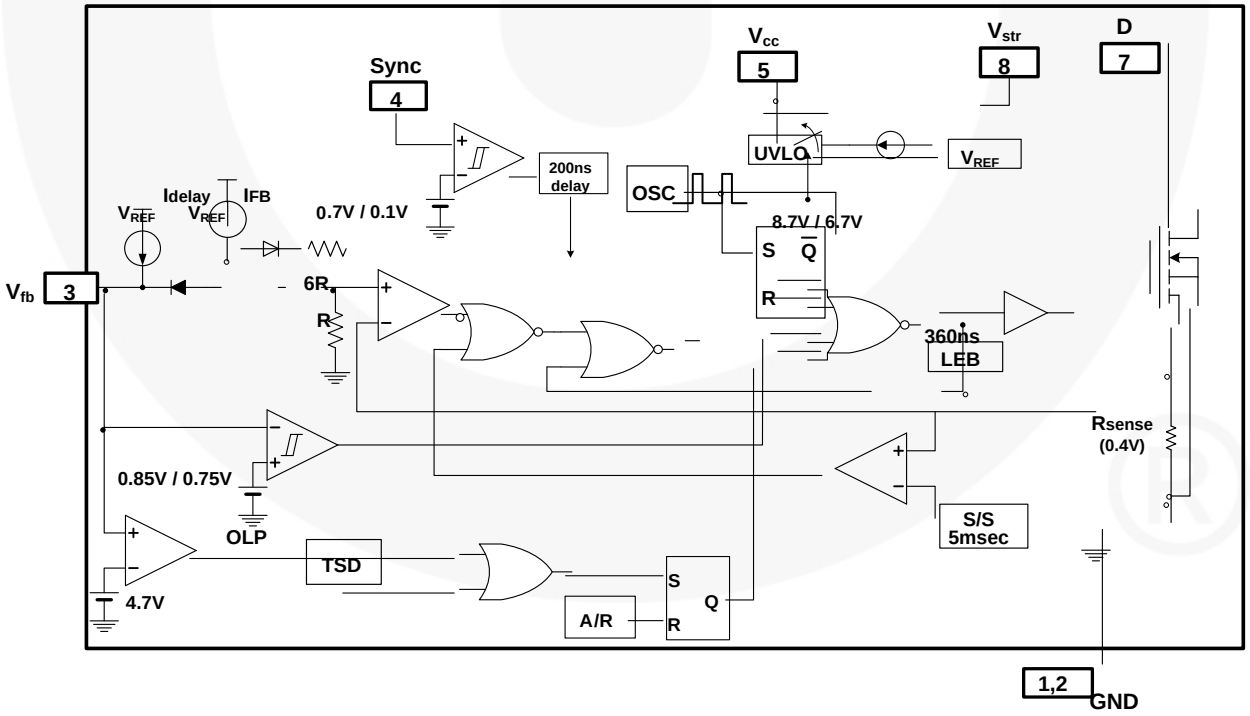


Figure 2. Internal Block Diagram

Pin Configuration

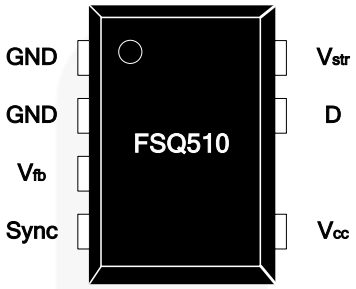


Figure 3. Pin Assignments

Pin Definitions

Pin #	Name	Description
1, 2	GND	This pin is the control ground and the SenseFET source.
3	V_{fb}	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 4.7 V, the overload protection triggers, which shuts down the FPS.
4	Sync	This pin is internally connected to the sync-detect comparator for valley switching. In normal valley-switching operation, the threshold of the sync comparator is 0.7 V/0.1 V.
5	V_{CC}	This pin is the positive supply input. This pin provides internal operating current for both startup and steady-state operation.
7	D	High-voltage power SenseFET drain connection.
8	V_{str}	This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 8.7 V, the internal current source is disabled.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{STR}	V_{str} Pin Voltage			500	V
V_{DS}	Drain Pin Voltage			700	V
V_{CC}	Supply Voltage			20	V
V_{FB}	Feedback Voltage Range		-0.3	Internally Clamped[5]	V
V_{Sync}	Sync Pin Voltage		-0.3	6.5	V
P_D	Total Power Dissipation	7-DIP		1.38	W
		7-MLSOP			
T_J	Maximum Junction Temperature			+150	°C
	Recommended Operating Junction Temperature[6]		-40	+140	
T_{STG}	Storage Temperature		-55	+150	°C

Notes:

5. V_{FB} is internally clamped at 6.5 V (I_{CLAMP_MAX}<100 μA) which has a tolerance between 6.2 V and 7.2 V.
6. The maximum value of the recommended operating junction temperature is limited by thermal shutdown.

Thermal Impedance

T_A=25°C unless otherwise specified. Items are tested with the standards JESD 51-2 and 51-10 (DIP).

Symbol	Parameter	Value	Unit
7-DIP, 7-MLSOP			
θ_{JA}	Junction-to-Ambient Thermal Impedance[7]	90	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance[8]	13	°C/W

Notes:

7. Free-standing with no heatsink; without copper clad; measurement condition - just before junction temperature T_J enters into TSD.
8. Measured on the DRAIN pin close to plastic interface.

Electrical Characteristics

T_J=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CC}=0 V, I_D=100 μA	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{DS}=700 V			150	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	T_J=25°C, I_D=180 mA		28	32	Ω
		T_J=100°C, I_D=180 mA		42	48	Ω
C_{ISS}	Input Capacitance[9]	V_{GS}=11 V		96		pF
C_{OSS}	Output Capacitance[9]	V_{DS}=40 V		28		pF
t_r	Rise Time[9]	V_{DS}=350 V, I_D=25 mA		100		ns
t_f	Fall Time[9]	V_{DS}=350 V, I_D=25 mA		50		ns
Control Section						
f_S	Initial Switching Frequency	V_{CC}=11 V, V_{FB}=5 V, V_{sync}=0 V	87.7	94.3	100.0	kHz
Δf_S	Switching Frequency Variation[9]	-25°C < T_J < 125°C		±5	±8	%
I_{FB}	Feedback Source Current	V_{CC}=11 V, V_{FB}=0 V	200	225	250	μA
t_B	Switching Blanking Time	V_{CC}=11 V, V_{FB}=1 V, V_{sync} Frequency Sweep	7.2	7.6	8.2	μs
t_W	Valley Detection Window Time[9]			3.0		μs
D_{MAX}	Maximum Duty Ratio	V_{CC}=11 V, V_{FB}=3 V	54	60	66	%
D_{MIN}	Minimum Duty Ratio	V_{CC}=11 V, V_{FB}=0 V			0	%
V_{START}	UVLO Threshold Voltage	V_{FB}=0 V, V_{CC} Sweep	8.0	8.7	9.4	V
V_{STOP}		After Turn-on, V_{FB}=0 V	6.0	6.7	7.4	V
$t_{S/S}$	Internal Soft-Start Time	V_{STR}=40 V, V_{CC} Sweep	3	5	7	ms
Burst-Mode Section						
V_{BURH}	Burst-Mode Voltage	V_{CC}=11 V, V_{FB} Sweep	0.75	0.85	0.95	V
V_{BURL}			0.65	0.75	0.85	V
HYS				100		mV
Protection Section						
I_{LIM}	Peak Current Limit	di/dt=90 mA/μs	280	320	360	mA
V_{SD}	Shutdown Feedback Voltage	V_{DS}=40 V, V_{CC}=11 V, V_{FB} Sweep	4.2	4.7	5.2	V
I_{DELAY}	Shutdown Delay Current	V_{CC}=11 V, V_{FB}=5 V	3.5	4.5	5.5	μA
t_{LEB}	Leading-Edge Blanking Time[9]			360		ns
T_{SD}	Thermal Shutdown Temperature[9]		130	140	150	°C
HYS				60		°C
Synchronous Section						
V_{SH}	Synchronous Threshold Voltage	V_{CC}=11 V, V_{FB}=1 V	0.55	0.70	0.85	V
V_{SL}		V_{CC}=11 V, V_{FB}=1 V	0.05	0.10	0.15	V
t_{Sync}	Synchronous Delay Time		180	200	220	ns
Total Device Section						
I_{OP}	Operating Supply Current (Control Part Only)	V_{CC}=11 V, V_{FB}=5.5 V		0.8	1.0	mA
I_{CH}	Startup Charging Current	V_{CC}=V_{FB}=0 V,V_{STR}=40 V		1.0	1.2	mA
V_{STR}	Supply Voltage	V_{CC}=V_{FB}=0 V, V_{STR} Sweep		27		V

Note:

9. These parameters, although guaranteed, are not 100% tested in production.

Comparison between FSD210B and FSQ510

Function	FSD210B	FSQ510	Advantages of FSQ510
Control Mode	Voltage Mode	Current Mode	Fast Response Easy-to-Design Control Loop
Operation Method	Constant Frequency PWM	Valley Switching Operation	Turn-on at Minimum Drain Voltage High Efficiency and Low EMI
EMI Reduction Method	Frequency Modulation	Valley Switching	Frequency Variation Depending on the Ripple of DC Link Voltage High Efficiency and Low EMI
Soft-Start	3 ms (Built-in)	5ms (Built-in)	Longer Soft-Start Time
Protection	TSD	TSD with Hysteresis	Enhanced Thermal Shutdown Protection
Power Balance	Long T_{CLD}	Short T_{CLD}	Small Difference of Input Power between the Low and High Input Voltage Cases
Power Ratings	Less than 5 W Under Open-Frame Condition at the Universal Line Input	More than 6 W Under Open-Frame Condition at the Universal Line Input	More Output Power Rating Available due to the Valley Switching

Typical Performance Characteristics

Characteristic graphs are normalized at T_A=25°C.

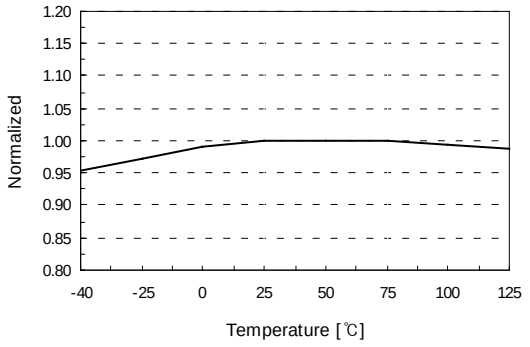


Figure 4. Operating Frequency (f_{OSC}) vs. T_A

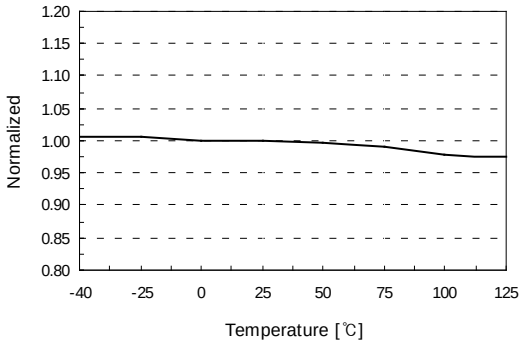


Figure 5. Peak Current Limit (I_{LIM}) vs. T_A

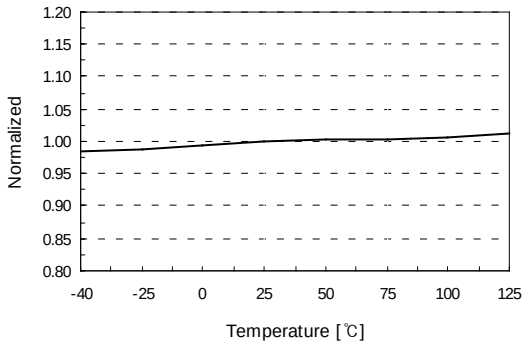


Figure 6. Start Threshold Voltage (V_{START}) vs. T_A

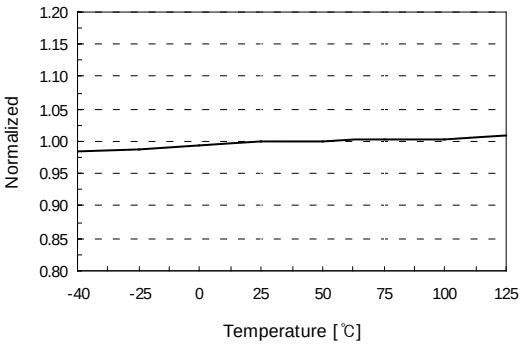


Figure 7. Stop Threshold Voltage (V_{STOP}) vs. T_A

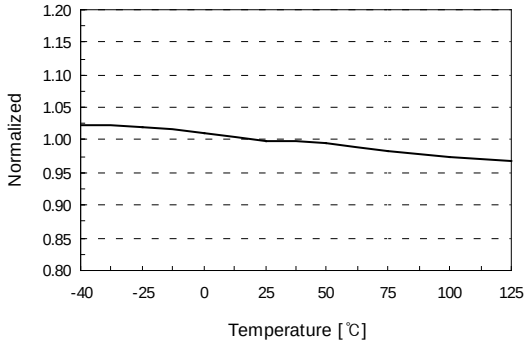


Figure 8. Shutdown Feedback Voltage (V_{SD}) vs. T_A

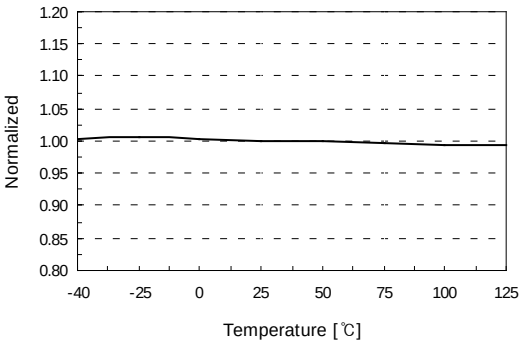


Figure 9. Maximum Duty Cycle (D_{MAX}) vs. T_A

Typical Performance Characteristics (Continued)

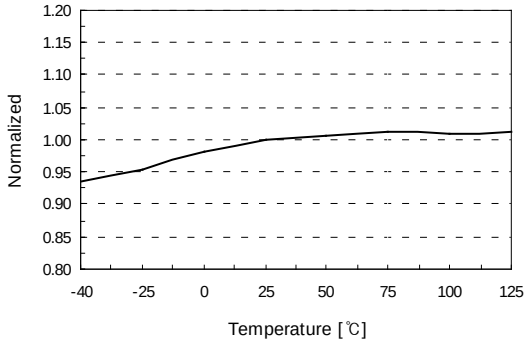


Figure 10. Feedback Source Current (I_{FB}) vs. T_A

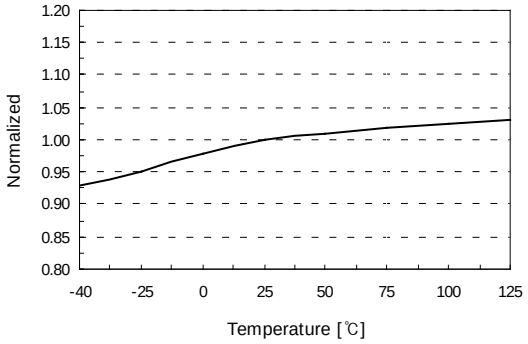


Figure 11. Shutdown Delay Current (I_{DELAY}) vs. T_A

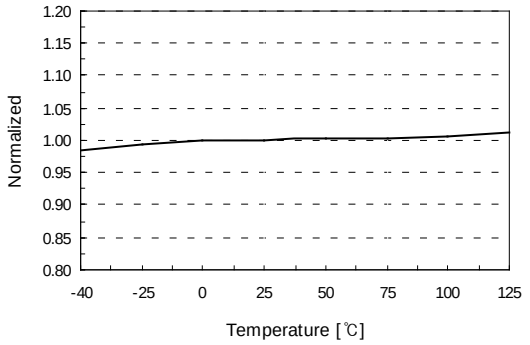


Figure 12. Operating Supply Current (I_{OP}) vs. T_A

Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 13. When V_{CC} reaches 8.7 V, the FPS begins switching and the internal high-voltage current source is disabled. The FPS continues normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 6.7 V.

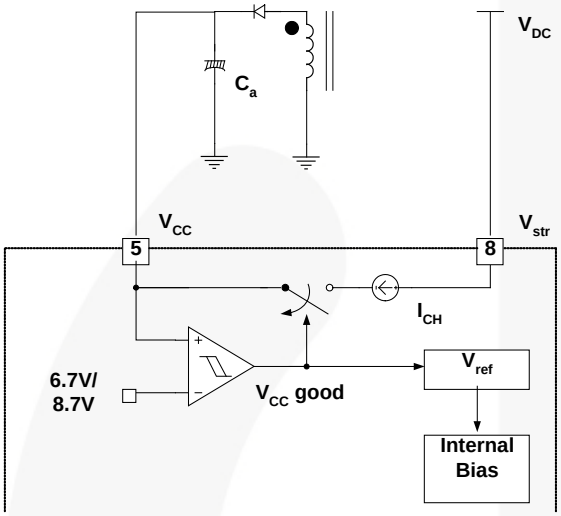


Figure 13. Startup Block

2. Feedback Control: This device employs current-mode control, as shown in Figure 14. An opto-coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5 V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the drain current. This typically occurs when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-Pulse Current Limit: Because current-mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 14. Assuming that the 225 µA current source flows only through the internal resistor (6R + R=12.6kΩ), the cathode voltage of diode D2 is about 2.8 V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.8 V, the maximum voltage of the cathode of D2 is clamped at this voltage, clamping V_{FB}*. Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode VS-PWM control. To counter this effect, the FPS employs a leading-edge blanking (LEB) circuit to inhibit the VS-PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

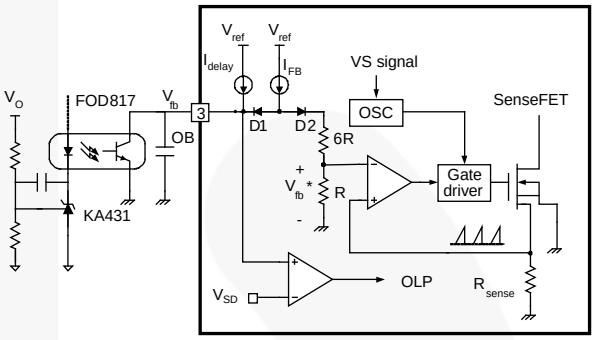


Figure 14. Valley Switching Pulse-Width Modulation (VS-PWM) Circuit

3. Synchronization: The FSQ510 employs a valley-switching technique to minimize the switching noise and loss. The basic waveforms of the valley switching converter are shown in Figure 15. To minimize the MOSFET switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, as shown in Figure 15. The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 15.

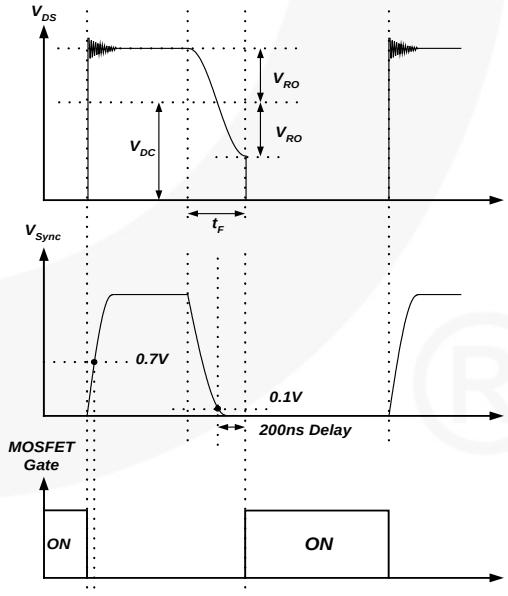


Figure 15. Valley Switching Waveforms

4. Protection Circuits: The FSQ510 has two self-protective functions, overload protection (OLP) and thermal shutdown (TSD). The protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the under-voltage lockout (UVLO) stop voltage of 6.7 V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 8.7 V, the FSQ510 resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, reliability is improved without increasing cost.

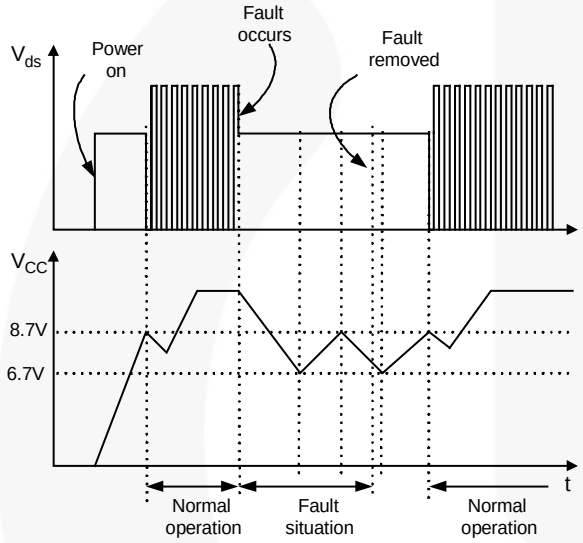


Figure 16. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_o) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.8 V, D1 is blocked and the 5 µA current source starts to charge C_B slowly up. In this condition, V_{FB} continues increasing until it reaches 4.7 V, when the switching operation is terminated, as shown in Figure 17. The delay time for shutdown is the time required to charge C_B from 2.8 V to 4.7 V with 5 µA. A 20 ~ 50 ms delay time is typical for most applications. This protection is implemented in auto-restart mode.

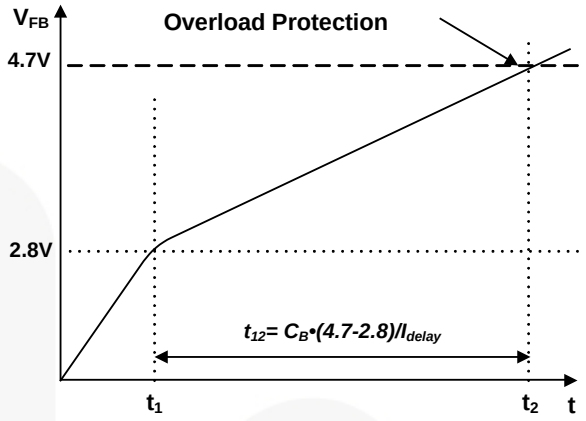


Figure 17. Overload Protection

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package make it easy for the control IC to detect the abnormal over temperature of the SenseFET. If the temperature exceeds approximately 140°C, the thermal shutdown triggers and the FPS stops operation. The FPS operates in auto-restart mode until the temperature decreases to around 80°C, when normal operation resumes.

5. Soft-Start: The FPS has an internal soft-start circuit that increases the VS-PWM comparator inverting input voltage, together with the SenseFET current, slowly after it starts up. The typical soft-start time is 5 ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup.

6. Burst-Mode Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 18, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (750 mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (850 mV), switching resumes. The feedback voltage then falls and the process repeats. Burst mode alternately enables and disables switching of the SenseFET, reducing switching loss in standby mode.

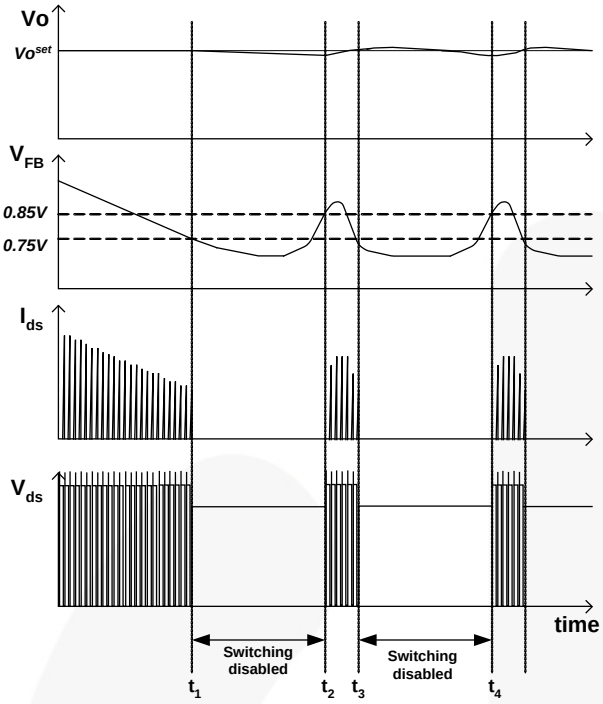


Figure 18. Burst-Mode Operation

7. Advanced Valley Switching Operation: To minimize switching loss and Electromagnetic Interference (EMI), the MOSFET turns on when the drain voltage reaches its minimum value in VS converters. Due to the Discontinuous Conduction Mode (DCM) operation, the feedback voltage is not changed, despite the DC link voltage ripples, if the load condition is not changed. Since the slope of the drain current is changed depending on the DC link voltage, the turn-on duration of MOSFET is variable with the DC link voltage ripples. The switching period is changed continuously with the DC link voltage ripples. Not only the switching at the instant of the minimum drain voltage, but also the continuous change of the switching period, reduces EMI. V_S converters inherently scatter the EMI spectrum.

Typical products for VSC turn the MOSFET on when the first valley is detected. In this case, the range of the switching frequency is very wide as a result of the load variations. At a very light-load, for example, the switching frequency can be as high as several hundred kHz. Some products for VSC, such as Fairchild's FSCQ-series, define the turn-on instant of SenseFET change at the first valley into at the second valley, when the load condition decreases under its predetermined level. The range of switching frequency narrows somewhat. For details, consult an FSCQ-series datasheet, such as:

http://www.fairchildsemi.com/pf/FS/FSCQ1265RT.html

The range of the switching frequency can be limited tightly in FSQ-series. Because a kind of blanking time (t_B) is adopted, as shown in Figure 19, the switching frequency has minimum and maximum values.

Once the SenseFET is enabled, the next start is prohibited during the blanking time (t_B). After the blanking time, the controller finds the first valley within the duration of the valley detection window time (t_W) (case A, B, and C). If no valley is found in t_W, the internal SenseFET is forced to turn on at the end of t_W (case D). Therefore, FSQ510 has minimum switching frequency of 94.3 kHz and maximum switching frequency of 132 kHz, typically, as shown in Figure 20.

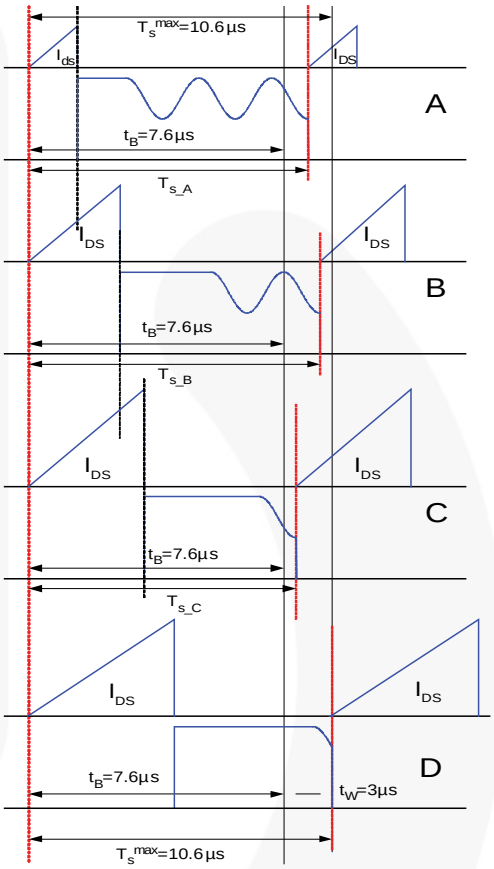


Figure 19. Advanced VS Operation

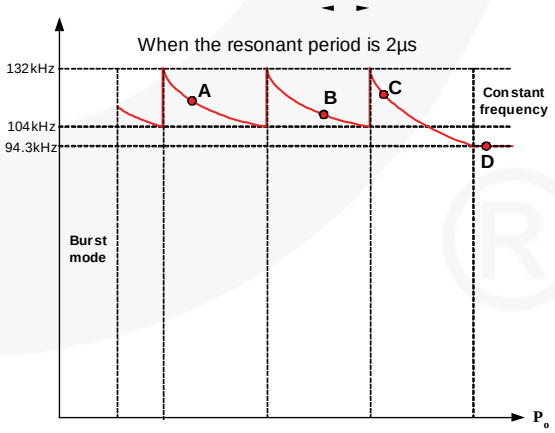
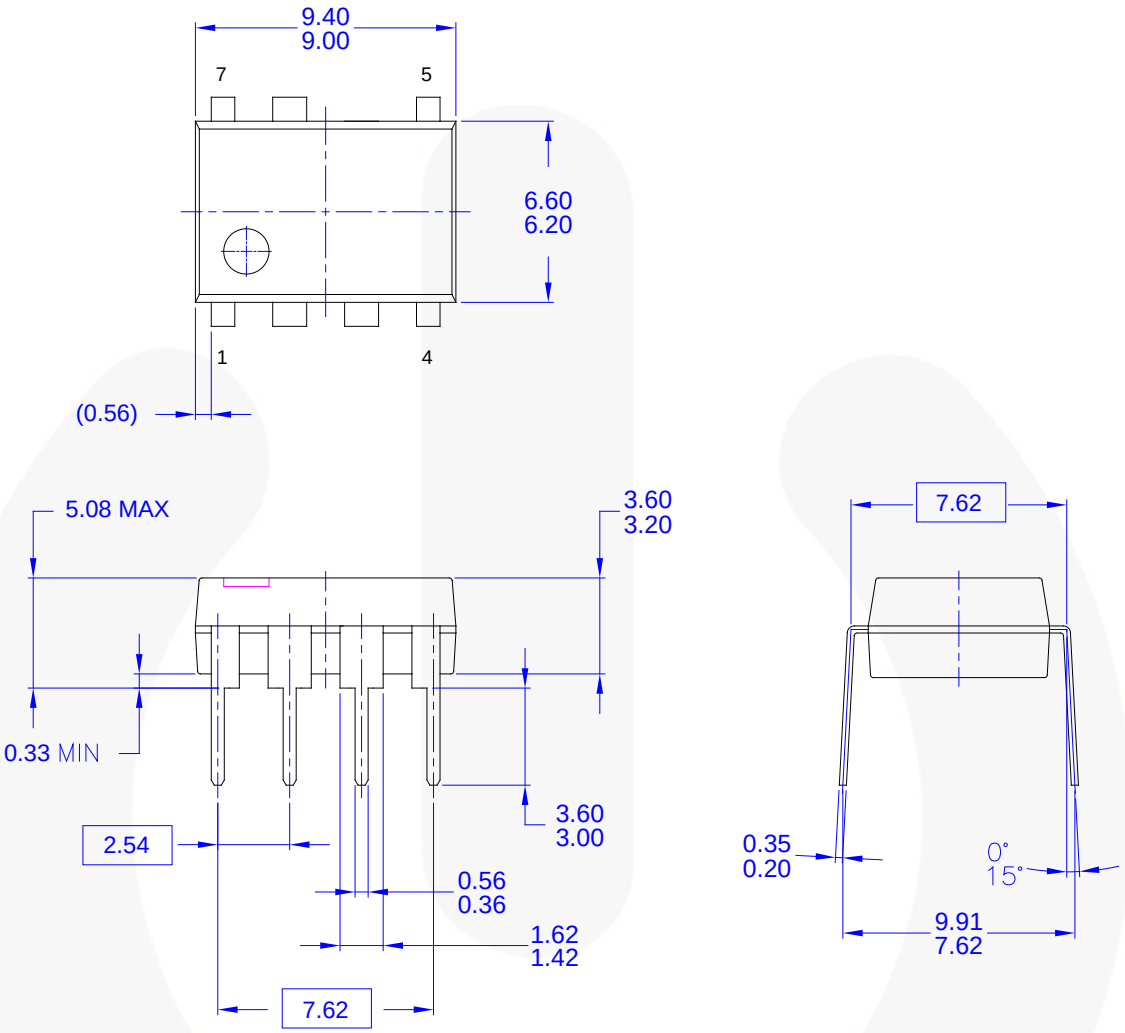


Figure 20. Switching Frequency Range of the Advanced Valley Switching

Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE COMPLIES TO JEDEC MS-001, VARIATION BA, EXCEPT FOR TERMINAL COUNT (7 RATHER THAN 8)

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVISION: MKT-NA07BREV2

Figure 21. 7-Lead, Dual In-line Package (DIP)

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Package Dimensions (Continued)

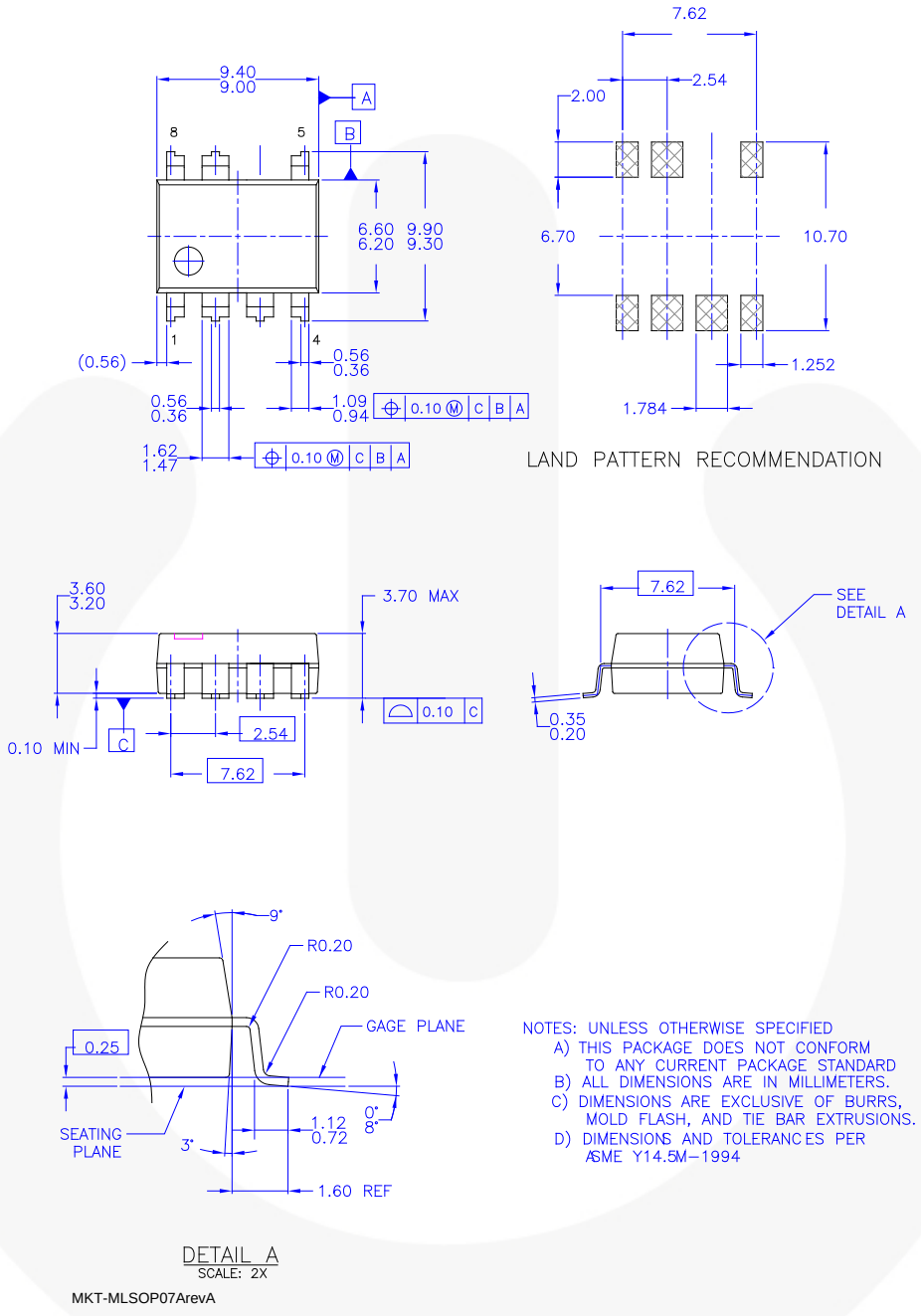

Figure 22. 7-Lead, MLSOP

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