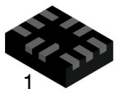
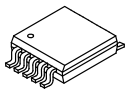
Low-Power, Two-Port, High-Speed, USB2.0 (480 Mbps) UART Switch

FSUSB42



UQFN10 1.4 × 1.8, 0.4 P
CASE 523BC



MSOP10
CASE 846AP

Description

The FSUSB42 is a bi−directional, low−power, two−port, high−speed, USB2.0 switch. Configured as a double−pole, double−throw switch (DPDT) switch, it is optimized for switching between any combination of high−speed (480 Mbps) or Full−Speed (12 Mbps) sources.

The FSUSB42 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (CON) of 3.7 pF. The wide bandwidth of this device (720 MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel−to−channel crosstalk also minimizes interference.

The FSUSB42 contains special circuitry on the switch I/O pins for applications w here the V_{CC} supply is powered−of f (V_{CC} = 0 V), which allow s the device to withstand an over−voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the SEL pin is low er than the supply voltage (V_{CC}). This feature is especially valuable to ultra−portable applications, such as cell phones, allowing for direct interface with the general−purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

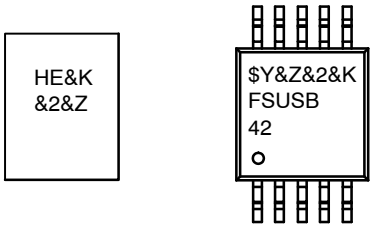
Features

- Low On Capacitance: 3.7 pF Typical
- Low On Resistance: 3.9 Ω Typical
- Low Pow er Consumption: 1 μA Maximum
  - 15 μA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN} = 1.8 V, V_{CC} = 4.4 V)
- Wide −3 db Bandwidth: > 720 MHz
- Packaged in:
  - 10−Lead UMLP (1.4 x 1.8 mm)
  - 10−Lead MSOP
- 8 kV ESD Rating, >16 kV Power / GND ESD Rating
- Over−Voltage Tolerance (OVT) On All USB Ports Up to 5.25 V without External Components

Typical Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set−Top Box

MARKING DIAGRAMS



HE, FSUCB42	= Specific Device Code
$Y	= **onsemi** Logo
&K	= 2 Digit Lot Run Traceability Code
&2	= 2−Digit Date Code
&Z	= Assembly Location

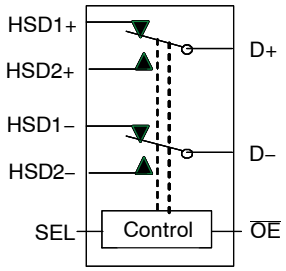


Figure 1. Analog Symbol

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

Pin Assignments

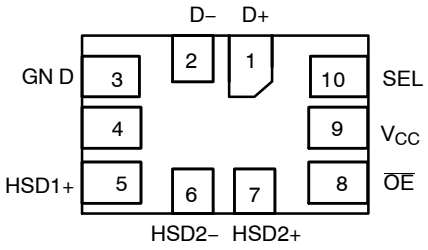


Figure 2. 10−Lead UMLP (Top−Through View)

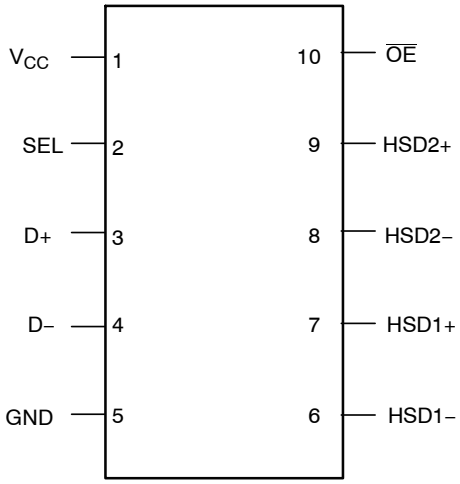


Figure 3. 10−Lead MSOP (Top−Through View)

PIN DESCRIPTION

UMLP Pin#	MSOP Pin#	Name	Description
1	3	D+	Common USB Data Bus
2	4	D−	Common USB Data Bus
3	5	GND	Ground
4	6	HSD1−	Multiplexed Source Input 1
5	7	HSD1+	Multiplexed Source Input 1
6	8	HSD2−	Multiplexed Source Input 2
7	9	HSD2+	Multiplexed Source Input 2
8	10	$\overline{OE}$	Switch Enable
9	1	V_{CC}	Supply Voltage
10	2	SEL	Switch Select

TRUTH TABLE

SEL	$\overline{OE}$	Function
X	HIGH	Disconnect
LOW	LOW	D+ = HSD1+, D− = HSD1−
HIGH	LOW	D+ = HSD2+, D− = HSD2−

1. LOW ≤ V_{IL}.
2. HIGH ≤ V_{IH}.
3. X = Don't Care.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	5.6	V
V_{CNTRL}	DC Input Voltage (S, $\overline{OE}$) (Note 4)		−0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage (Note 4) (VCC = 0 V)		−0.50	5.25	V
I_{IK}	DC Input Diode Current		−50	–	mA
I_{OUT}	DC Output Current		–	100	mA
T_{STG}	Storage Temperature		−65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J−STD−020A)		–	1	Level
ESD	Human Body Model, JEDEC: JESD22−A114	All Pins	7	–	kV
		I/O GND	8	–	
		Power to GND	16	–	
		D+/D−	9	–	
	IEC 61000−4−2 System on USB Connector Pins D+ & D−	Air Discharge	15	–	
		Contact	8	–	
	Charged Device Model, JEDEC: JESD22−C101		2	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2.4	4.4	V
V_{CNTRL}	Control Input Voltage (S, $\overline{OE}$) (Note 5)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	−0.5	4.5	V
T_A	Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. The control input must be held HIGH or LOW and it must not float.

DC ELECTRICAL CHARACTERISTICS

(All typical value are at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
V_{IK}	Clamp Diode Voltage	I_{IN} = 18 mA	3.0	–	–	−1.2	V
V_{IH}	Input Voltage High		2.4 to 3.6	1.3	–	–	V
			4.3	1.7	–	–	
V_{IL}	Input Voltage Low		2.4 to 3.6	–	–	0.5	V
			4.3	–	–	0.7	
I_{IN}	Control Input Leakage	V_{SW} = 0 to V_{CC}	0 to 4.3	−1	–	1	μA
I_{OZ}	Off State Leakage	0 ≤ Dn, HSD1n, HSD2n ≤ 3.6 V	4.3	−2	–	2	μA
I_{OFF}	Power−Off Leakage Current (All I/O Ports)	V_{SW} = 0 V to 4.3 V, V_{CC} = 0 V Figure 5	0	−2	–	2	μA
R_{ON}	HS Switch On Resistance (Note 6)	V_{SW} = 0.4 V, I_{ON} =8 mA Figure 4	2.4	–	4.5	7.5	Ω
			3.0	–	3.9	6.5	
ΔR_{ON}	HS Delta R_{ON} (Note 7)	V_{SW} = 0.4, I_{ON} = 8 mA	3.0	–	0.65	–	Ω
I_{CC}	Quiescent Supply Current	V_{CNTRL} = 0 or V_{CC}, I_{OUT} = 0	4.3	–	–	1	μA

DC ELECTRICAL CHARACTERISTICS (continued)

(All typical value are at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
I_{CCT}	Increase in I_{CC} Current per Control Voltage and V_{CC}	V_{CNTRL} = 2.6, V_{CC} = 4.3 V	4.3	–	–	10	μA
		V_{CNTRL} = 1.8, V_{CC} = 4.3 V	4.3		–	15	μA

6. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
7. Guaranteed by characterization.

AC ELECTRICAL CHARACTERISTICS

(All typical value are for V_{CC} = 3.3 V at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
t_{ON}	Turn−On Time S, $\overline{OE}$ to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 0.8 V, Figure 6, Figure 7	2.4	–	24	40	ns
			3.0 to 3.6	–	13	30	
t_{OFF}	Turn−Off Time S, $\overline{OE}$ to Output	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 0.8 V, Figure 6, Figure 7	2.4	–	15	35	ns
			3.0 to 3.6	–	12	25	
t_{PD}	Propagation Delay (Note 8)	C_L = 5 pF, R_L = 50 Ω, Figure 6, Figure 8	3.3	–	0.25	–	ns
t_{BBM}	Break−Before−Make	R_L = 50 Ω, C_L = 5 pF, V_{SW1} = V_{SW2} = 0.8 V, Figure 10	2.4	2.0	–	10	ns
			3.0 to 3.6	2.0	–	6.5	
O_{IRR}	Off Isolation	R_L = 50 Ω, f = 240 MHz, Figure 12	3.0 to 3.6	–	−30	–	dB
Xtalk	Non−Adjacent Channel Crosstalk	R_L = 50 Ω, f = 240 MHz, Figure 13	3.0 to 3.6	–	−45	–	dB
BW	−3 db Band Width	R_L = 50 Ω, C_L = 0 pF, Figure 11	3.0 to 3.6	–	720	–	MHz
		R_L = 50 Ω, C_L = 5 pF, Figure 11		–	550	–	MHz

8. Guaranteed by characterization.

USB HIGH−SPEED−RELATED AC ELECTRICAL CHARACTERISTICS

(All typical value are for V_{CC} = 3.3 V at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
$t_{SK(P)}$	Skew of Opposite Transition of the Same Output (Note 9)	C_L = 5 pF, R_L = 50 Ω, Figure 9	–	–	20	–	ps
t_J	Total Jitter (Note 9)	R_L = 50 Ω, C_L = 5 pF, t_R = t_F = 500 ps (10−90%) at 480 Mbps (PRBS = 2^{15} − 1)	–	–	200	–	ps

9. Guaranteed by characterization.

CAPACITANCE

Symbol	Parameter	Condition	T_A = −40°C to +85°C			Unit
			Min	Typ	Max	
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0 V	–	1.5	–	pF
C_{ON}	D+/D− On Capacitance	V_{CC} = 3.3 V, $\overline{OE}$ = 0 V, f = 240 MHz, Figure 15	–	3.7	–	pF
C_{OFF}	D1n, D2n Off Capacitance	V_{CC} and $\overline{OE}$ = 3.3 V, Figure 14	–	2.0	–	pF

Test Diagrams

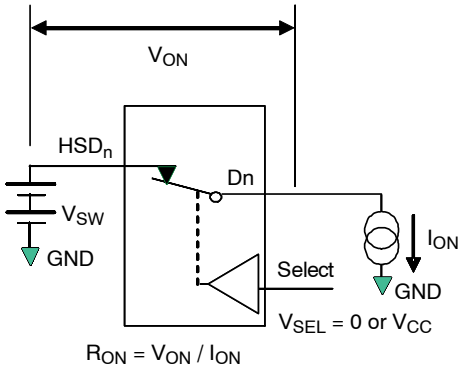
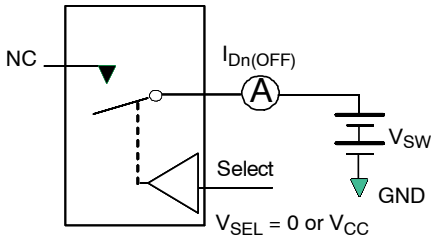
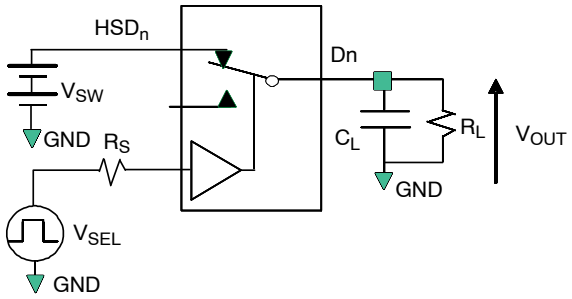


Figure 4. On Resistance



**Each switch port is tested separately

Figure 5. Off Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 6. AC Test Circuit Load

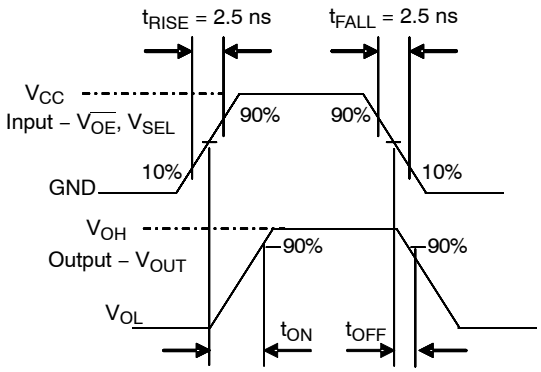


Figure 7. Turn−On / Turn−Off Waveforms

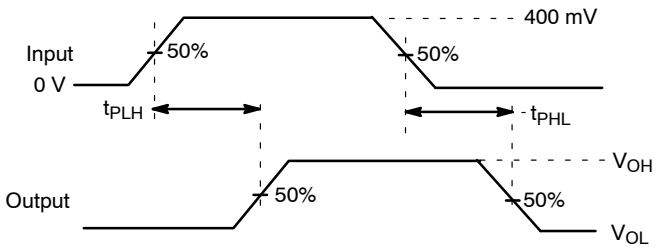


Figure 8. Propagation Delay ($t_R t_F$ − 500 ps)

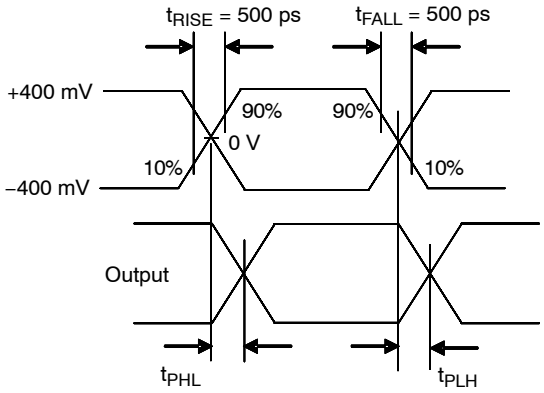


Figure 9. Intra-Pair Skew Test $t_{SK(P)}$

Test Diagrams (continued)

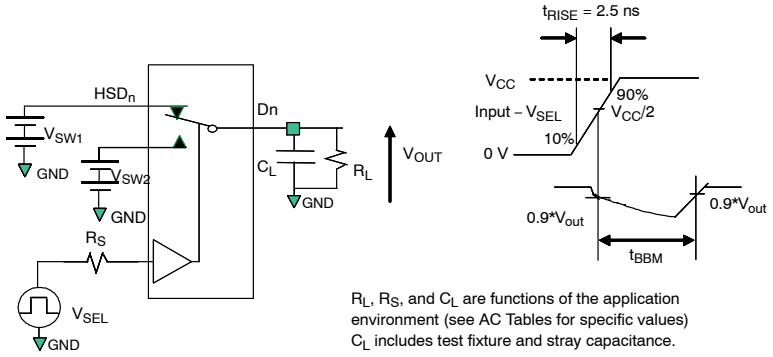


Figure 10. Break−Before−Make Interval Timing

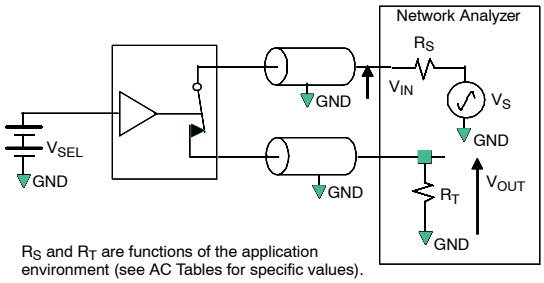


Figure 11. Bandwidth

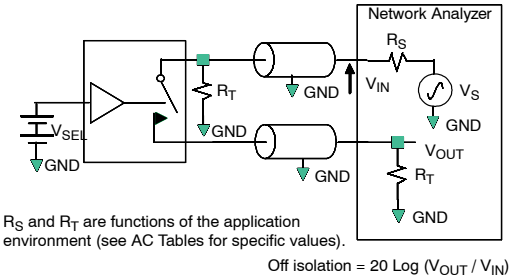


Figure 12. Channel Off Isolation

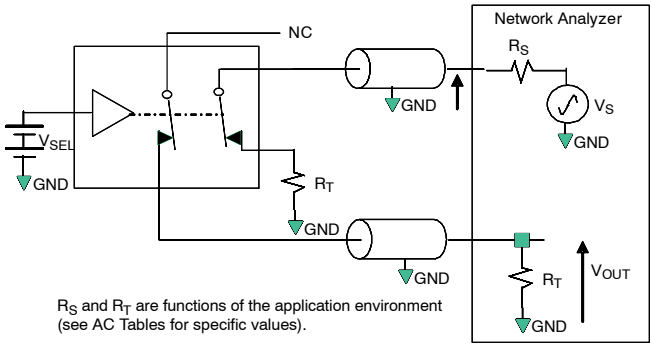


Figure 13. Non-Adjacent Channel-to-Channel Crosstalk

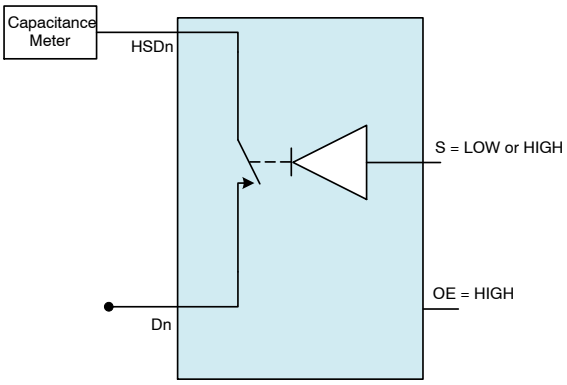


Figure 14. Channel Off Capacitance

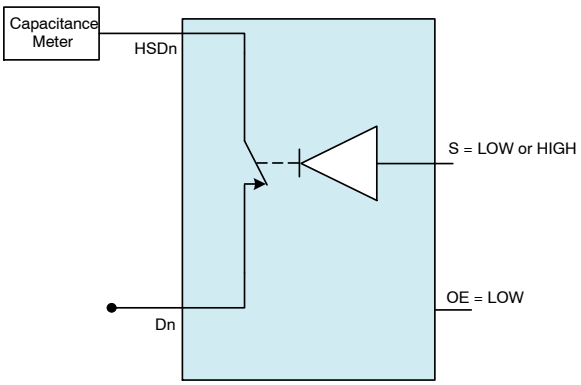
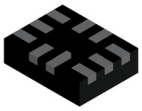


Figure 15. Channel On Capacitance

ORDERING INFORMATION

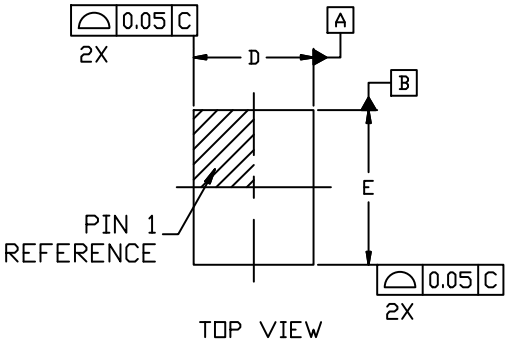
Part Number	Device Code	Operating Temperature Range	Package	Shipping†
FSUSB42UMX	HE	−40 to 85°C	10−Lead, Quad, Ultrathin Molded Leadless Package (UQFN10), 1.4 × 1.8 mm	5000 / Tape and Reel
FSUSB42MUX	FSUSB42	−40 to 85°C	10−Lead, Molded Small−Outline Package (MSOP) JEDEC MO−187, 3.0 mm Wide	4000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

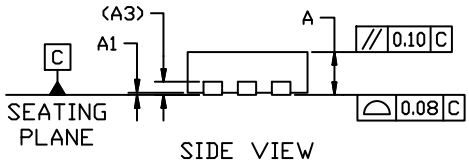


UQFN10 1.4x1.8, 0.4P
CASE 523BC
ISSUE B

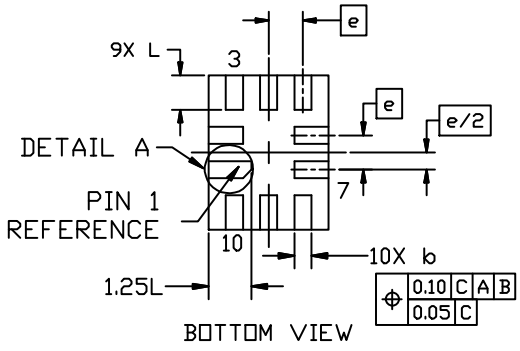
DATE 13 MAY 2022



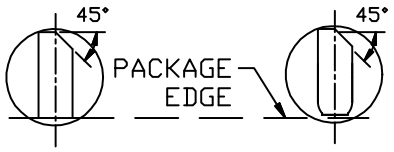
TOP VIEW



SIDE VIEW



BOTTOM VIEW



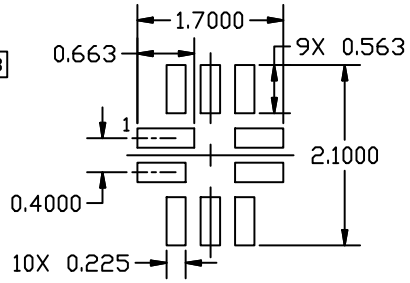
DETAIL A

OPTIONAL CONSTRUCTIONS

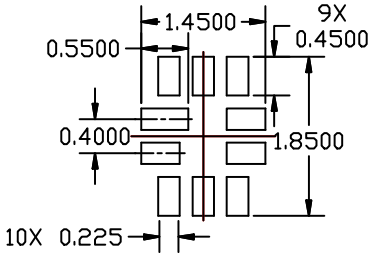
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2018
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	0.025	0.05
A3	0.152 REF		
b	0.15	0.20	0.25
D	1.35	1.40	1.45
E	1.75	1.80	1.85
e	0.40 BSC		
L	0.35	0.40	0.45



RECOMMENDED LAND PATTERN



OPTIONAL MINIMIAL TOE LAND PATTERN

RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

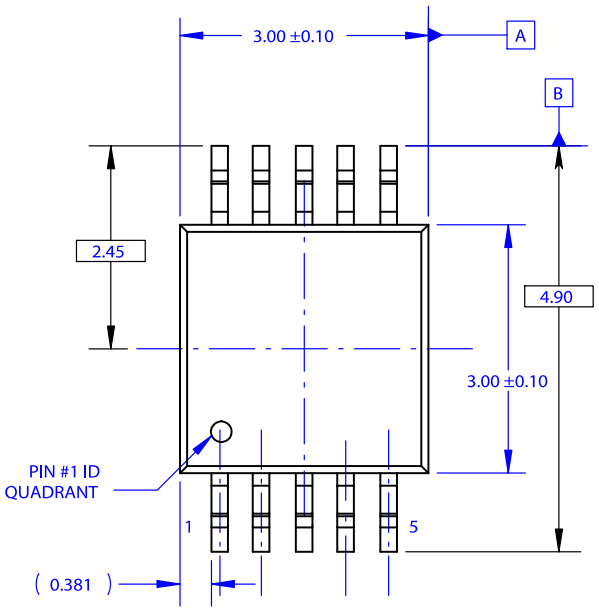
DOCUMENT NUMBER:	**98AON13705G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**UQFN10 1.4x1.8, 0.4P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

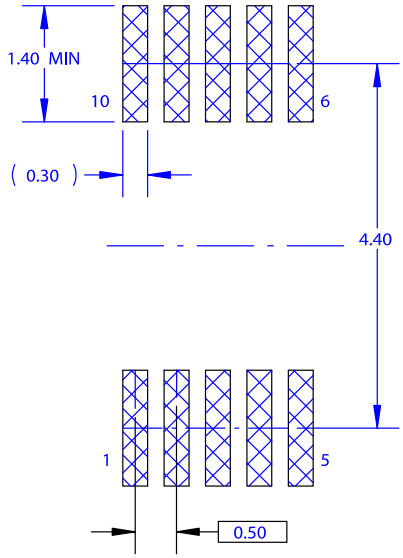
ON Semiconductor®

MSOP10
CASE 846AP
ISSUE O

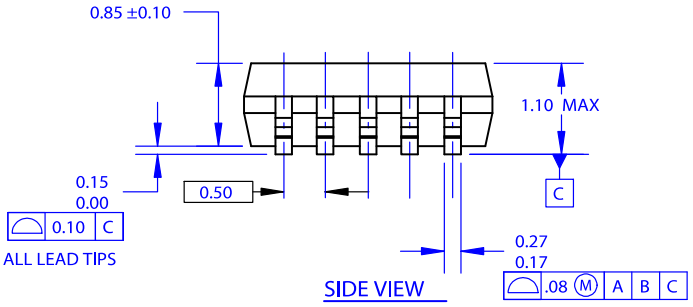
DATE 31 JAN 2017



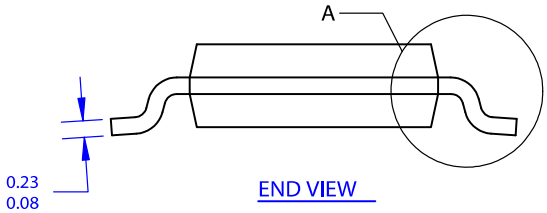
TOP VIEW



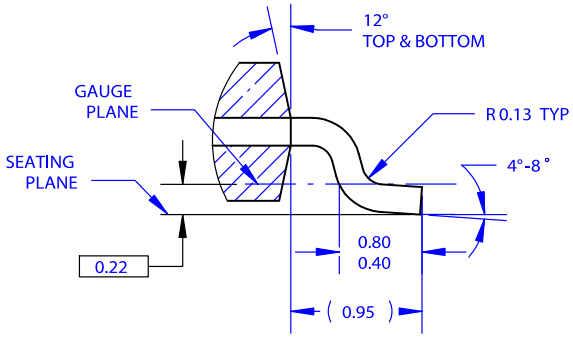
LAND PATTERN RECOMMENDATION



SIDE VIEW



END VIEW



DETAIL A
SCALE 20 : 1

NOTES: UNLESS OTHERWISE SPECIFIED

A. THIS PACKAGE CONFORMS TO JEDEC MO-187 VARIATION BA.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES AS PER ASME Y14.5-1994.
E. LAND PATTERN AS PER IPC7351#SOP50P490X110-10AN

DOCUMENT NUMBER:	**98AON13758G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**MSOP10**		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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