FSVP532

Standard multi-protocol reader IC

Rev. 1.0 — 18 September 2017 **Product data sheet**

1.General description

The FSVP532 is a highly integrated transceiver module for contactless communication at 13.56 MHz based on the 80C51 microcontroller core. It supports 6 different operating modes:

- PIN2PIN compatiable PN532
- ISO/IEC 14443A/MIFARE Reader/Writer
- FeliCa Reader/Writer
- ISO/IEC 14443B Reader/Writer
- ISO/IEC 14443A/MIFARE Card MIFARE Classic 1K or MIFARE Classic 4K card emulation mode
- FeliCa Card emulation
- ISO/IEC 18092, ECMA 340 Peer-to-Peer

The FSVP532 implements a demodulator and decoder for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The FSVP532 handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The FSVP532 supports MIFARE Classic 1K or MIFARE Classic 4K card emulation mode. The FSVP532 supports contactless communication using MIFARE Higher transfer speeds up to 424 kbit/s in both directions.

The FSVP532 can demodulate and decode FeliCa coded signals. The FSVP532 handles the FeliCa framing and error detection. The FSVP532 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The FSVP532 supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision. This must be implemented in firmware as well as upper layers.

In card emulation mode, the FSVP532 is able to answer to a Reader/Writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The FSVP532 generates the load modulation signals, either from its transmitter or from the LOADMOD pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S2C interface.

Compliant to ECMA 340 and ISO/IEC 18092 NFCIP-1 Passive and Active communication modes, the FSVP532 offers the possibility to communicate to another NFCIP-1 compliant device, at transfer speeds up to 424 kbit/s.The FSVP532 handles the complete NFCIP-1 framing and error detection.

The FSVP532 transceiver can be connected to an external antenna for

Reader/Writer or Card/PICC modes, without any additional active component.

The FSVP532 supports the following host interfaces:

- SPI
- I2C
- High Speed UART (HSU)

An embedded low-dropout voltage regulator allows the device to be connected directly to a battery. In addition, a power switch is included to supply power to a secure IC.

2.Features and benefits

- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated data mode detector
- Supports ISO/IEC 14443A/MIFARE
- Supports ISO/IEC 14443B (Reader/Writer mode only)
- Typical operating distance in Reader/Writer mode for communication to
- ISO/IEC 14443A/MIFARE, ISO/IEC 14443B or FeliCa cards up to 50 mm depending on antenna size and tuning
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on antenna size, tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE or FeliCa card emulation mode of approximately 100 mm depending on antenna size, tuning and external field strength
- Supports MIFARE Classic 1K or MIFARE Classic 4K encryption in Reader/Writer mode and MIFARE higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Supports contactless communication according to the FeliCa protocol at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFCIP-1 up to 424 kbit/s
- Possibility to communicate on the RF interface above 424 kbit/s using external analog components
- Supported host interfaces
- SPI interface
- I2C interface
- Power switch for external secure companion chip
- Dedicated IO ports for external device control
- Integrated antenna detector for production tests
- ECMA 373 NFC-WI interface to connect an external secure IC

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3.Applications

- Mobile and portable devices
- Consumer applications

4.Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery supply voltage		2.7		5.5	V
ICV_{DD}	LDO output voltage	V_{BAT} > 3.4 V V_{SS} =0V	[1] 2.7	3	3.4	V
PV_{DD}	Supply voltage for host interface	V_{SS} = 0 V	1.6	-	3.6	V
SV_{DD}	Output voltage for secure IC interface	V_{SS} = 0 V (SV_{DD} Switch Enabled)	DV_{DD} -0.5	-	DV_{DD}	V
I_{HPD}	Hard-Power-Down current consumption	V_{BAT} =5V	-	-	2	μA
I_{SPD}	Soft-Power-Down current consumption	V_{BAT} = 5 V, RF level detector on	-	-	45	μA
I_{DVDD}	Digital supply current	V_{BAT} =5 V, SV_{DD} switch off	[1] -	25	-	mA
I_{SVDD}	SV_{DD} load current	V_{BAT} =5 V, SV_{DD} switch on	-	-	30	mA
I_{AVDD}	Analog supply current	V_{BAT} =5 V	-	6	-	mA
I_{TVDD}	Transmitter supply	current During RF transmission, VBAT =5 V		60[3]	150[4]	mA
P_{tot}	Continuous total power dissipation	T_{amb} = -30 to +85 °C	[2] -		0.5	W
T_{amb}	Operating temperature range		-30	-	+85	°C

[1]DVDD, AVDD and TVDD must always be at the same supply voltage.

[2]The total current consumption depends on the firmware version (different internal IC clock speed)

[3]With an antenna tuned at 50 at 13.56 MHz

[4]The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

5.Block diagram

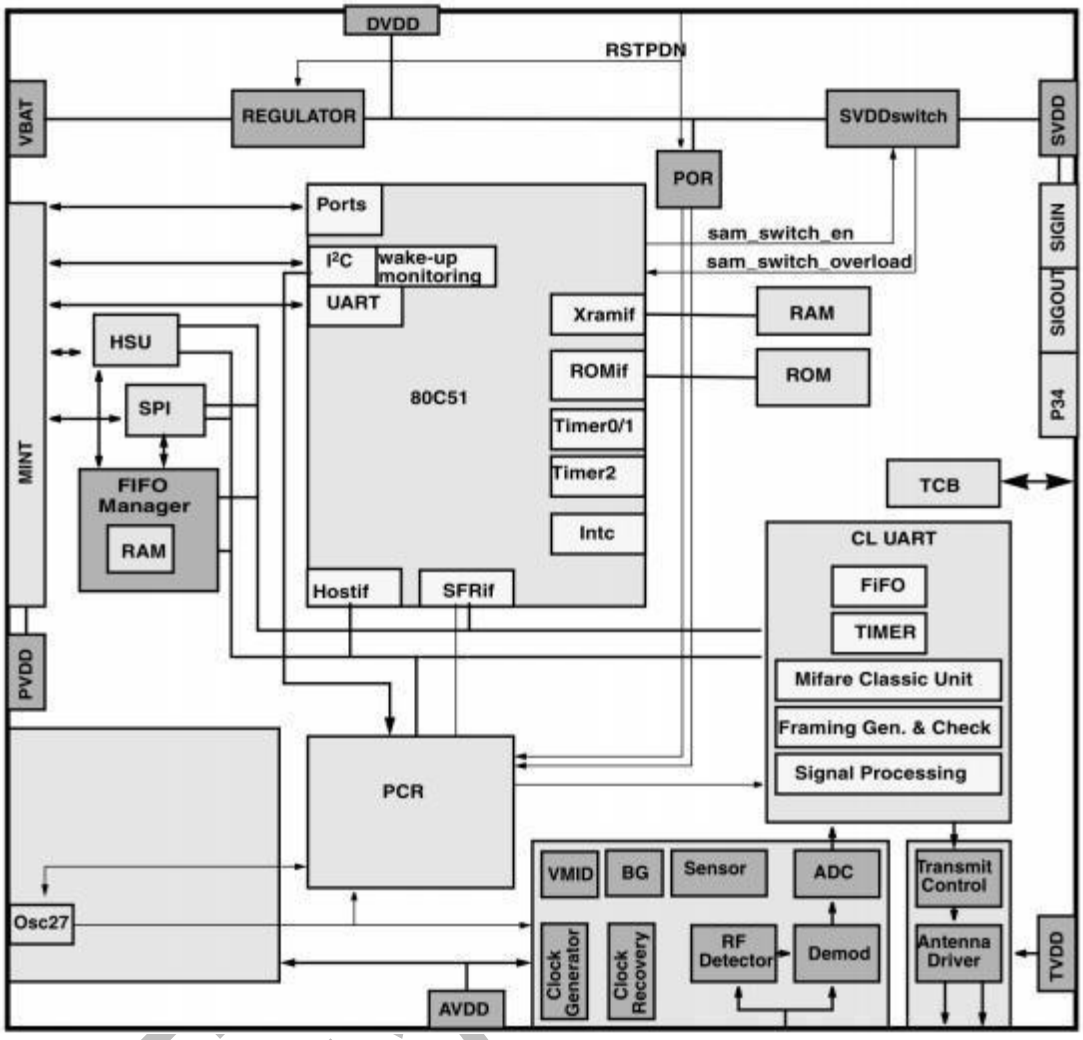


FIG1.Block Diagram of FSVP532

6.Functional description

6.1 Contactless Interface Unit (CIU)

The FSVP532 CIU is a modem for contactless communication at 13.56 MHz. It supports 6 different operating modes

- ISO/IEC 14443A/MIFARE Reader/Writer.
- FeliCa Reader/Writer.
- ISO/IEC 14443B Reader/Writer
- ISO/IEC 14443A/MIFARE Card 1K or MIFARE 4K card emulation mode
- FeliCa Card emulation
- ISO/IEC 18092, ECMA 340 NFCIP-1 Peer-to-Peer

The CIU implements a demodulator and decoder for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The CIU handles the

complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The CIU supports MIFARE Classic 1K or MIFARE Classic 4K card emulation mode. The CIU supports contactless communication using MIFARE Higher transfer speeds up to 424 kbit/s in both directions.

The CIU can demodulate and decode FeliCa coded signals. The CIU digital part handles the FeliCa framing and error detection. The CIU supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The CIU supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision which must be implemented in firmware as well as upper layers.

In card emulation mode, the CIU is able to answer to a Reader/Writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The CIU generates the load modulation signals, either from its transmitter or from the LOADMOD pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S2C interface. Compliant to ECMA 340 and ISO/IEC 18092 NFCIP-1 Passive and Active communication modes, the CIU offers the possibility to communicate to another NFCIP-1 compliant device, at transfer speeds up to 424 kbit/s.The CIU handles the complete NFCIP-1 framing and error detection.

The CIU transceiver can be connected to an external antenna for Reader/Writer or Card/PICC modes, without any additional active component.

6.1.1 Feature list

- Frequently accessed registers placed in SFR space
- Highly integrated analog circuitry to demodulate and decode received data
- Buffered transmitter drivers to minimize external components to connect an antenna.
- Integrated RF level detector
- Integrated data mode detector
- Typical operating distance of 50 mm in ISO/IEC 14443A/MIFARE or FeliCa in Reader/Writer mode depending on the antenna size, tuning and power supply
- Typical operating distance of 50 mm in NFCIP-1 mode depending on the antenna size, tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE card or FeliCa card operation mode of about 100 mm depending on the antenna size, tuning and the external field strength
- Supports MIFARE Classic 1K or MIFARE Classic 4K encryption in Reader/Writer mode
- Supports MIFARE higher data rate at 212 kbit/s and 424 kbit/s
- Supports contactless communication according to the FeliCa scheme at 212 kbit/s and 424 kbit/s

- Support of the NFC-WI/S2C interface
- 64 byte send and receive FIFO-buffer
- Programmable timer
- CRC Co-processor
- Internal self test and antenna presence detector
- 2 interrupt sources
- Adjustable parameters to optimize the transceiver performance according to the antenna characteristics

6.1.2 Simplified block diagram

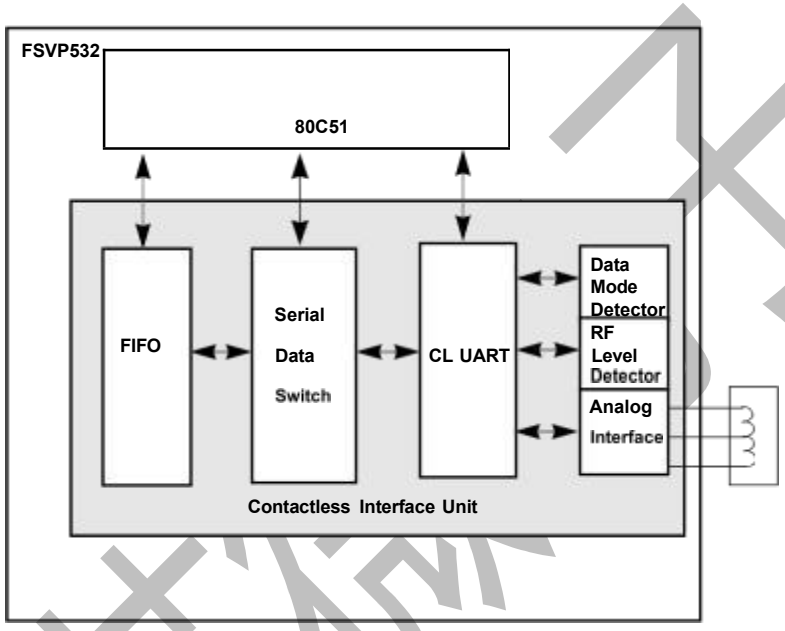


Fig 2. Simplify Contactless Interface Unit (CIU) block diagram

The Analog Interface handles the modulation and demodulation of the analog signals according to the Card emulation mode, Reader/Writer mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The data mode detector detects a ISO/IEC 14443-A MIFARE, FeliCa or NFCIP-1 mode in order to prepare the internal receiver to demodulate signals, which are sent to the FSVP532.

The NFC-WI/S2C interface supports communication to secure IC. It also supports digital signals for transfer speeds above 424 kbit/s.

The CL UART handles the protocol requirements for the communication schemes in co-operation with the appropriate firmware. The FIFO buffer allows a convenient data transfer from the 80C51 to the CIU and vice versa.

6.1.3 Reader/Writer modes

All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimal performance.

6.1.3.1 ISO/IEC 14443A Reader/Writer

The following diagram describes the communication on a physical level, the communication overview in the Table 3 describes the physical parameters.

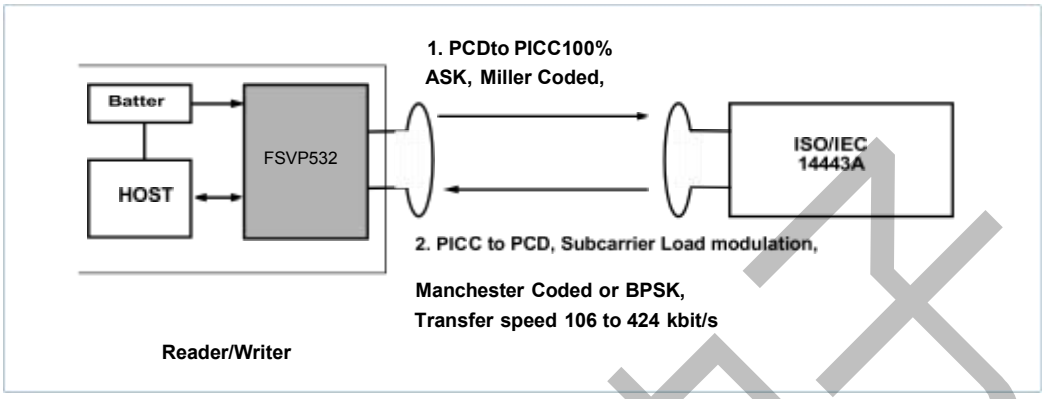
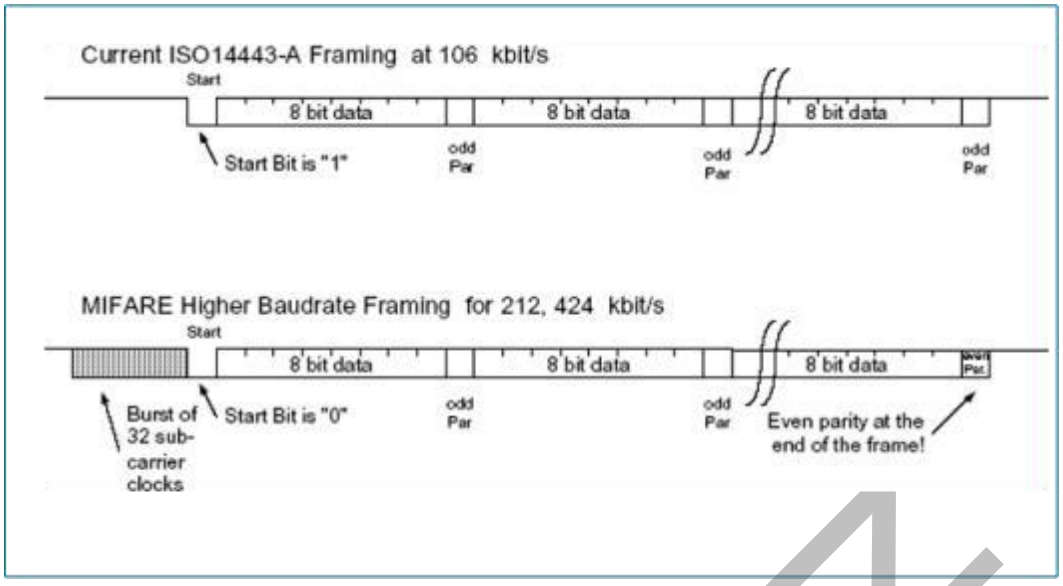


Table 3 Communication overview for ISO/IEC 14443A/MIFARE Reader/Writer

Communication scheme		ISO/IEC 14443A MIFARE	MIFARE Higher Baud Rate	
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
FSVP532 to PICC/Card	Modulation	100% ASK	100% ASK	100% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PICC/Card to FSVP532	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	$13.56\ MHz/16$	$13.56\ MHz/16$	$13.56\ MHz/16$
	Bit coding	Manchester coding	BPSK	BPSK

The internal CRC co-processor calculates the CRC value according the data coding and framing defined in the ISO/IEC 14443A part 3, and handles parity generation internally according to the transfer speed.

With appropriate firmware, the FSVP532 can handle the complete ISO/IEC 14443A/MIFARE protocol.



6.1.3.2 FeliCa Reader/Writer

The following diagram describes the communication at the physical level. Table 4 describes the physical parameters.

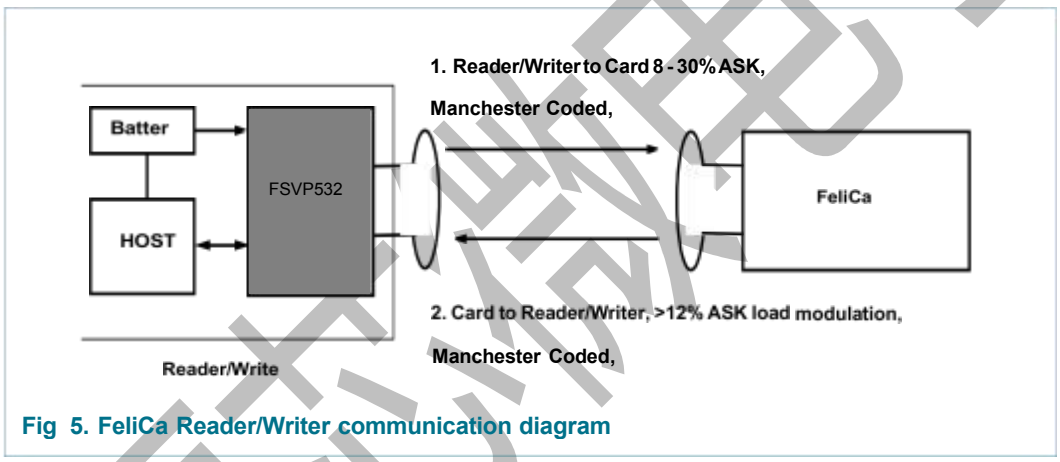


Fig 5. FeliCa Reader/Writer communication diagram

Table 4. Communication overview for FeliCa Reader/Writer

Communication scheme		FeliCa	FeliCa higher baud rate
Baud rate		212 kbit/s	424 kbit/s
Bit length		$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
FSVP532 to PICC/Card	Modulation	8 - 30% ASK	8 - 30% ASK
	Bit coding	Manchester coding	Manchester coding
PICC/Card to FSVP532	Modulation	>12% ASK	>12% ASK
	Bit coding	Manchester coding	Manchester coding

With appropriate firmware, the FSVP532 can handle the FeliCa protocol. The FeliCa Framing and coding must comply with the following table:

Table 5. FeliCa Framing and Coding

Preamble						SYNC		LEN	n-Data				CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh							

To enable the FeliCa communication a 6-byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2-byte SYNC bytes (B2h, 4Dh) are sent to synchronize the receiver. The following LEN byte indicates the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the 80C51 has to send the LEN and data bytes to the CIU. The Preamble and SYNC bytes are generated by the CIU automatically and must not be written to the FIFO. The CIU performs internally the CRC calculation and adds the result to the frame.

The starting value for the CRC Polynomial is 2 null bytes: (00h), (00h) Example of frame:

Table 6. FeliCa framing and coding

Preamble						SYNC		LEN	2 Data Bytes		CRC	
00	00	00	00	00	00	B2	4D	03	AB	CD	90	35

6.1.3.3 ISO/IEC 14443B Reader/Writer

The CIU supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision which must be implemented in firmware as well as upper layers.

The following diagram describes the communication at the physical level. Table 7 describes the physical parameters.

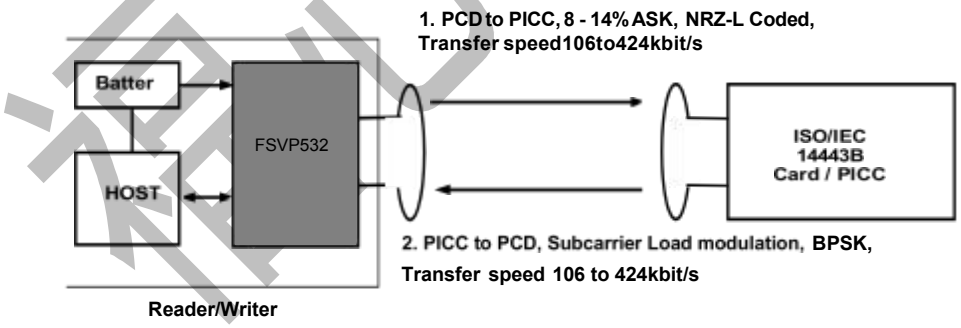


Fig 6. ISO/IEC 14443B Reader/Writer communication diagram

With appropriate firmware, the FSVP532 can handle the ISO/IEC 14443B protocol.

Table 7. Communication overview for ISO/IEC 14443B Reader/Writer

Communication scheme		ISO/IEC 14443B	Type B higher baud rate	
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
FSVP532 to PICC/Card	Modulation	8 -14% ASK	8 -14% ASK	8 -14% ASK
	Bit coding	NRZ-L	NRZ-L	NRZ-L
PICC/Card to FSVP532	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	Bit coding	BPSK	BPSK	BPSK

6.1.4 ISO/IEC 18092, ECMA 340 NFCIP-1 operating mode

A NFCIP-1 communication takes place between 2 devices:

- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

The NFCIP-1 communication differentiates between Active and Passive communication modes.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data
- Passive Communication mode means that the Target answers to an Initiator command in a load modulation scheme. The Initiator is active in terms of generating the RF field.

In order to fully support the NFCIP-1 standard the FSVP532 supports the Active and Passive Communications mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard

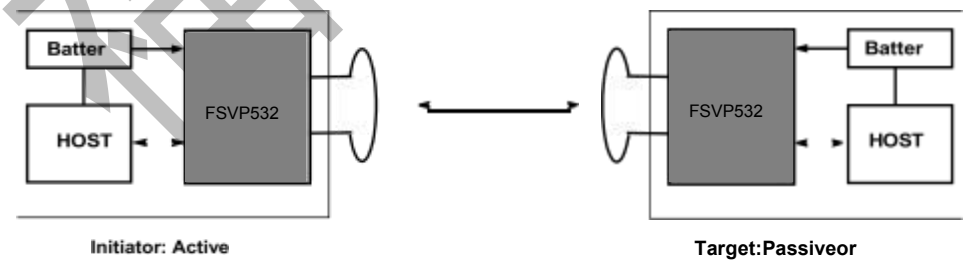


Fig 7. NFCIP-1 mode

With appropriate firmware, the FSVP532 can handle the NFCIP-1 protocol, for all communication modes and data rates, for both Initiator and Target.

6.1.4.1 ACTIVE Communication mode

Active Communication Mode means both the Initiator and the Target are using their own RF field to transmit data.

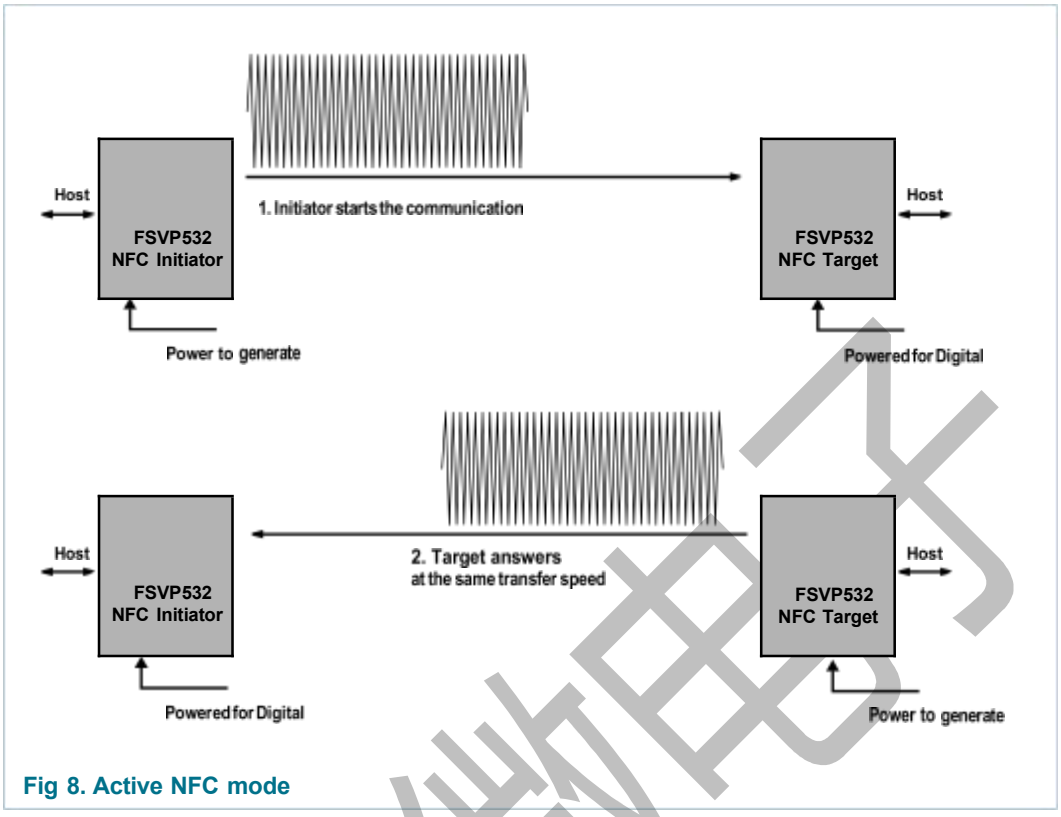


Fig 8. Active NFC mode

The following table gives an overview of the active communication modes:

Table 8. Communication overview for NFC Active Communication mode

Communication scheme		ISO/IEC 18092, ECMA 340, NFCIP-1		
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
Initiator to Target	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded
Target to Initiator	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded

6.1.4.2 PASSIVE Communication mode

Passive Communication Mode means that the target answers to an Initiator command in a load modulation scheme.

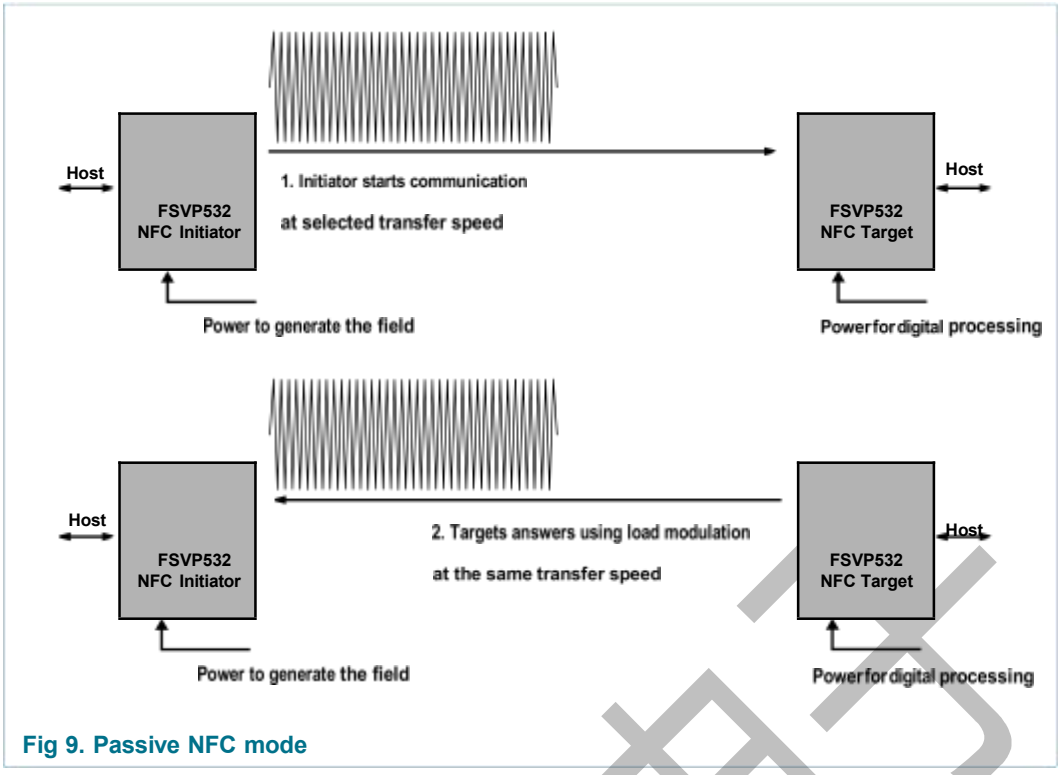


Fig 9. Passive NFC mode

The following table gives an overview of the active communication modes:

Table 9. Communication overview for NFC Passive Communication mode

Communication scheme		**ISO/IEC 18092, ECMA 340, NFCIP-1**		
Baud rate		**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
FSVP532 to PICC/Card	Modulation	100% ASK	100% ASK	100% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PICC/Card to FSVP532	Modulation	Subcarrier load modulation	>12% ASK	>12% ASK
	Subcarrier frequency	$13.56\ MHz/16$	No subcarrier	No subcarrier
	Bit coding	Manchester coding	Manchester coding	Manchester coding

6.1.4.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or ECMA 340.

6.1.4.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the ISO/IEC 18092 / ECMA340 NFCIP-1 standard. However the datalink layer is according to the following policy:

- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction.
- Speed should not be changed during a data transfer

In order not to disturb current infrastructure based on 13.56 MHz general rules to start NFC communication are defined in the following way:

- Per default NFCIP-1 device is in target mode, meaning its RF field is switched off.
- The RF level detector is active.
- Only if application requires the NFCIP-1 device shall switch to Initiator mode.
- Initiator shall only switch on its RF field if no external RF field is detected by RF Level detector during a time of TIDT.

The initiator performs initialization according to the selected mode.

6.1.5 Card operating modes

TheFSVP532 can be addressed like a FeliCa or ISO/IEC 14443A/MIFARE card. This means that the FSVP532 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A/MIFARE or FeliCa interface description.

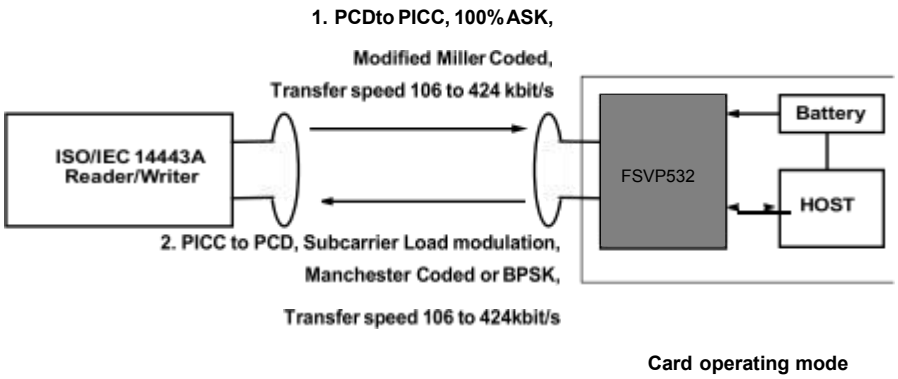
Remark: The FSVP532 does not support a secure storage of data. This has to be handled by a dedicated secure IC or a host. The secure IC is optional.

Remark: The FSVP532 can not be powered by the field in this mode and needs a power supply.

6.1.5.1 ISO/IEC 14443A/MIFARE card operating mode

With appropriate firmware, the FSVP532 can handle the ISO/IEC 14443A including the level 4, and the MIFARE protocols.

The following diagram describes the communication at the physical level. Next Table describes the physical parameters.



ISO/IEC 14443A/MIFARE card operating mode communication diagram

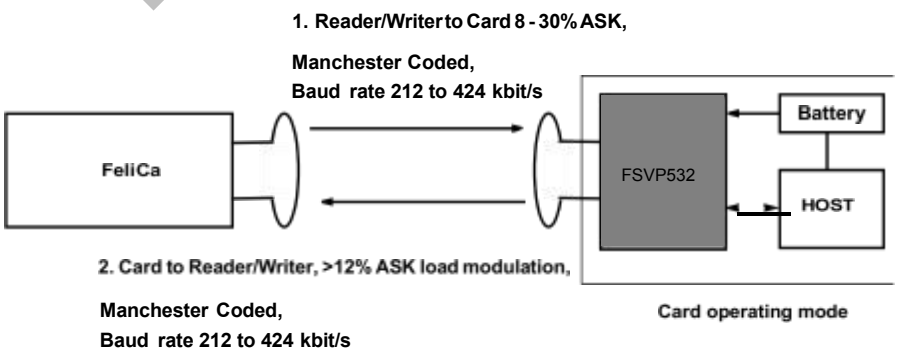
Table: Communication overview for ISO/IEC 14443A/MIFARE Card operating mode

Communication scheme		ISO/IEC 14443A MIFARE	MIFARE higher baud rate	
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
Reader/Writer to FSVP532	Modulation	100% ASK	100% ASK	100% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
FSVP532 to Reader/Writer	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	$13.56\ MHz/16$	$13.56\ MHz/16$	$13.56\ MHz/16$
	Bit coding	Manchester coding	BPSK	BPSK

6.1.5.2 FeliCa Card operating mode

With appropriate firmware, the FSVP532 can handle the FeliCa protocol.

The following diagram describes the communication at the physical level. Next Table describes the physical parameters



FeliCa card operating mode communication diagram

Table:Communication overview for FeliCa Card operating mode

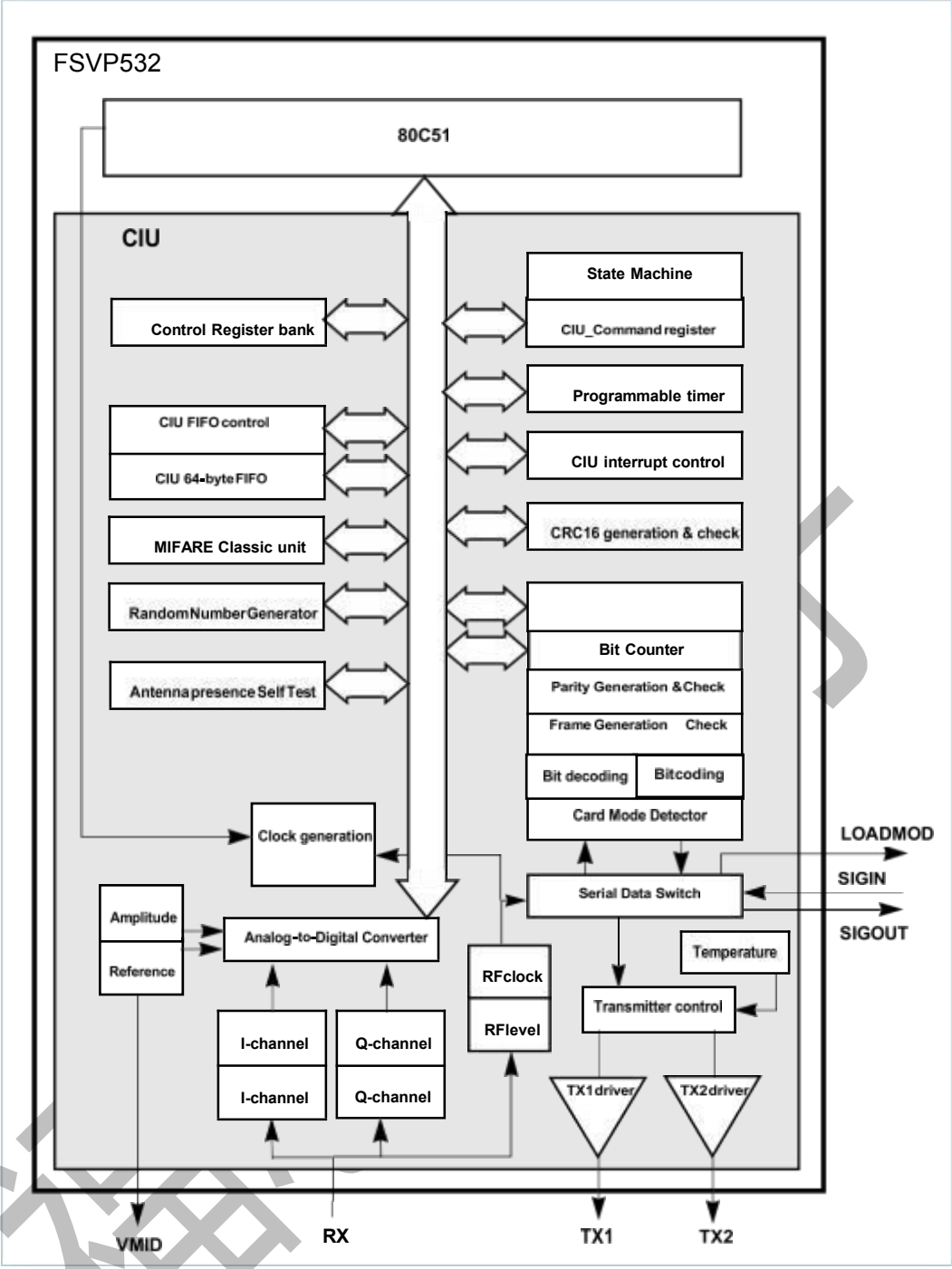
Communication scheme		**FeliCa**	**FeliCa higher baud rate**
Baud rate		**212 kbit/s**	**424 kbit/s**
Bit length		$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
Reader/Writer to FSVP532	Modulation	8 - 30% ASK	8 - 30% ASK
	Bit coding	Manchester coding	Manchester coding
FSVP532 to Reader/Writer	Modulation	>12% ASK	>12% ASK
	Bit coding	Manchester coding	Manchester coding

6.1.6 Overall CIU block diagram

The FSVP532 supports different contactless communication modes. The CIU supports the internal 80C51 for the different selected communication schemes such as Card Operation mode, Reader/Writer Operating mode or NFCIP-1 mode up to 424 kbit/s. The CIU generates bit- and byte-oriented framing and handles error detection according to these different contactless protocols.

Higher transfer speeds up to 3.39 Mbit/s can be handled by the digital part of the CIU. To modulate and demodulate the data an external circuit has to be connected to the communication interface pins SIGIN/SIGOUT.

Remark: The size and tuning of the antenna have an important impact on the achievable operating distance.

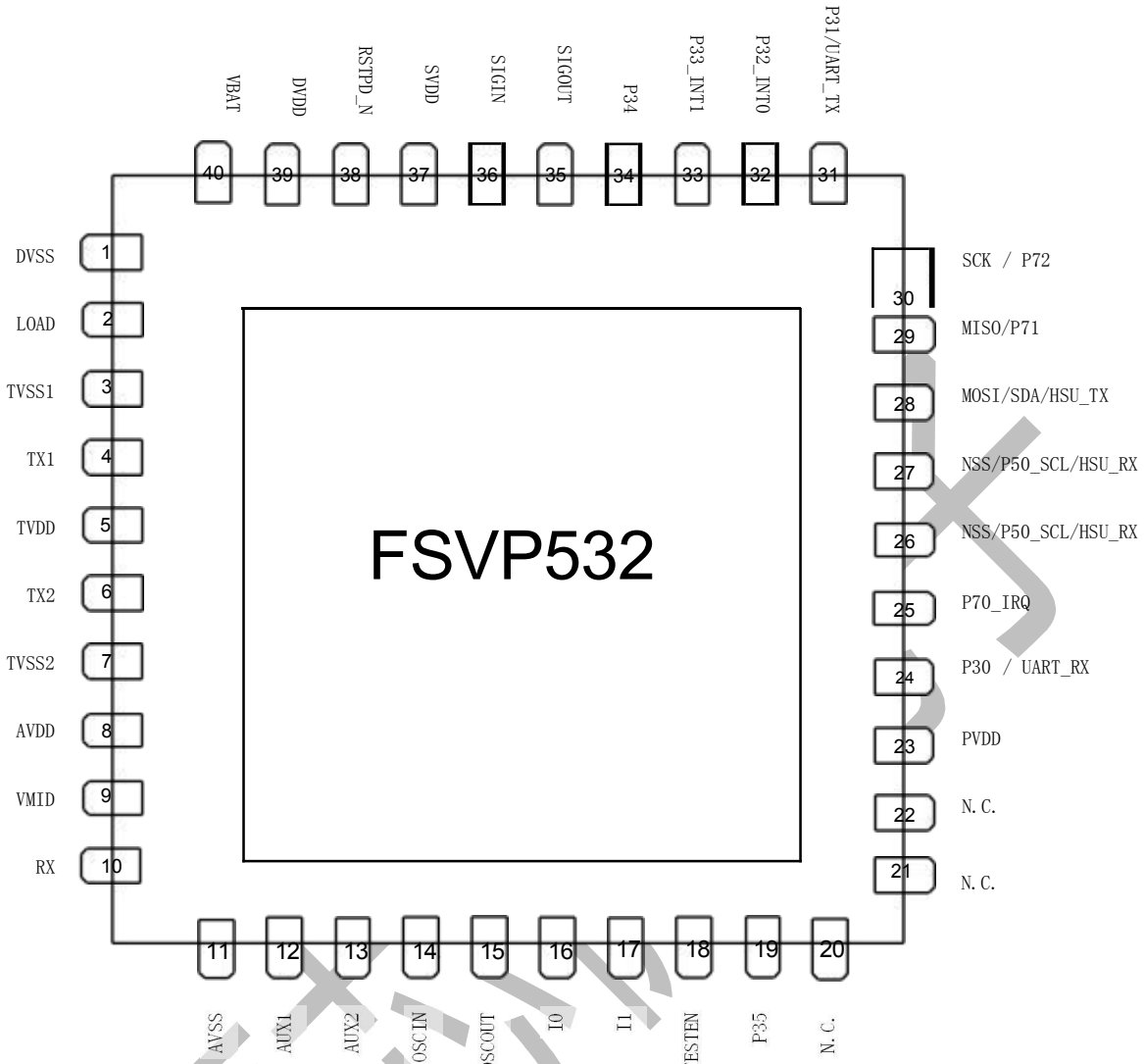


CIU detailed block diagram

7 Pinning information

7.1 Pinning

Pin configuration for HVQFN 40



7.2 Pin Description

Symbol	Pin	Type	Ref Voltage	Description
1	DVSS	PWR		Digital ground
2	LOADMOD	O	DVDD	Load modulation signal
3	TVSS1	PWR		Transmitter ground

4	TX1	O	TVDD	Transmitter output 1: transmits modulated 13.56 MHz energy carrier
5	TVDD	PWR		Transmitter power supply
6	TX2	O	TVDD	Transmitter output 2: transmits modulated 13.56 MHz energy carrier
7	TVSS2	PWR		Transmitter ground
8	AVDD	PWR		Analog power supply
9	VMID	O	AVDD	Internally generated reference voltage to bias the receiving path
10	RX	I	AVDD	Receiver input.
11	AVSS	PWR		Analog ground.
12	AUX1	O	AVDD	Auxiliary output 1: analog and digital test signals
13	AUX2	O	AVDD	Auxiliary output 2: analog and digital test signals
14	OSCIN	I	AVDD	Crystal oscillator input: to oscillator inverting amplifier
15	OSCOUT	O	AVDD	Crystal oscillator output: from oscillator inverting amplifier
16	I0	I	DVDD	Host interface selector 0
17	I1	I	DVDD	Host interface selector 1
18	TESTEN	I	DVDD	Reserved for test: connect to ground for normal operation
19	P35	IO	DVDD	General purpose IO
20	N.C.			Not connected
21	N.C.			Not connected
22	N.C.			Not connected
23	PVDD	PWR		Pad power supply
24	P30 UART_RX	IO	PVDD	General purpose IO / Debug UART receive input
25	P70_IRQ	IO	PVDD	General purpose IO. Can be used as Interrupt request to host
26	RSTOUT_N	O	PVDD	Reset indicator: when low, circuit is in reset state
27	NSS P50_SCL HSU_RX	IO	PVDD	Host interface pin: SPI Not Slave Selected (NSS) or I2C clock (SCL) or HSU receive (HSU_RX)
28	MOSI SDA HSU_TX	IO	PVDD	Host interface pin: SPI Master Out Slave In (MOSI) or I2C data (SDA) or HSU transmit (HSU_TX)
29	MISO	IO	PVDD	Host interface pin: SPI Master In Slave Out

	P71			(MISO). Can be used as general purpose IO.
30	SCK P72	IO	PVDD	Host interface pin: SPI serial clock Can be used as general purpose IO
31	P31 UART_TX	IO	PVDD	General purpose IO/ Debug UART TX
32	P32_INT0	IO	PVDD	General purpose IO / Interrupt source INT0
33	P33_INT1	IO	PVDD	General purpose IO / Interrupt source INT1
34	P34 SIC_CLK	IO	SVDD	General purpose IO / Secure IC clock
35	SIGOUT	O	SVDD	Contactless communication interface output: delivers a serial data stream according to NFCIP-1 to a secure IC
36	SIGIN	I	SVDD	Contactless communication interface input: accepts a serial data stream according to NFCIP-1 and from a secure IC.
37	SVDD	O		Switchable output power for secure IC power supply with overload detection. Used as a reference voltage for secure IC communication.
38	RSTPD_N	I	PVDD	Reset and Power-Down: When low, internal current sources are switched off, the oscillator is disabled, and input pads are disconnected from the outside world. The internal reset phase starts on the negative edge on this pin.
39	DVDD	O		Internal digital power supply
40	VBAT	PWR		Main external power supply

9 Package outline

QFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm