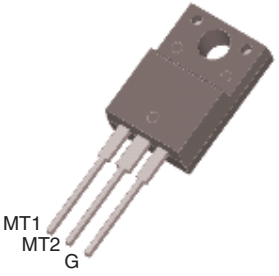
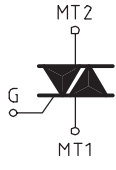


**LOGIC LEVEL TRIAC**

<b>TO220-F (FULLY ISOLATED CASE)</b>	<b>On-State Current</b> 12 Amp	<b>Gate Trigger Current</b> < 10 mA
 	<b>Off-State Voltage</b> 200 V ÷ 800 V	
	This series of TRIACs uses a high performance PNPN technology. These parts are intended for general purpose AC switching applications with highly inductive loads.	

**Absolute Maximum Ratings, according to IEC publication No. 134**

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_C = 95^\circ\text{C}$	12	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 60 Hz ( $t = 16.7\text{ ms}$ )	132	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 50 Hz ( $t = 20\text{ ms}$ )	120	A
$I^2t$	Fusing Current	$t_p = 10\text{ ms}$ , Half Cycle	72	A <sup>2</sup> s
$I_{GM}$	Peak Gate Current	$20\text{ }\mu\text{s max.}$ $T_j = 125^\circ\text{C}$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125^\circ\text{C}$	1	W
$di/dt$	Critical rate of rise of on-state current	$I_G = 2x I_{GT}$ , $t_r \leq 100\text{ ns}$ $f = 120\text{ Hz}$ , $T_j = 125^\circ\text{C}$	50	A/ $\mu\text{s}$
$T_j$	Operating Temperature		(-40 +125)	$^\circ\text{C}$
$T_{stg}$	Storage Temperature		(-40 +150)	$^\circ\text{C}$
$T_{sld}$	Soldering Temperature	10s max	260	$^\circ\text{C}$
$V_{iso}$	R.M.S. isolation voltage 50/60 Hz sinusoidal waveform		2.500	Vac

SYMBOL	PARAMETER	VOLTAGE					Unit
		B	D	M	S	N	
$V_{DRM}$	Repetitive Peak Off State Voltage	200	400	600	700	800	V
$V_{RRM}$							

# LOGIC LEVEL TRIAC

## Electrical Characteristics

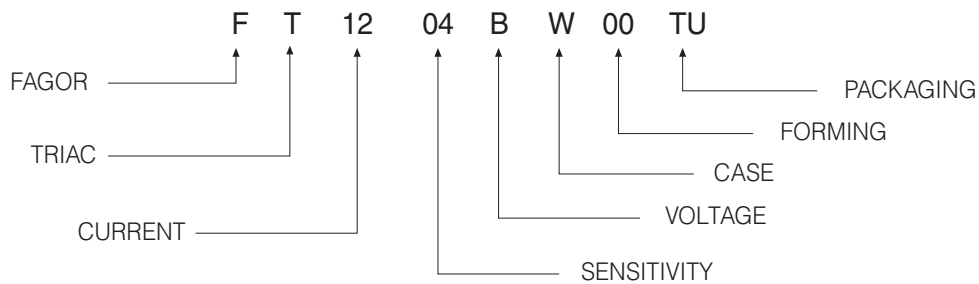
SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY			Unit
					04	08	09	
$I_{GT}^{(1)}$	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 33\Omega, T_j = 25^\circ C$	Q1÷Q3 Q4	MAX MAX	5	10	10 10	mA mA
$V_{GT}$	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 33\Omega, T_j = 25^\circ C$	Q1÷Q3 Q1÷Q4	MAX MAX	1.3		1.3	V V
$V_{GD}$	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3K\Omega, T_j = 125^\circ C$	Q1÷Q3 Q1÷Q4	MIN MIN	0.2		0.2	V V
$I_H^{(2)}$	Holding Current	$I_T = 100 \text{ mA}, \text{ Gate open}, T_j = 25^\circ C$		MAX	15	15	20	mA
$I_L$	Latching Current	$I_G = 1.2 I_{GT}, T_j = 25^\circ C$	Q1, Q3 Q1,Q3,Q4 Q2	MAX MAX MAX	25	25	20	mA mA mA
$dV/dt^{(2)}$	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, \text{ Gate open}$ $T_j = 125^\circ C$		MIN	40	40	50	V/ $\mu s$
$(dI/dt)^c^{(2)}$	Critical Rate of Current Rise	$(dv/dt)_c = 0.1 \text{ V}/\mu s, T_j = 125^\circ C$ $(dv/dt)_c = 10 \text{ V}/\mu s, T_j = 125^\circ C$ without snubber $T_j = 125^\circ C$		MIN MIN MIN	6.5	6.5	2.5	A/ms A/ms
$V_{TM}^{(2)}$	On-state Voltage	$I_T = 17 \text{ Amp}, t_p = 380 \mu s, T_j = 25^\circ C$		MAX	1.55			V
$V_{t(o)}^{(2)}$	Threshold Voltage	$T_j = 125^\circ C$		MAX	0.80			V
$r_d^{(2)}$	Dynamic Resistance	$T_j = 125^\circ C$		MAX	40			m $\Omega$
$I_{DRM}/I_{RRM}$	Off-State Leakage Current	$V_D = V_{DRM}, T_j = 125^\circ C$ $V_R = V_{RRM}, T_j = 25^\circ C$		MAX MAX	1 5			mA $\mu A$
$R_{th(j-c)}$	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.9			°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient	$S = 1 \text{ cm}^2$			50			°C/W

(1) Minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

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## PART NUMBER INFORMATION



**LOGIC LEVEL TRIAC**

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

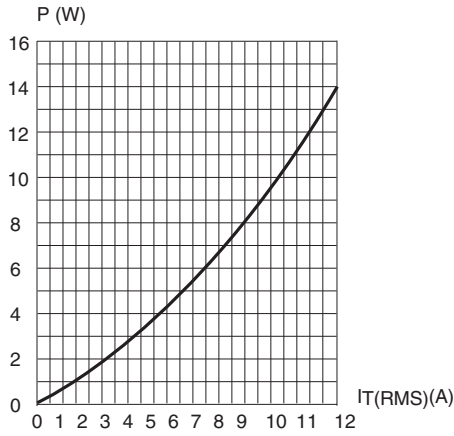


Fig. 2: RMS on-state current versus case temperature (full cycle).

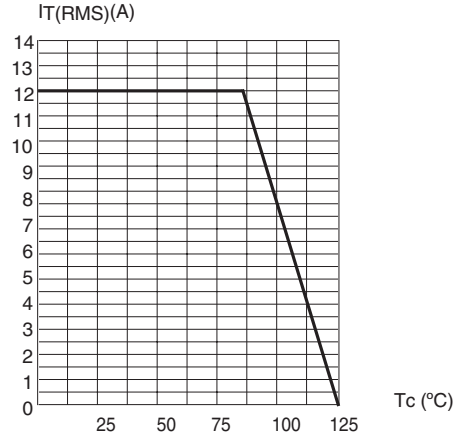


Fig. 3: Relative variation of thermal impedance versus pulse duration.

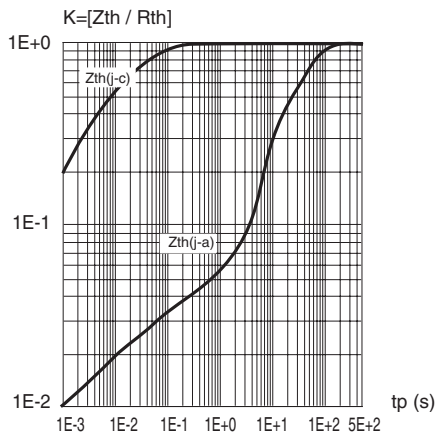


Fig. 4: On-state characteristics (maximum values)

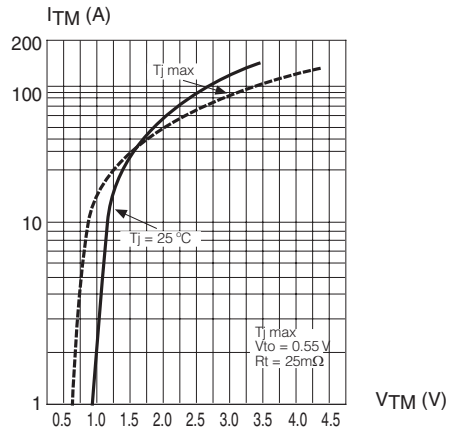


Fig. 5: Surge peak on-state current versus number of cycles

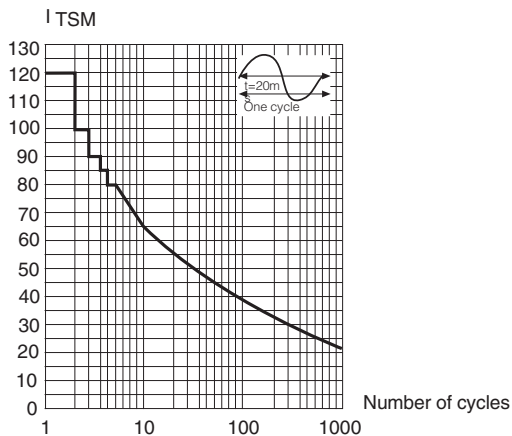
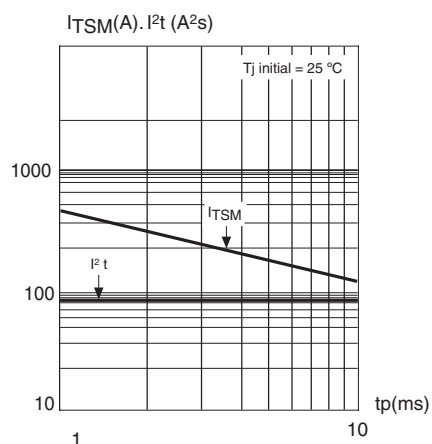


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms, and corresponding value of I²t.



### LOGIC LEVEL TRIAC

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

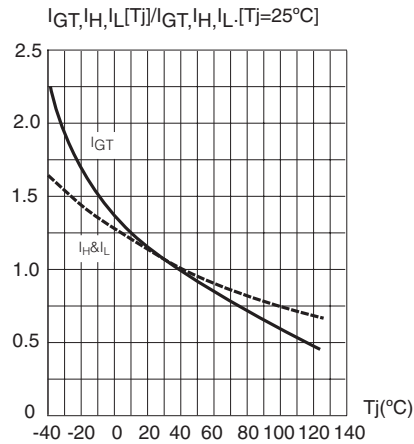


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

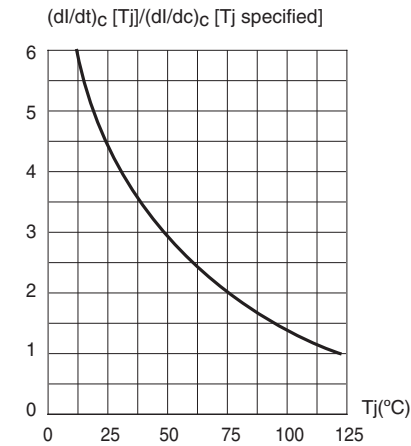
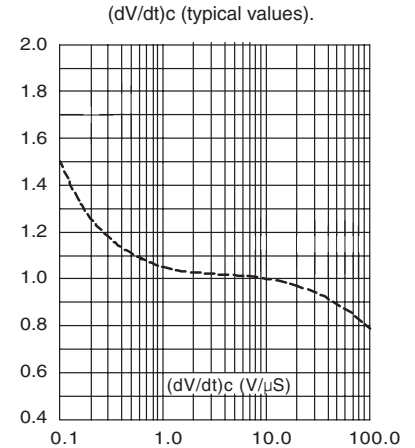


Fig. 9: Relative variation of critical rate of decrease of main current versus



### PACKAGE MECHANICAL DATA TO220-F

