Product Data Sheet

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FT1505C_B

a-Si TFT LCD Single Chip Driver
240RGBX320 Resolution and 262K Color

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1 Description

FT1505C is a single-chip 262k-color TFT LCD panel driver IC with built-in 172,800 bytes RAM, a 720-channel source driver, a 320-channel gate driver, and power supply circuit capable of supporting QVGA (240RGBx320-dot) resolution display.

The dithering image processing is implemented in the FT1505C to provide 16.7M-color display quality and the Multi-domain Vertical Alignment (MVA) wide view angle display is also supported in the FT1505C.

For efficient data transfer, the FT1505C supports 4 kinds of system interfaces which are i80-system MPU interface via 8-/9-/16-/18-bit bus, VSYNC interface (system interface + VSYNC, internal clock, DB17-DB0), serial data transfer interface (SPI), and RGB 6-/16-/18-bit interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-DB0).

In VSYNC interface modes, the combined use of widow address function enable displaying a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to display the refresh data only to minimize the amount of data transfer and the total power consumption.

FT1505C can operate at low voltage up to 1.65V I/O interface voltage, and an internal voltage follower circuit to generate voltage levels for driving LCD panel. The FT1505C also supports different power management functions (through software control) such as 8-color display mode, sleep mode, standby mode, and deep standby mode to make the FT1505C an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

2 Features

Single chip controller driver for 240RGB x 320-dot a-Si TFT LCD display supporting true 262K-color
Dithering image processing improvement to support 16.7M-color display quality
Supporting MVA (Multi-domain Vertical Alignment) wide view display
Incorporate 720-channel source driver and 320-channel gate driver
Internal 172,800 bytes graphic RAM
System interfaces
i80 system interface via 8-/ 9-/16-/18-bit bus
Serial Peripheral Interface (SPI)
VSYNC interface (System interface + VSYNC)
FMRK interface (System interface + FMARK)
Internal oscillator and hardware reset
Resizing function (×1/2, ×1/4)
Reversible source/gate driver shift direction
Window address function to specify a rectangular area for internal GRAM access
Abundant color display and drawing functions
γ-correction function enabling display in 262,144 colors
1 line-unit vertical scrolling function
Partial drive function, enabling partially driving an LCD panel at positions specified by user
Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)

- N-line-inversion liquid crystal drive to invert polarity of liquid crystal at an interval of arbitrary number of line period

Internal EPROM (EPROM): User identification code (4 bits), Vcom level adjustment (12 bits)
a-TFT LCD storage capacitor: Cst only
Power saving functions
8-color display mode
Sleep mode
Standby mode
Deep standby mode
Input power supply voltages:
IOVcc = 1.65v ~ 3.3v (interface I/O supply)
Vci = 2.4v ~ 3.3v (Logic regulator and LCD analog circuit power supply)
LCD driver output voltage:
Source/VCOM power supply voltage
DDVDH - GND = 4.5v ~ 6.0v
VCL – GND = -2.0v ~ -3.0v
Vci – VCL ≦ 6.0v
Gate driver output voltage
VGH - AGND = 10.0v ~ 20.0v
VGL – AGND = -5.0v ~ -15.0v
VGH – VGL ≦ 28.0v
VCOM driver output voltage

VcomH = 3.0v ~ (DDVDH-0.5)v

VcomL = (VCL+0.5)v ~ 0v

VcomH – VcomL ≦ 6.0v

Table 1 FT1505C power supply main specifications

No.	Item		FT1505C
1	TFT data lines		720 output
2	TFT gate lines		320 output
3	TFT display storage capacitor		Cst only (Common Vcom formula)
4	Liquid crystal drive output	S1~S720	V0 ~ V63 grayscales
		G1~G320	VGH-VGL
		Vcom	VcomH / VcomL
5	Input voltage	IOVcc (interface power)	1.65v ~ 3.30v Power supply to IM0/ID, IM1-3, RESET, DB17-DB0, RDN, SDI, SDO, WR/SCL, RS, CSN, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK Connect to Vci on the FPC when IOVcc and Vci are at the same electrical potential.
		Vci (liquid crystal drive power)	2.40v ~ 3.30v Connect to IOVcc on the FPC when IOVcc and Vci are at the same electrical potential.
6	Regulated voltage	VDD	1.7v
7	Internal step-up circuits	DDVDH	Vci1 x 2
		VGH	Vci1 x 6, x 5, x 4
		VGL	Vci1 x -3, x -4, x -5
		VCL	Vci1 x -1

3 Block Diagram

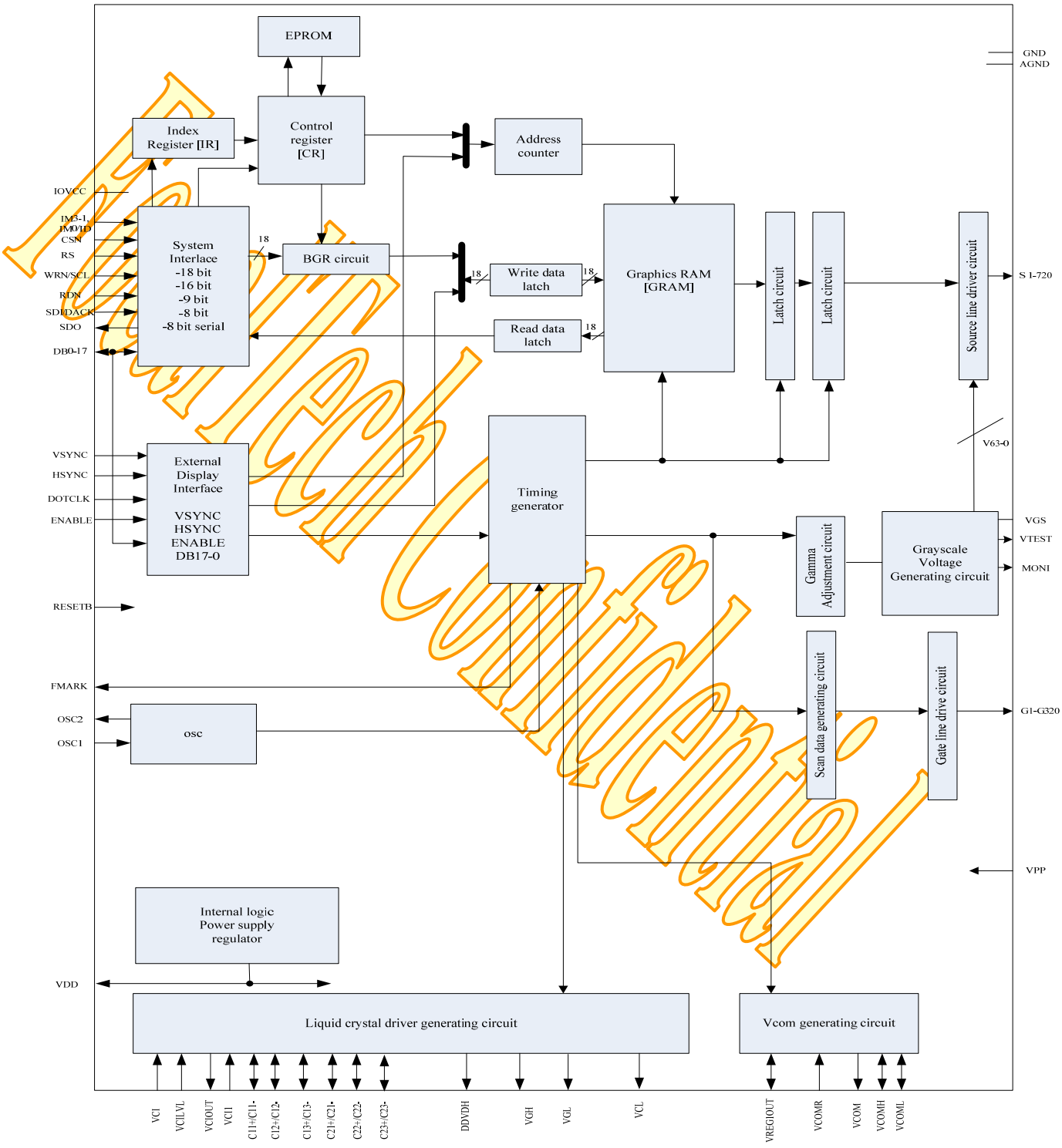


Figure 1

4 Pin Function

Table 2 Interface

<table>
<tr><th>Signal</th><th>NUM</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM3-IM1
IM0/ID</td><td>4</td><td>I</td><td>GND or IOVcc</td><td>Selects MPU interface format. Amplitude: IOVcc-GND.
When selecting clock synchronous serial interface, IM0 pin is used to set the device code ID.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU interface format</th><th>DB pins</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X</td><td>Setting disabled</td><td>–</td><td>–</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface.</td><td>DB17-DB10, DB8-DB1</td><td>65,536 or 262,144 see Note1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-DB10</td><td>65,536 or 262,144 see Note2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>Clock synchronous serial interface (SPI)</td><td>SDI/SDO</td><td>65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>X</td><td>Setting disabled</td><td>–</td><td>–</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>–</td><td>–</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>–</td><td>–</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-DB0</td><td>262,114</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-DB9</td><td>262,114</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>X</td><td>Setting disabled</td><td></td><td>-</td></tr>
</table>
Note1: 65,536 colors in 1 transfer, 262,144 colors in 2 transfer
Note2: 65,536 colors in 2 transfer, 262,144 colors in 3 transfer</td><td>All pins can't be floating.</td></tr>
<tr><td>CSN</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVcc-GND
Low: the FT1505C is selected and accessible
High: the FT1505C is not selected and not accessible.</td><td>IOVcc</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVcc-GND
Low: select Index or status register
High: select control register</td><td>IOVcc</td></tr>
<tr><td>WRN/SCL</td><td>1</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WRN is low.
Synchronous clock signal (SCL) in serial interface operation.
Amplitude: IOVcc-GND</td><td>IOVcc</td></tr>
<tr><td>RDN</td><td>1</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RDN is low.
Amplitude: IOVcc-GND</td><td>IOVcc</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal.
Amplitude: IOVcc-GND</td><td>GND or IOVcc</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal.
Amplitude: IOVcc-GND</td><td>OPEN</td></tr>
</table>

Table 3 Interface (continued)

Signal	NUM	I/O	Connect to	Function	When not in use
DB0-DB17	18	I/O	MPU	Parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVcc-GND). Fix unused pins to either IOVcc or GND level. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-DB1 are used. 18-bit I/F: DB17-DB0 are used.	GND or IOVcc
ENABLE	1	I	MPU	Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	GND or IOVcc
VSYNC	1	I	MPU	Frame synchronous signal . Low active. (Amplitude: IOVcc-GND).	GND or IOVcc
HSYNC	1	I	MPU	Line synchronous signal. Low active. (Amplitude: IOVcc-GND).	GND or IOVcc
DOTCLK	1	I	MPU	Dot clock signal. The data is inputted on the rising edge of DOTCLK. (Amplitude: IOVcc-GND).	GND or IOVcc
FMARK	1	O	MPU	Frame head pulse to synchronize RAM data writes operation with the frame head position. (Amplitude: IOVcc-GND).	Open

Table 4 Reset and oscillator

Signal	NUM	I/O	Connect to	Function	When not in use
RESETB	1	I	MPU or external RC circuit	Reset signal Initializes the FT1505C when RESET input is low. Make sure to execute a power-on reset when turning on the power supply. (Amplitude: IOVcc-GND).	-
OSC1 OSC2	2	I O	Oscillator	Leave them open	Open

Table 5 Power supply

Signal	NUM	I/O	Connect to	Function	When not in use
GND	1	-	Power supply	GND of Internal logic and GRAM. GND of interface pins: RESETB; CSN; WR; RDN; RS; DB17-DB0; VSYNC; HSYNC; DOTCLK; ENABLE. GND = 0v	-
VDD	1	O	Stabilizing capacitor	Internal regulator output used for logic and GRAM power supply. Connect a stabilizing capacitor.	-
IOVcc	1	-	Power supply	Power supply to interface pins: RESETB; CSN; WR; RDN; RS; DB17-DB0; VSYNC; HSYNC; DOTCLK; ENABLE. IOVcc = 1.65v ~ 3.3v.	-
AGND	1	-	Power supply	Analog GND (for liquid crystal power supply circuit): AGND = 0v. In case of COG, connect to GND on the FPC to prevent noise.	-
Vci	1	I	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.4v ~ 3.3v.	-

Table 6 Step-up circuit

Signal	NUM	I/O	Connect to	Function	When not in use
Vci1	1	I/O	**Normal mode**: Stabilizing Capacitor **Fixed mode**: Directly connected Vci	**Normal mode:** Reference voltage for step-up circuit 1. Vci1 must be set for the output voltages DDVDH, VGH, VGL to be generated within the respective setting ranges. See Page 118 --**Strongly recommended mode.** **Fixed mode:** Directly connected Vci. In this case, the Vciout adjustment circuit is not available. (Please be careful register VC[2:0] setting to avoid conflict. –See Page 47 .It's potential negative factor for picture quality) but the efficiency of the step-up operation can be enhanced. More detail Circuit see page 119	-
VCL	1	O	Stabilizing capacitor	Power Supply for VCOML drive, internally generated	-
DDVDH	1	O	Stabilizing capacitor	Source driver unit liquid crystal drive voltage and Vcom drive power supply. DDVDH is generated from Vci1 in the step-up circuit 1. The step-up factor is set by instruction (BT). DDVDH = 4.5v ~ 6.0v	-
VGH	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2. The step-up factor is set by instruction (BT). VGH = max. 20.0v	-
VGL	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2. The step-up factor is set by instruction (BT). VGL = max. -15.0V	-
C11A, C11B C12A, C12B	5	I/O	Step-up capacitor	Capacitor connection pins of the step-up circuit 1.	-
C13A, C13B	4	I/O	Step-up capacitor	Capacitor connection pins of the step-up circuit 3.	-
C21A, C21B C22A, C22B	7	I/O	Step-up capacitor	Capacitor connection pins of the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.	-

Table 7 Liquid crystal drive

Signal	Number	I/O	Connect to	Function	When not in use
VREG1OUT	1	O	Stabilizing capacitor	VREG1OUT is generated from Vci, and the output level is set by instruction (VRH) and used for (1) source driver grayscale reference voltage, (2) VcomH level reference voltage, (3) Vcom amplitude reference voltage (4) liquid crystal drive electrical potential in 8-color display mode. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 2.4v ~ (DDVDH – 0.5)v	Open
Vcom	1	O	TFT common electrode	Power supply to TFT common electrode. Vcom voltage is defined by VcomH and VcomL. The alternating cycle can be changed by setting register. Also Vcom output can be controlled by instruction (COM).	Open
VcomH	1	O	Stabilizing capacitor	The high level of Vcom which can be changed by either internal electric volume or connecting variable resistor (VcomR)	Open
VcomL	1	O	Stabilizing capacitor	The low level of Vcom. Connect to a stabilizing capacitor	Open
VcomR	1	I	Variable resistor or open	Connect a variable resistor between VREG1OUT and GND when adjusting the VcomH level externally.	Open
VGS	1	I	GND or external resistor	Reference level of grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor	-
S1 ~ S720	720	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S720.	Open
G1 ~ G320	320	O	LCD	Gate output signal Gate select level: VGH Gate non-select level: VGL	Open

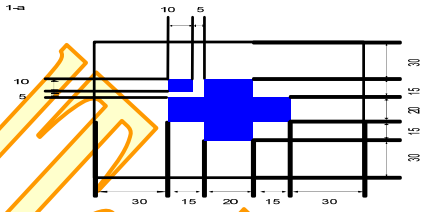
Table 8 test and dummy

Signal	Number	I/O	Connect to	Function	When not in use
PTEST1 - 2	2	O	-	Test pin. Leave it open.	Open
TESTM1 - 3	3	I	GND	Test pin.	GND or Open
TS0-9	10	O	-	Test pin. Leave it open.	Open
OSC_TEST	1	-	-	Test pin. Leave them open.	Open
DUMMY14 - 15	2	-	-	Dummy pads. Available for measuring the COG contact resistance. Dummy14 and Dummy15 are short-circuited within the chip.	Open
DUMMY1 - 13 DUMMY16 - 25	23	-	-	Dummy pads. Leave them open.	Open

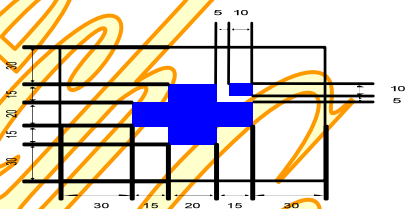
.Chip Size: 18.08 mm X 0.83 mm
.Chip Thickness: 400um (typ.)
.Pad Coordinate: Pad Center
.Coordinate Origin: chip center
.Au BUMP size:
(1) 50 um * 80 um
Input / Output
(No.1 ~ No.243)
(2) 16 um * 98 um
Staggered LCD output side
(No. 244 ~ No. 1291)

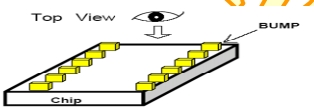
Alignment Mark:

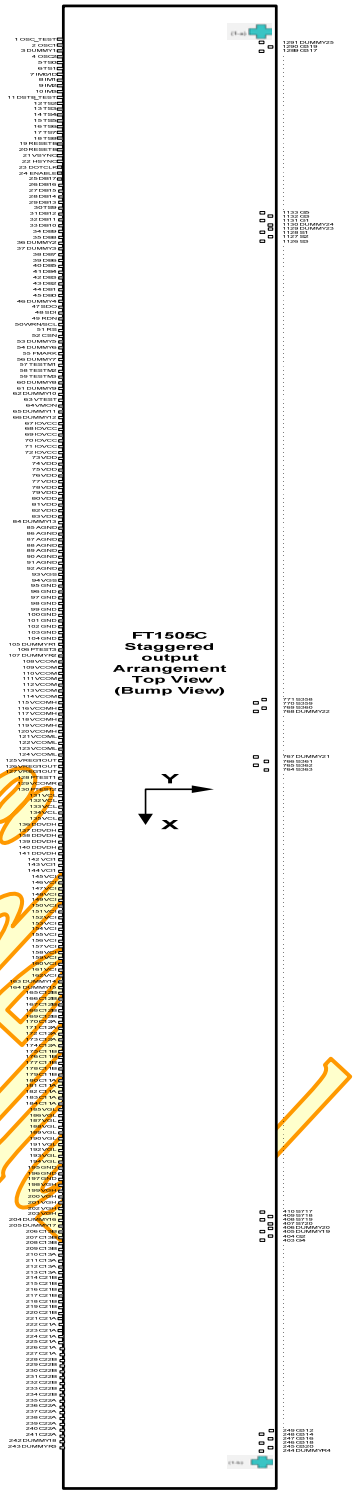
1-a



1-b







5 FT1505C PAD coordinates 1 (Unit: um)

PAD NO.	PAD NAME	X	Y
1	OSC_TEST	-8610	-307.5
2	OSC1	-8540	-307.5
3	DUMMY1	-8470	-307.5
4	OSC2	-8400	-307.5
5	TS0	-8330	-307.5
6	TS1	-8260	-307.5
7	IM0/ID	-8190	-307.5
8	IM1	-8120	-307.5
9	IM2	-8050	-307.5
10	IM3	-7980	-307.5
11	DSTB_TEST	-7910	-307.5
12	TS2	-7840	-307.5
13	TS3	-7770	-307.5
14	TS4	-7700	-307.5
15	TS5	-7630	-307.5
16	TS6	-7560	-307.5
17	TS7	-7490	-307.5
18	TS8	-7420	-307.5
19	RESETB	-7350	-307.5
20	RESETB	-7280	-307.5
21	VSYNC	-7210	-307.5
22	HSYNC	-7140	-307.5
23	DOTCLK	-7070	-307.5
24	ENABLE	-7000	-307.5
25	DB17	-6905	-307.5
26	DB16	-6825	-307.5
27	DB15	-6745	-307.5
28	DB14	-6665	-307.5
29	DB13	-6585	-307.5
30	TS9	-6495	-307.5
31	DB12	-6405	-307.5
32	DB11	-6325	-307.5

PAD NO.	PAD NAME	X	Y
51	RS	-4830	-307.5
52	CSN	-4760	-307.5
53	DUMMY5	-4690	-307.5
54	DUMMY6	-4620	-307.5
55	FMARK	-4550	-307.5
56	DUMMY7	-4480	-307.5
57	TESTM1	-4410	-307.5
58	TESTM2	-4340	-307.5
59	TESTM3	-4270	-307.5
60	DUMMY8	-4200	-307.5
61	DUMMY9	-4130	-307.5
62	DUMMY10	-4060	-307.5
63	VTEST	-3990	-307.5
64	VMON	-3920	-307.5
65	DUMMY11	-3850	-307.5
66	DUMMY12	-3780	-307.5
67	IOVCC	-3710	-307.5
68	IOVCC	-3640	-307.5
69	IOVCC	-3570	-307.5
70	IOVCC	-3500	-307.5
71	IOVCC	-3430	-307.5
72	IOVCC	-3360	-307.5
73	VDD	-3290	-307.5
74	VDD	-3220	-307.5
75	VDD	-3150	-307.5
76	VDD	-3080	-307.5
77	VDD	-3010	-307.5
78	VDD	-2940	-307.5
79	VDD	-2870	-307.5
80	VDD	-2800	-307.5
81	VDD	-2730	-307.5
82	VDD	-2660	-307.5

33	DB10	-6245	-307.5	83	VDD	-2590	-307.5
34	DB9	-6165	-307.5	84	DUMMY13	-2520	-307.5
35	DB8	-6085	-307.5	85	AGND	-2450	-307.5
36	DUMMY2	-5990	-307.5	86	AGND	-2380	-307.5
37	DUMMY3	-5920	-307.5	87	AGND	-2310	-307.5
38	DB7	-5825	-307.5	88	AGND	-2240	-307.5
39	DB6	-5745	-307.5	89	AGND	-2170	-307.5
40	DB5	-5665	-307.5	90	AGND	-2100	-307.5
41	DB4	-5585	-307.5	91	AGND	-2030	-307.5
42	DB3	-5505	-307.5	92	AGND	-1960	-307.5
43	DB2	-5425	-307.5	93	VGS	-1890	-307.5
44	DB1	-5345	-307.5	94	VGS	-1820	-307.5
45	DB0	-5265	-307.5	95	GND	-1750	-307.5
46	DUMMY4	-5180	-307.5	96	GND	-1680	-307.5
47	SDO	-5110	-307.5	97	GND	-1610	-307.5
48	SDI	-5040	-307.5	98	GND	-1540	-307.5
49	RDN	-4970	-307.5	99	GND	-1470	-307.5
50	WRN/SCL	-4900	-307.5	100	GND	-1400	-307.5

FT1505C PAD coordinates 2 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
101	GND	-1330	-307.5	151	VCI	2170	-307.5
102	GND	-1260	-307.5	152	VCI	2240	-307.5
103	GND	-1190	-307.5	153	VCI	2310	-307.5
104	GND	-1120	-307.5	154	VCI	2380	-307.5
105	DUMMYR1	-1050	-307.5	155	VCI	2450	-307.5
106	PTEST3	-980	-307.5	156	VCI	2520	-307.5
107	DUMMYR2	-910	-307.5	157	VCI	2590	-307.5
108	VCOM	-840	-307.5	158	VCI	2660	-307.5
109	VCOM	-770	-307.5	159	VCI	2730	-307.5
110	VCOM	-700	-307.5	160	VCI	2800	-307.5
111	VCOM	-630	-307.5	161	VCI	2870	-307.5
112	VCOM	-560	-307.5	162	VCI	2940	-307.5
113	VCOM	-490	-307.5	163	DUMMY14	3010	-307.5

114	VCOM	-420	-307.5	164	DUMMY15	3080	-307.5
115	VCOMH	-350	-307.5	165	C12B	3150	-307.5
116	VCOMH	-280	-307.5	166	C12B	3220	-307.5
117	VCOMH	-210	-307.5	167	C12B	3290	-307.5
118	VCOMH	-140	-307.5	168	C12B	3360	-307.5
119	VCOMH	-70	-307.5	169	C12B	3430	-307.5
120	VCOMH	0	-307.5	170	C12A	3500	-307.5
121	VCOML	70	-307.5	171	C12A	3570	-307.5
122	VCOML	140	-307.5	172	C12A	3640	-307.5
123	VCOML	210	-307.5	173	C12A	3710	-307.5
124	VCOML	280	-307.5	174	C12A	3780	-307.5
125	VREG1OUT	350	-307.5	175	C11B	3850	-307.5
126	VREG1OUT	420	-307.5	176	C11B	3920	-307.5
127	VREG1OUT	490	-307.5	177	C11B	3990	-307.5
128	PTEST1	560	-307.5	178	C11B	4060	-307.5
129	VCOMR	630	-307.5	179	C11B	4130	-307.5
130	PTEST2	700	-307.5	180	C11A	4200	-307.5
131	VCL	770	-307.5	181	C11A	4270	-307.5
132	VCL	840	-307.5	182	C11A	4340	-307.5
133	VCL	910	-307.5	183	C11A	4410	-307.5
134	VCL	980	-307.5	184	C11A	4480	-307.5
135	VCL	1050	-307.5	185	VGL	4550	-307.5
136	DDVDH	1120	-307.5	186	VGL	4620	-307.5
137	DDVDH	1190	-307.5	187	VGL	4690	-307.5
138	DDVDH	1260	-307.5	188	VGL	4760	-307.5
139	DDVDH	1330	-307.5	189	VGL	4830	-307.5
140	DDVDH	1400	-307.5	190	VGL	4900	-307.5
141	DDVDH	1470	-307.5	191	VGL	4970	-307.5
142	VCI1	1540	-307.5	192	VGL	5040	-307.5
143	VCI1	1610	-307.5	193	VGL	5110	-307.5
144	VCI1	1680	-307.5	194	VGL	5180	-307.5
145	VCI	1750	-307.5	195	GND	5250	-307.5
146	VCI	1820	-307.5	196	GND	5320	-307.5
147	VCI	1890	-307.5	197	GND	5390	-307.5

148	VCI	1960	-307.5	198	VGH	5460	-307.5
149	VCI	2030	-307.5	199	VGH	5530	-307.5
150	VCI	2100	-307.5	200	VGH	5600	-307.5

FT1505C PAD coordinates 3 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
201	VGH	5670	-307.5	251	G308	8547	319.5
202	VGH	5740	-307.5	252	G306	8531	202.5
203	VGH	5810	-307.5	253	G304	8515	319.5
204	DUMMY16	5880	-307.5	254	G302	8499	202.5
205	DUMMY17	5950	-307.5	255	G300	8483	319.5
206	C13B	6020	-307.5	256	G298	8467	202.5
207	C13B	6090	-307.5	257	G296	8451	319.5
208	C13B	6160	-307.5	258	G294	8435	202.5
209	C13B	6230	-307.5	259	G292	8419	319.5
210	C13A	6300	-307.5	260	G290	8403	202.5
211	C13A	6370	-307.5	261	G288	8387	319.5
212	C13A	6440	-307.5	262	G286	8371	202.5
213	C13A	6510	-307.5	263	G284	8355	319.5
214	C21B	6580	-307.5	264	G282	8339	202.5
215	C21B	6650	-307.5	265	G280	8323	319.5
216	C21B	6720	-307.5	266	G278	8307	202.5
217	C21B	6790	-307.5	267	G276	8291	319.5
218	C21B	6860	-307.5	268	G274	8275	202.5
219	C21B	6930	-307.5	269	G272	8259	319.5
220	C21B	7000	-307.5	270	G270	8243	202.5
221	C21A	7070	-307.5	271	G268	8227	319.5
222	C21A	7140	-307.5	272	G266	8211	202.5
223	C21A	7210	-307.5	273	G264	8195	319.5
224	C21A	7280	-307.5	274	G262	8179	202.5
225	C21A	7350	-307.5	275	G260	8163	319.5
226	C21A	7420	-307.5	276	G258	8147	202.5
227	C21A	7490	-307.5	277	G256	8131	319.5
228	C22B	7560	-307.5	278	G254	8115	202.5

229	C22B	7630	-307.5	279	G252	8099	319.5
230	C22B	7700	-307.5	280	G250	8083	202.5
231	C22B	7770	-307.5	281	G248	8067	319.5
232	C22B	7840	-307.5	282	G246	8051	202.5
233	C22B	7910	-307.5	283	G244	8035	319.5
234	C22B	7980	-307.5	284	G242	8019	202.5
235	C22A	8050	-307.5	285	G240	8003	319.5
236	C22A	8120	-307.5	286	G238	7987	202.5
237	C22A	8190	-307.5	287	G236	7971	319.5
238	C22A	8260	-307.5	288	G234	7955	202.5
239	C22A	8330	-307.5	289	G232	7939	319.5
240	C22A	8400	-307.5	290	G230	7923	202.5
241	C22A	8470	-307.5	291	G228	7907	319.5
242	DUMMY18	8540	-307.5	292	G226	7891	202.5
243	DUMMYR3	8610	-307.5	293	G224	7875	319.5
244	DUMMYR4	8659	202.5	294	G222	7859	202.5
245	G320	8643	319.5	295	G220	7843	319.5
246	G318	8627	202.5	296	G218	7827	202.5
247	G316	8611	319.5	297	G216	7811	319.5
248	G314	8595	202.5	298	G214	7795	202.5
249	G312	8579	319.5	299	G212	7779	319.5
250	G310	8563	202.5	300	G210	7763	202.5

FT1505C PAD coordinates 4 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
301	G208	7747	319.5	351	G108	6947	319.5
302	G206	7731	202.5	352	G106	6931	202.5
303	G204	7715	319.5	353	G104	6915	319.5
304	G202	7699	202.5	354	G102	6899	202.5
305	G200	7683	319.5	355	G100	6883	319.5
306	G198	7667	202.5	356	G98	6867	202.5
307	G196	7651	319.5	357	G96	6851	319.5
308	G194	7635	202.5	358	G94	6835	202.5
309	G192	7619	319.5	359	G92	6819	319.5

310	G190	7603	202.5	360	G90	6803	202.5
311	G188	7587	319.5	361	G88	6787	319.5
312	G186	7571	202.5	362	G86	6771	202.5
313	G184	7555	319.5	363	G84	6755	319.5
314	G182	7539	202.5	364	G82	6739	202.5
315	G180	7523	319.5	365	G80	6723	319.5
316	G178	7507	202.5	366	G78	6707	202.5
317	G176	7491	319.5	367	G76	6691	319.5
318	G174	7475	202.5	368	G74	6675	202.5
319	G172	7459	319.5	369	G72	6659	319.5
320	G170	7443	202.5	370	G70	6643	202.5
321	G168	7427	319.5	371	G68	6627	319.5
322	G166	7411	202.5	372	G66	6611	202.5
323	G164	7395	319.5	373	G64	6595	319.5
324	G162	7379	202.5	374	G62	6579	202.5
325	G160	7363	319.5	375	G60	6563	319.5
326	G158	7347	202.5	376	G58	6547	202.5
327	G156	7331	319.5	377	G56	6531	319.5
328	G154	7315	202.5	378	G54	6515	202.5
329	G152	7299	319.5	379	G52	6499	319.5
330	G150	7283	202.5	380	G50	6483	202.5
331	G148	7267	319.5	381	G48	6467	319.5
332	G146	7251	202.5	382	G46	6451	202.5
333	G144	7235	319.5	383	G44	6435	319.5
334	G142	7219	202.5	384	G42	6419	202.5
335	G140	7203	319.5	385	G40	6403	319.5
336	G138	7187	202.5	386	G38	6387	202.5
337	G136	7171	319.5	387	G36	6371	319.5
338	G134	7155	202.5	388	G34	6355	202.5
339	G132	7139	319.5	389	G32	6339	319.5
340	G130	7123	202.5	390	G30	6323	202.5
341	G128	7107	319.5	391	G28	6307	319.5
342	G126	7091	202.5	392	G26	6291	202.5
343	G124	7075	319.5	393	G24	6275	319.5

344	G122	7059	202.5	394	G22	6259	202.5
345	G120	7043	319.5	395	G20	6243	319.5
346	G118	7027	202.5	396	G18	6227	202.5
347	G116	7011	319.5	397	G16	6211	319.5
348	G114	6995	202.5	398	G14	6195	202.5
349	G112	6979	319.5	399	G12	6179	319.5
350	G110	6963	202.5	400	G10	6163	202.5

FT1505C PAD coordinates 5 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
401	G8	6147	319.5	451	S676	5327	202.5
402	G6	6131	202.5	452	S675	5311	319.5
403	G4	6115	319.5	453	S674	5295	202.5
404	G2	6099	202.5	454	S673	5279	319.5
405	DUMMY19	6083	319.5	455	S672	5263	202.5
406	DUMMY20	6047	319.5	456	S671	5247	319.5
407	S720	6031	202.5	457	S670	5231	202.5
408	S719	6015	319.5	458	S669	5215	319.5
409	S718	5999	202.5	459	S668	5199	202.5
410	S717	5983	319.5	460	S667	5183	319.5
411	S716	5967	202.5	461	S666	5167	202.5
412	S715	5951	319.5	462	S665	5151	319.5
413	S714	5935	202.5	463	S664	5135	202.5
414	S713	5919	319.5	464	S663	5119	319.5
415	S712	5903	202.5	465	S662	5103	202.5
416	S711	5887	319.5	466	S661	5087	319.5
417	S710	5871	202.5	467	S660	5071	202.5
418	S709	5855	319.5	468	S659	5055	319.5
419	S708	5839	202.5	469	S658	5039	202.5
420	S707	5823	319.5	470	S657	5023	319.5
421	S706	5807	202.5	471	S656	5007	202.5
422	S705	5791	319.5	472	S655	4991	319.5
423	S704	5775	202.5	473	S654	4975	202.5
424	S703	5759	319.5	474	S653	4959	319.5

425	S702	5743	202.5	475	S652	4943	202.5
426	S701	5727	319.5	476	S651	4927	319.5
427	S700	5711	202.5	477	S650	4911	202.5
428	S699	5695	319.5	478	S649	4895	319.5
429	S698	5679	202.5	479	S648	4879	202.5
430	S697	5663	319.5	480	S647	4863	319.5
431	S696	5647	202.5	481	S646	4847	202.5
432	S695	5631	319.5	482	S645	4831	319.5
433	S694	5615	202.5	483	S644	4815	202.5
434	S693	5599	319.5	484	S643	4799	319.5
435	S692	5583	202.5	485	S642	4783	202.5
436	S691	5567	319.5	486	S641	4767	319.5
437	S690	5551	202.5	487	S640	4751	202.5
438	S689	5535	319.5	488	S639	4735	319.5
439	S688	5519	202.5	489	S638	4719	202.5
440	S687	5503	319.5	490	S637	4703	319.5
441	S686	5487	202.5	491	S636	4687	202.5
442	S685	5471	319.5	492	S635	4671	319.5
443	S684	5455	202.5	493	S634	4655	202.5
444	S683	5439	319.5	494	S633	4639	319.5
445	S682	5423	202.5	495	S632	4623	202.5
446	S681	5407	319.5	496	S631	4607	319.5
447	S680	5391	202.5	497	S630	4591	202.5
448	S679	5375	319.5	498	S629	4575	319.5
449	S678	5359	202.5	499	S628	4559	202.5
450	S677	5343	319.5	500	S627	4543	319.5

FT1505C PAD coordinates 6 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
501	S626	4527	202.5	551	S576	3727	202.5
502	S625	4511	319.5	552	S575	3711	319.5
503	S624	4495	202.5	553	S574	3695	202.5
504	S623	4479	319.5	554	S573	3679	319.5
505	S622	4463	202.5	555	S572	3663	202.5

506	S621	4447	319.5	556	S571	3647	319.5
507	S620	4431	202.5	557	S570	3631	202.5
508	S619	4415	319.5	558	S569	3615	319.5
509	S618	4399	202.5	559	S568	3599	202.5
510	S617	4383	319.5	560	S567	3583	319.5
511	S616	4367	202.5	561	S566	3567	202.5
512	S615	4351	319.5	562	S565	3551	319.5
513	S614	4335	202.5	563	S564	3535	202.5
514	S613	4319	319.5	564	S563	3519	319.5
515	S612	4303	202.5	565	S562	3503	202.5
516	S611	4287	319.5	566	S561	3487	319.5
517	S610	4271	202.5	567	S560	3471	202.5
518	S609	4255	319.5	568	S559	3455	319.5
519	S608	4239	202.5	569	S558	3439	202.5
520	S607	4223	319.5	570	S557	3423	319.5
521	S606	4207	202.5	571	S556	3407	202.5
522	S605	4191	319.5	572	S555	3391	319.5
523	S604	4175	202.5	573	S554	3375	202.5
524	S603	4159	319.5	574	S553	3359	319.5
525	S602	4143	202.5	575	S552	3343	202.5
526	S601	4127	319.5	576	S551	3327	319.5
527	S600	4111	202.5	577	S550	3311	202.5
528	S599	4095	319.5	578	S549	3295	319.5
529	S598	4079	202.5	579	S548	3279	202.5
530	S597	4063	319.5	580	S547	3263	319.5
531	S596	4047	202.5	581	S546	3247	202.5
532	S595	4031	319.5	582	S545	3231	319.5
533	S594	4015	202.5	583	S544	3215	202.5
534	S593	3999	319.5	584	S543	3199	319.5
535	S592	3983	202.5	585	S542	3183	202.5
536	S591	3967	319.5	586	S541	3167	319.5
537	S590	3951	202.5	587	S540	3151	202.5
538	S589	3935	319.5	588	S539	3135	319.5
539	S588	3919	202.5	589	S538	3119	202.5

540	S587	3903	319.5	590	S537	3103	319.5
541	S586	3887	202.5	591	S536	3087	202.5
542	S585	3871	319.5	592	S535	3071	319.5
543	S584	3855	202.5	593	S534	3055	202.5
544	S583	3839	319.5	594	S533	3039	319.5
545	S582	3823	202.5	595	S532	3023	202.5
546	S581	3807	319.5	596	S531	3007	319.5
547	S580	3791	202.5	597	S530	2991	202.5
548	S579	3775	319.5	598	S529	2975	319.5
549	S578	3759	202.5	599	S528	2959	202.5
550	S577	3743	319.5	600	S527	2943	319.5

FT1505C PAD coordinates 7 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
601	S526	2927	202.5	651	S476	2127	202.5
602	S525	2911	319.5	652	S475	2111	319.5
603	S524	2895	202.5	653	S474	2095	202.5
604	S523	2879	319.5	654	S473	2079	319.5
605	S522	2863	202.5	655	S472	2063	202.5
606	S521	2847	319.5	656	S471	2047	319.5
607	S520	2831	202.5	657	S470	2031	202.5
608	S519	2815	319.5	658	S469	2015	319.5
609	S518	2799	202.5	659	S468	1999	202.5
610	S517	2783	319.5	660	S467	1983	319.5
611	S516	2767	202.5	661	S466	1967	202.5
612	S515	2751	319.5	662	S465	1951	319.5
613	S514	2735	202.5	663	S464	1935	202.5
614	S513	2719	319.5	664	S463	1919	319.5
615	S512	2703	202.5	665	S462	1903	202.5
616	S511	2687	319.5	666	S461	1887	319.5
617	S510	2671	202.5	667	S460	1871	202.5
618	S509	2655	319.5	668	S459	1855	319.5
619	S508	2639	202.5	669	S458	1839	202.5
620	S507	2623	319.5	670	S457	1823	319.5

621	S506	2607	202.5	671	S456	1807	202.5
622	S505	2591	319.5	672	S455	1791	319.5
623	S504	2575	202.5	673	S454	1775	202.5
624	S503	2559	319.5	674	S453	1759	319.5
625	S502	2543	202.5	675	S452	1743	202.5
626	S501	2527	319.5	676	S451	1727	319.5
627	S500	2511	202.5	677	S450	1711	202.5
628	S499	2495	319.5	678	S449	1695	319.5
629	S498	2479	202.5	679	S448	1679	202.5
630	S497	2463	319.5	680	S447	1663	319.5
631	S496	2447	202.5	681	S446	1647	202.5
632	S495	2431	319.5	682	S445	1631	319.5
633	S494	2415	202.5	683	S444	1615	202.5
634	S493	2399	319.5	684	S443	1599	319.5
635	S492	2383	202.5	685	S442	1583	202.5
636	S491	2367	319.5	686	S441	1567	319.5
637	S490	2351	202.5	687	S440	1551	202.5
638	S489	2335	319.5	688	S439	1535	319.5
639	S488	2319	202.5	689	S438	1519	202.5
640	S487	2303	319.5	690	S437	1503	319.5
641	S486	2287	202.5	691	S436	1487	202.5
642	S485	2271	319.5	692	S435	1471	319.5
643	S484	2255	202.5	693	S434	1455	202.5
644	S483	2239	319.5	694	S433	1439	319.5
645	S482	2223	202.5	695	S432	1423	202.5
646	S481	2207	319.5	696	S431	1407	319.5
647	S480	2191	202.5	697	S430	1391	202.5
648	S479	2175	319.5	698	S429	1375	319.5
649	S478	2159	202.5	699	S428	1359	202.5
650	S477	2143	319.5	700	S427	1343	319.5

FT1505C PAD coordinates 8 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
701	S426	1327	202.5	751	S376	527	202.5

702	S425	1311	319.5	752	S375	511	319.5
703	S424	1295	202.5	753	S374	495	202.5
704	S423	1279	319.5	754	S373	479	319.5
705	S422	1263	202.5	755	S372	463	202.5
706	S421	1247	319.5	756	S371	447	319.5
707	S420	1231	202.5	757	S370	431	202.5
708	S419	1215	319.5	758	S369	415	319.5
709	S418	1199	202.5	759	S368	399	202.5
710	S417	1183	319.5	760	S367	383	319.5
711	S416	1167	202.5	761	S366	367	202.5
712	S415	1151	319.5	762	S365	351	319.5
713	S414	1135	202.5	763	S364	335	202.5
714	S413	1119	319.5	764	S363	319	319.5
715	S412	1103	202.5	765	S362	303	202.5
716	S411	1087	319.5	766	S361	287	319.5
717	S410	1071	202.5	767	DUMMY21	271	202.5
718	S409	1055	319.5	768	DUMMY22	-271	202.5
719	S408	1039	202.5	769	S360	-287	319.5
720	S407	1023	319.5	770	S359	-303	202.5
721	S406	1007	202.5	771	S358	-319	319.5
722	S405	991	319.5	772	S357	-335	202.5
723	S404	975	202.5	773	S356	-351	319.5
724	S403	959	319.5	774	S355	-367	202.5
725	S402	943	202.5	775	S354	-383	319.5
726	S401	927	319.5	776	S353	-399	202.5
727	S400	911	202.5	777	S352	-415	319.5
728	S399	895	319.5	778	S351	-431	202.5
729	S398	879	202.5	779	S350	-447	319.5
730	S397	863	319.5	780	S349	-463	202.5
731	S396	847	202.5	781	S348	-479	319.5
732	S395	831	319.5	782	S347	-495	202.5
733	S394	815	202.5	783	S346	-511	319.5
734	S393	799	319.5	784	S345	-527	202.5
735	S392	783	202.5	785	S344	-543	319.5

736	S391	767	319.5	786	S343	-559	202.5
737	S390	751	202.5	787	S342	-575	319.5
738	S389	735	319.5	788	S341	-591	202.5
739	S388	719	202.5	789	S340	-607	319.5
740	S387	703	319.5	790	S339	-623	202.5
741	S386	687	202.5	791	S338	-639	319.5
742	S385	671	319.5	792	S337	-655	202.5
743	S384	655	202.5	793	S336	-671	319.5
744	S383	639	319.5	794	S335	-687	202.5
745	S382	623	202.5	795	S334	-703	319.5
746	S381	607	319.5	796	S333	-719	202.5
747	S380	591	202.5	797	S332	-735	319.5
748	S379	575	319.5	798	S331	-751	202.5
749	S378	559	202.5	799	S330	-767	319.5
750	S377	543	319.5	800	S329	-783	202.5

FT1505C PAD coordinates 9 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
801	S328	-799	319.5	851	S278	-1599	319.5
802	S327	-815	202.5	852	S277	-1615	202.5
803	S326	-831	319.5	853	S276	-1631	319.5
804	S325	-847	202.5	854	S275	-1647	202.5
805	S324	-863	319.5	855	S274	-1663	319.5
806	S323	-879	202.5	856	S273	-1679	202.5
807	S322	-895	319.5	857	S272	-1695	319.5
808	S321	-911	202.5	858	S271	-1711	202.5
809	S320	-927	319.5	859	S270	-1727	319.5
810	S319	-943	202.5	860	S269	-1743	202.5
811	S318	-959	319.5	861	S268	-1759	319.5
812	S317	-975	202.5	862	S267	-1775	202.5
813	S316	-991	319.5	863	S266	-1791	319.5
814	S315	-1007	202.5	864	S265	-1807	202.5
815	S314	-1023	319.5	865	S264	-1823	319.5
816	S313	-1039	202.5	866	S263	-1839	202.5

817	S312	-1055	319.5	867	S262	-1855	319.5
818	S311	-1071	202.5	868	S261	-1871	202.5
819	S310	-1087	319.5	869	S260	-1887	319.5
820	S309	-1103	202.5	870	S259	-1903	202.5
821	S308	-1119	319.5	871	S258	-1919	319.5
822	S307	-1135	202.5	872	S257	-1935	202.5
823	S306	-1151	319.5	873	S256	-1951	319.5
824	S305	-1167	202.5	874	S255	-1967	202.5
825	S304	-1183	319.5	875	S254	-1983	319.5
826	S303	-1199	202.5	876	S253	-1999	202.5
827	S302	-1215	319.5	877	S252	-2015	319.5
828	S301	-1231	202.5	878	S251	-2031	202.5
829	S300	-1247	319.5	879	S250	-2047	319.5
830	S299	-1263	202.5	880	S249	-2063	202.5
831	S298	-1279	319.5	881	S248	-2079	319.5
832	S297	-1295	202.5	882	S247	-2095	202.5
833	S296	-1311	319.5	883	S246	-2111	319.5
834	S295	-1327	202.5	884	S245	-2127	202.5
835	S294	-1343	319.5	885	S244	-2143	319.5
836	S293	-1359	202.5	886	S243	-2159	202.5
837	S292	-1375	319.5	887	S242	-2175	319.5
838	S291	-1391	202.5	888	S241	-2191	202.5
839	S290	-1407	319.5	889	S240	-2207	319.5
840	S289	-1423	202.5	890	S239	-2223	202.5
841	S288	-1439	319.5	891	S238	-2239	319.5
842	S287	-1455	202.5	892	S237	-2255	202.5
843	S286	-1471	319.5	893	S236	-2271	319.5
844	S285	-1487	202.5	894	S235	-2287	202.5
845	S284	-1503	319.5	895	S234	-2303	319.5
846	S283	-1519	202.5	896	S233	-2319	202.5
847	S282	-1535	319.5	897	S232	-2335	319.5
848	S281	-1551	202.5	898	S231	-2351	202.5
849	S280	-1567	319.5	899	S230	-2367	319.5
850	S279	-1583	202.5	900	S229	-2383	202.5

FT1505C PAD coordinates 10 (Unit: um)

PAD NO.	PAD NAME	X	Y
901	S228	-2399	319.5
902	S227	-2415	202.5
903	S226	-2431	319.5
904	S225	-2447	202.5
905	S224	-2463	319.5
906	S223	-2479	202.5
907	S222	-2495	319.5
908	S221	-2511	202.5
909	S220	-2527	319.5
910	S219	-2543	202.5
911	S218	-2559	319.5
912	S217	-2575	202.5
913	S216	-2591	319.5
914	S215	-2607	202.5
915	S214	-2623	319.5
916	S213	-2639	202.5
917	S212	-2655	319.5
918	S211	-2671	202.5
919	S210	-2687	319.5
920	S209	-2703	202.5
921	S208	-2719	319.5
922	S207	-2735	202.5
923	S206	-2751	319.5
924	S205	-2767	202.5
925	S204	-2783	319.5
926	S203	-2799	202.5
927	S202	-2815	319.5
928	S201	-2831	202.5
929	S200	-2847	319.5
930	S199	-2863	202.5
931	S198	-2879	319.5

PAD NO.	PAD NAME	X	Y
951	S178	-3199	319.5
952	S177	-3215	202.5
953	S176	-3231	319.5
954	S175	-3247	202.5
955	S174	-3263	319.5
956	S173	-3279	202.5
957	S172	-3295	319.5
958	S171	-3311	202.5
959	S170	-3327	319.5
960	S169	-3343	202.5
961	S168	-3359	319.5
962	S167	-3375	202.5
963	S166	-3391	319.5
964	S165	-3407	202.5
965	S164	-3423	319.5
966	S163	-3439	202.5
967	S162	-3455	319.5
968	S161	-3471	202.5
969	S160	-3487	319.5
970	S159	-3503	202.5
971	S158	-3519	319.5
972	S157	-3535	202.5
973	S156	-3551	319.5
974	S155	-3567	202.5
975	S154	-3583	319.5
976	S153	-3599	202.5
977	S152	-3615	319.5
978	S151	-3631	202.5
979	S150	-3647	319.5
980	S149	-3663	202.5
981	S148	-3679	319.5

932	S197	-2895	202.5	982	S147	-3695	202.5
933	S196	-2911	319.5	983	S146	-3711	319.5
934	S195	-2927	202.5	984	S145	-3727	202.5
935	S194	-2943	319.5	985	S144	-3743	319.5
936	S193	-2959	202.5	986	S143	-3759	202.5
937	S192	-2975	319.5	987	S142	-3775	319.5
938	S191	-2991	202.5	988	S141	-3791	202.5
939	S190	-3007	319.5	989	S140	-3807	319.5
940	S189	-3023	202.5	990	S139	-3823	202.5
941	S188	-3039	319.5	991	S138	-3839	319.5
942	S187	-3055	202.5	992	S137	-3855	202.5
943	S186	-3071	319.5	993	S136	-3871	319.5
944	S185	-3087	202.5	994	S135	-3887	202.5
945	S184	-3103	319.5	995	S134	-3903	319.5
946	S183	-3119	202.5	996	S133	-3919	202.5
947	S182	-3135	319.5	997	S132	-3935	319.5
948	S181	-3151	202.5	998	S131	-3951	202.5
949	S180	-3167	319.5	999	S130	-3967	319.5
950	S179	-3183	202.5	1000	S129	-3983	202.5

FT1505C PAD coordinates 11 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
1001	S128	-3999	319.5	1051	S78	-4799	319.5
1002	S127	-4015	202.5	1052	S77	-4815	202.5
1003	S126	-4031	319.5	1053	S76	-4831	319.5
1004	S125	-4047	202.5	1054	S75	-4847	202.5
1005	S124	-4063	319.5	1055	S74	-4863	319.5
1006	S123	-4079	202.5	1056	S73	-4879	202.5
1007	S122	-4095	319.5	1057	S72	-4895	319.5
1008	S121	-4111	202.5	1058	S71	-4911	202.5
1009	S120	-4127	319.5	1059	S70	-4927	319.5
1010	S119	-4143	202.5	1060	S69	-4943	202.5
1011	S118	-4159	319.5	1061	S68	-4959	319.5
1012	S117	-4175	202.5	1062	S67	-4975	202.5

1013	S116	-4191	319.5	1063	S66	-4991	319.5
1014	S115	-4207	202.5	1064	S65	-5007	202.5
1015	S114	-4223	319.5	1065	S64	-5023	319.5
1016	S113	-4239	202.5	1066	S63	-5039	202.5
1017	S112	-4255	319.5	1067	S62	-5055	319.5
1018	S111	-4271	202.5	1068	S61	-5071	202.5
1019	S110	-4287	319.5	1069	S60	-5087	319.5
1020	S109	-4303	202.5	1070	S59	-5103	202.5
1021	S108	-4319	319.5	1071	S58	-5119	319.5
1022	S107	-4335	202.5	1072	S57	-5135	202.5
1023	S106	-4351	319.5	1073	S56	-5151	319.5
1024	S105	-4367	202.5	1074	S55	-5167	202.5
1025	S104	-4383	319.5	1075	S54	-5183	319.5
1026	S103	-4399	202.5	1076	S53	-5199	202.5
1027	S102	-4415	319.5	1077	S52	-5215	319.5
1028	S101	-4431	202.5	1078	S51	-5231	202.5
1029	S100	-4447	319.5	1079	S50	-5247	319.5
1030	S99	-4463	202.5	1080	S49	-5263	202.5
1031	S98	-4479	319.5	1081	S48	-5279	319.5
1032	S97	-4495	202.5	1082	S47	-5295	202.5
1033	S96	-4511	319.5	1083	S46	-5311	319.5
1034	S95	-4527	202.5	1084	S45	-5327	202.5
1035	S94	-4543	319.5	1085	S44	-5343	319.5
1036	S93	-4559	202.5	1086	S43	-5359	202.5
1037	S92	-4575	319.5	1087	S42	-5375	319.5
1038	S91	-4591	202.5	1088	S41	-5391	202.5
1039	S90	-4607	319.5	1089	S40	-5407	319.5
1040	S89	-4623	202.5	1090	S39	-5423	202.5
1041	S88	-4639	319.5	1091	S38	-5439	319.5
1042	S87	-4655	202.5	1092	S37	-5455	202.5
1043	S86	-4671	319.5	1093	S36	-5471	319.5
1044	S85	-4687	202.5	1094	S35	-5487	202.5
1045	S84	-4703	319.5	1095	S34	-5503	319.5
1046	S83	-4719	202.5	1096	S33	-5519	202.5

1047	S82	-4735	319.5	1097	S32	-5535	319.5
1048	S81	-4751	202.5	1098	S31	-5551	202.5
1049	S80	-4767	319.5	1099	S30	-5567	319.5
1050	S79	-4783	202.5	1100	S29	-5583	202.5

FT1505C PAD coordinates 12 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
1101	S28	-5599	319.5	1151	G41	-6419	202.5
1102	S27	-5615	202.5	1152	G43	-6435	319.5
1103	S26	-5631	319.5	1153	G45	-6451	202.5
1104	S25	-5647	202.5	1154	G47	-6467	319.5
1105	S24	-5663	319.5	1155	G49	-6483	202.5
1106	S23	-5679	202.5	1156	G51	-6499	319.5
1107	S22	-5695	319.5	1157	G53	-6515	202.5
1108	S21	-5711	202.5	1158	G55	-6531	319.5
1109	S20	-5727	319.5	1159	G57	-6547	202.5
1110	S19	-5743	202.5	1160	G59	-6563	319.5
1111	S18	-5759	319.5	1161	G61	-6579	202.5
1112	S17	-5775	202.5	1162	G63	-6595	319.5
1113	S16	-5791	319.5	1163	G65	-6611	202.5
1114	S15	-5807	202.5	1164	G67	-6627	319.5
1115	S14	-5823	319.5	1165	G69	-6643	202.5
1116	S13	-5839	202.5	1166	G71	-6659	319.5
1117	S12	-5855	319.5	1167	G73	-6675	202.5
1118	S11	-5871	202.5	1168	G75	-6691	319.5
1119	S10	-5887	319.5	1169	G77	-6707	202.5
1120	S9	-5903	202.5	1170	G79	-6723	319.5
1121	S8	-5919	319.5	1171	G81	-6739	202.5
1122	S7	-5935	202.5	1172	G83	-6755	319.5
1123	S6	-5951	319.5	1173	G85	-6771	202.5
1124	S5	-5967	202.5	1174	G87	-6787	319.5
1125	S4	-5983	319.5	1175	G89	-6803	202.5
1126	S3	-5999	202.5	1176	G91	-6819	319.5
1127	S2	-6015	319.5	1177	G93	-6835	202.5

1128	S1	-6031	202.5	1178	G95	-6851	319.5
1129	DUMMY23	-6047	319.5	1179	G97	-6867	202.5
1130	DUMMY24	-6083	319.5	1180	G99	-6883	319.5
1131	G1	-6099	202.5	1181	G101	-6899	202.5
1132	G3	-6115	319.5	1182	G103	-6915	319.5
1133	G5	-6131	202.5	1183	G105	-6931	202.5
1134	G7	-6147	319.5	1184	G107	-6947	319.5
1135	G9	-6163	202.5	1185	G109	-6963	202.5
1136	G11	-6179	319.5	1186	G111	-6979	319.5
1137	G13	-6195	202.5	1187	G113	-6995	202.5
1138	G15	-6211	319.5	1188	G115	-7011	319.5
1139	G17	-6227	202.5	1189	G117	-7027	202.5
1140	G19	-6243	319.5	1190	G119	-7043	319.5
1141	G21	-6259	202.5	1191	G121	-7059	202.5
1142	G23	-6275	319.5	1192	G123	-7075	319.5
1143	G25	-6291	202.5	1193	G125	-7091	202.5
1144	G27	-6307	319.5	1194	G127	-7107	319.5
1145	G29	-6323	202.5	1195	G129	-7123	202.5
1146	G31	-6339	319.5	1196	G131	-7139	319.5
1147	G33	-6355	202.5	1197	G133	-7155	202.5
1148	G35	-6371	319.5	1198	G135	-7171	319.5
1149	G37	-6387	202.5	1199	G137	-7187	202.5
1150	G39	-6403	319.5	1200	G139	-7203	319.5

FT1505C PAD coordinates 13 (Unit: um)

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
1201	G141	-7219	202.5	1251	G241	-8019	202.5
1202	G143	-7235	319.5	1252	G243	-8035	319.5
1203	G145	-7251	202.5	1253	G245	-8051	202.5
1204	G147	-7267	319.5	1254	G247	-8067	319.5
1205	G149	-7283	202.5	1255	G249	-8083	202.5
1206	G151	-7299	319.5	1256	G251	-8099	319.5
1207	G153	-7315	202.5	1257	G253	-8115	202.5
1208	G155	-7331	319.5	1258	G255	-8131	319.5

1209	G157	-7347	202.5	1259	G257	-8147	202.5
1210	G159	-7363	319.5	1260	G259	-8163	319.5
1211	G161	-7379	202.5	1261	G261	-8179	202.5
1212	G163	-7395	319.5	1262	G263	-8195	319.5
1213	G165	-7411	202.5	1263	G265	-8211	202.5
1214	G167	-7427	319.5	1264	G267	-8227	319.5
1215	G169	-7443	202.5	1265	G269	-8243	202.5
1216	G171	-7459	319.5	1266	G271	-8259	319.5
1217	G173	-7475	202.5	1267	G273	-8275	202.5
1218	G175	-7491	319.5	1268	G275	-8291	319.5
1219	G177	-7507	202.5	1269	G277	-8307	202.5
1220	G179	-7523	319.5	1270	G279	-8323	319.5
1221	G181	-7539	202.5	1271	G281	-8339	202.5
1222	G183	-7555	319.5	1272	G283	-8355	319.5
1223	G185	-7571	202.5	1273	G285	-8371	202.5
1224	G187	-7587	319.5	1274	G287	-8387	319.5
1225	G189	-7603	202.5	1275	G289	-8403	202.5
1226	G191	-7619	319.5	1276	G291	-8419	319.5
1227	G193	-7635	202.5	1277	G293	-8435	202.5
1228	G195	-7651	319.5	1278	G295	-8451	319.5
1229	G197	-7667	202.5	1279	G297	-8467	202.5
1230	G199	-7683	319.5	1280	G299	-8483	319.5
1231	G201	-7699	202.5	1281	G301	-8499	202.5
1232	G203	-7715	319.5	1282	G303	-8515	319.5
1233	G205	-7731	202.5	1283	G305	-8531	202.5
1234	G207	-7747	319.5	1284	G307	-8547	319.5
1235	G209	-7763	202.5	1285	G309	-8563	202.5
1236	G211	-7779	319.5	1286	G311	-8579	319.5
1237	G213	-7795	202.5	1287	G313	-8595	202.5
1238	G215	-7811	319.5	1288	G315	-8611	319.5
1239	G217	-7827	202.5	1289	G317	-8627	202.5
1240	G219	-7843	319.5	1290	G319	-8643	319.5
1241	G221	-7859	202.5	1291	DUMMY25	-8659	202.5
1242	G223	-7875	319.5				

1243	G225	-7891	202.5
1244	G227	-7907	319.5
1245	G229	-7923	202.5
1246	G231	-7939	319.5
1247	G233	-7955	202.5
1248	G235	-7971	319.5
1249	G237	-7987	202.5
1250	G239	-8003	319.5

Alignment Marks			
	1-a	-8751	269
	1-b	8751	269

6 Bump Arrangement

(1) I/O pin (No. 1 ~ No. 243)

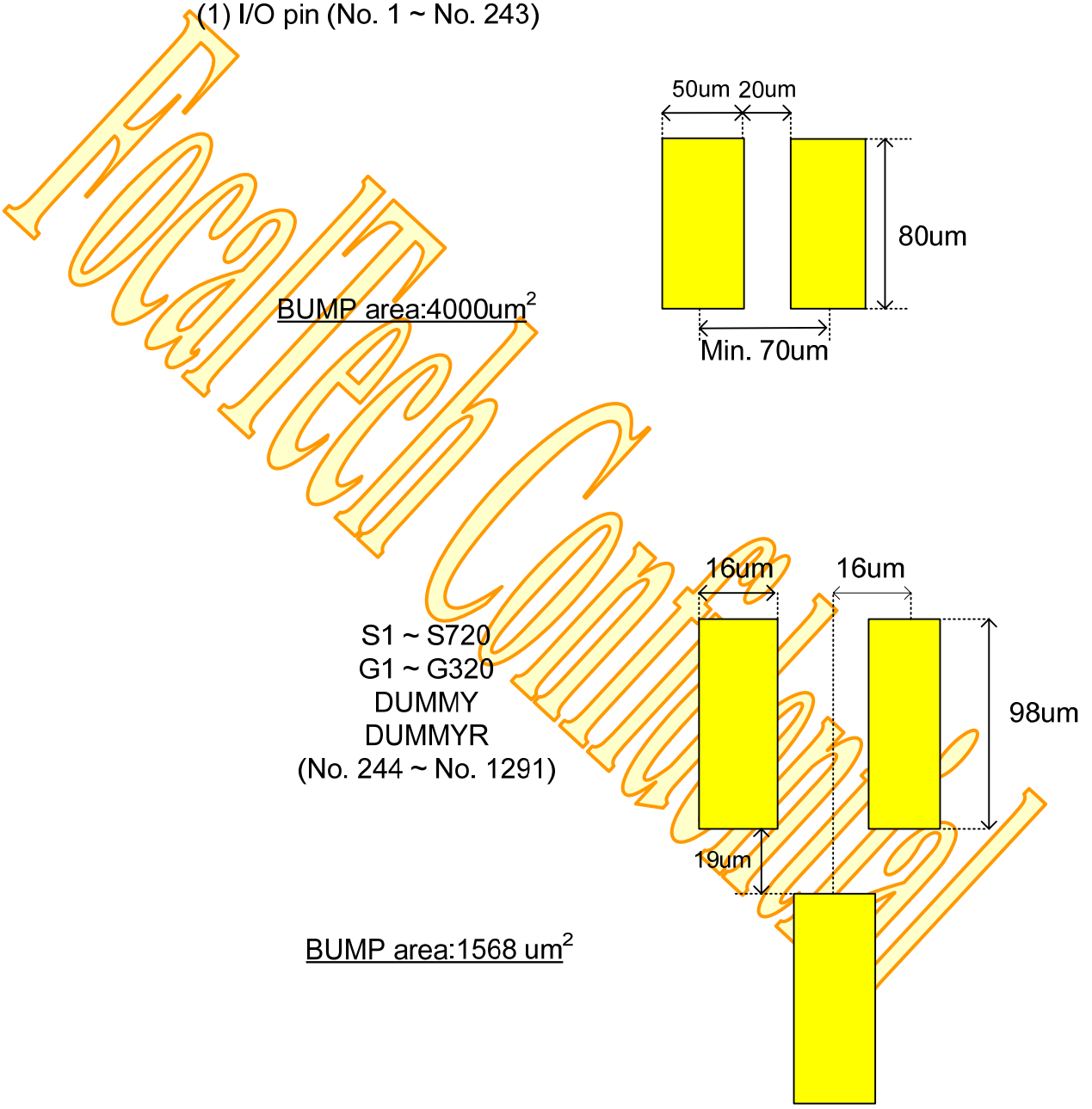


Figure 3

7 Block Function

7.1 System Interface

The FT1505C supports the following system interfaces: 80-system high-speed interface via 8-, 9-, 16-, 18-bit bus and clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The FT1505C has 16-bit index register (IR), 18-bit write-data register (WDR), and 18-bit read-data register (RDR). The IR is the register to store index information from control register and the internal GRAM. The WDR is the register to temporarily store the data to be written to the internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via the RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the FT1505C performs the first read operation from the internal GRAM. Valid data is read out when the FT1505C performs the second and subsequent read operations.

The instruction execution time except starting oscillation takes 0 clock cycle and instructions can be written consecutively.

Table 9 Register Selection (80-system 8/9/16/18-bit bus Interface)

WRN	RDN	RS	Function
0	1	0	Write index to IR
1	0	0	Read internal status
0	1	1	Write to control register/internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 10 Register Selection (clock synchronous serial interface - SPI)

Start byte

R/W	RS	Function
0	0	Write index to IR
1	0	Read internal status
0	1	Write to control register/internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

7.2 External Display Interface (VSYNC interfaces)

The FT1505C supports VSYNC interface as the moving picture display interface (external display interface). In VSYNC interface operation, the display operation is synchronized with the internal clock and VSYNC signal, which is used for frame synchronization. The display data is written to the internal GRAM via system interface but there are restrictions in setting the speed and the method to write data to the internal RAM. For details, see the "External Display Interface" section.

The FT1505C allows switching between the external display interface operation and the system interface operation by instruction so that the optimal interface is selected for the kind of picture on the panel (still and/or moving picture). The FT1505C writes the display data to the internal GRAM to enable transferring data only when the frame data is updated, which contributes to the reduction of data to be transferred from the system and power consumption required for moving picture display.

7.3 Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the address setting instruction is written in the IR, the address information is sent from the IR to the AC. When the data is written to the internal GRAM, the AC is automatically incremented (plus one) or decremented (minus one). The window address function enables writing data only within the rectangular area specified in GRAM by setting.

7.4 Graphics RAM (GRAM)

GRAM is graphics RAM, which is used to store graphic pattern data.

7.5 Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltages according to the grayscale data in the γ-correction registers to enable a maximum 262k-color display.

7.6 Timing Generator

The timing generator generates timing signals to operate internal circuits such as GRAM. The FT1505C generates timing signals for display operation such as the RAM read operation and for internal operation such as RAM access from MPU and outputs them separately to avoid mutual interference. Also FMARK is generated internally and output from the timing generator.

7.7 Oscillator (OSC)

The FT1505C generates the RC oscillation clock signal by internal RC oscillator. No external resistor is needed. Adjust the frame frequency by command setting. In deep standby mode, RC oscillation is halted to reduce power consumption. For details, see “Oscillator”.

7.8 Liquid crystal driver Circuit

The liquid crystal driver circuit of the FT1505C consists of a 720-channel source driver (S1 ~ S720) and a 320-output gate driver (G1 ~ G320). The display pattern data is latched when 720 bits of data are input. The latched data control the source driver and generates liquid crystal drive waveform. The shift direction of 720-bit source output from the source driver is determined by instruction (SS bit). The shift direction of gate output from the gate driver can be changed by setting the GS bit. The gate pin assignment can be changed by setting the SM bit. Set SM and GS bits to select the optimal scan mode for the module.

7.9 Internal logic power supply regulator

The internal logic power supply regulator generates internal power supply for RAM: VDD.

7.10 Liquid crystal drive power supply circuit

The liquid crystal drive power supply circuit generates the voltage levels to drive liquid crystal: VREG1OUT, DDVDH, VGL, VGH, VCOM.

8 System Interface

The following kinds of system interface are available with the FT1505C and the interface is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 54 IM bits settings and system interface

IM3	IM2	IM1	IM0	Interface operation	DB Pins	Colors
0	0	0	0	Setting disabled	-	-
0	0	0	1	Setting disabled	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	65,536 or 262,144 Note1
0	0	1	1	80-system 8-bit interface	DB17-10	65,536 or 262,144 Note2
0	1	0	ID	Clock synchronous serial interface	SDI/SDO	65,536
0	1	1	*	Setting disabled	-	-
1	0	0	0	Setting disabled	-	-
1	0	0	1	Setting disabled	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	262,144
1	0	1	1	80-system 9-bit interface	DB17-9	262,144
1	1	*	*	Setting disabled	-	-

Note 1: 65,536 colors in 1 transfer, 262,144 colors in 2 transfers
Note 2: 65,536 colors in 2 transfers, 262,144 colors in 3 transfers
Note 3: 'Setting disabled' option is operating under 80-system 18-bit interface.

8.1 80-system 18-bit interface

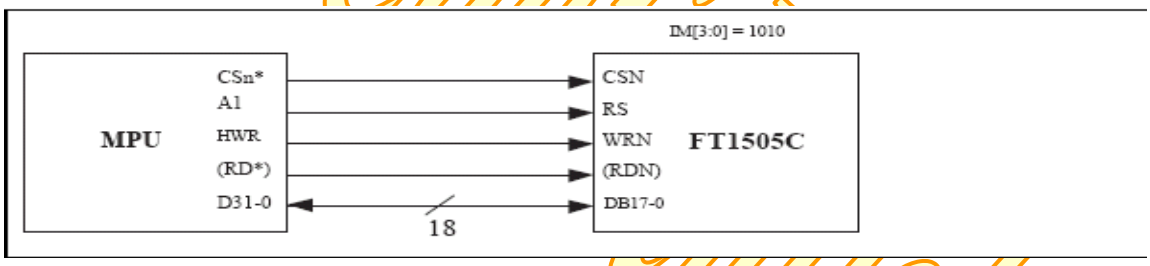


Figure 11

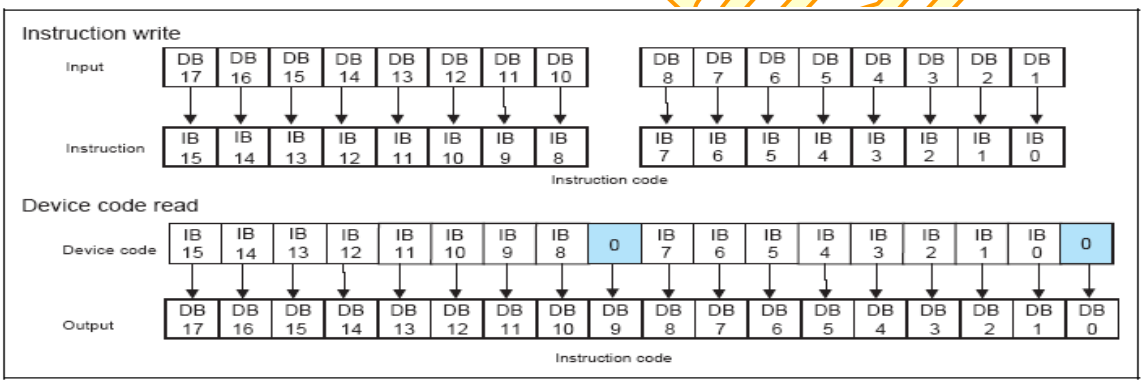


Figure 12: Instruction/Device code read (18-bit interface)

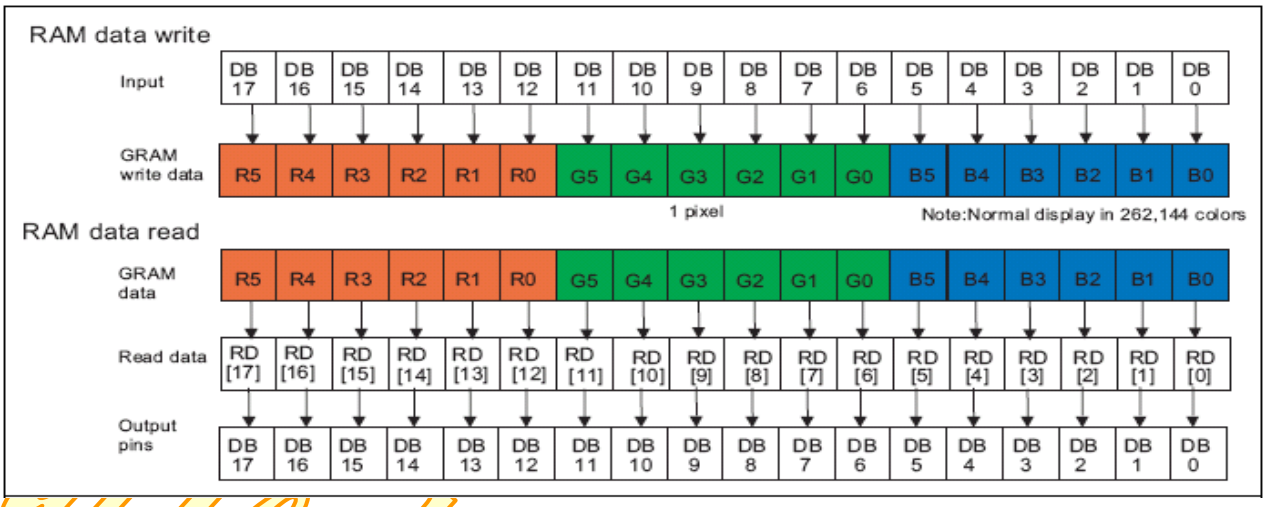


Figure 13: RAM data write/read (18-bit interface)

8.2 80-system 16-bit interface

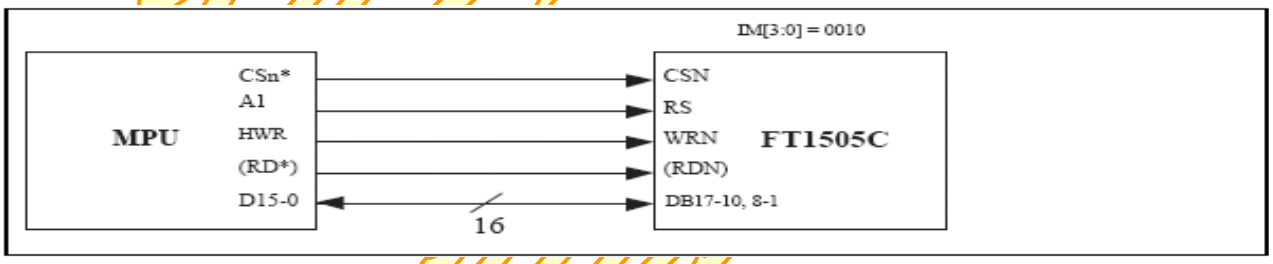


Figure 14

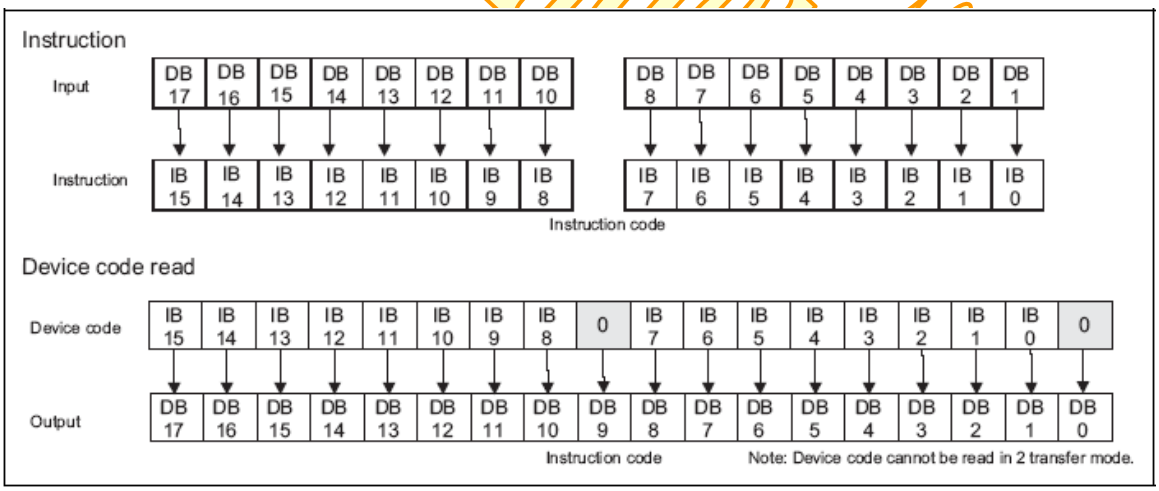


Figure 15: Instruction/Device code read (16-bit interface)

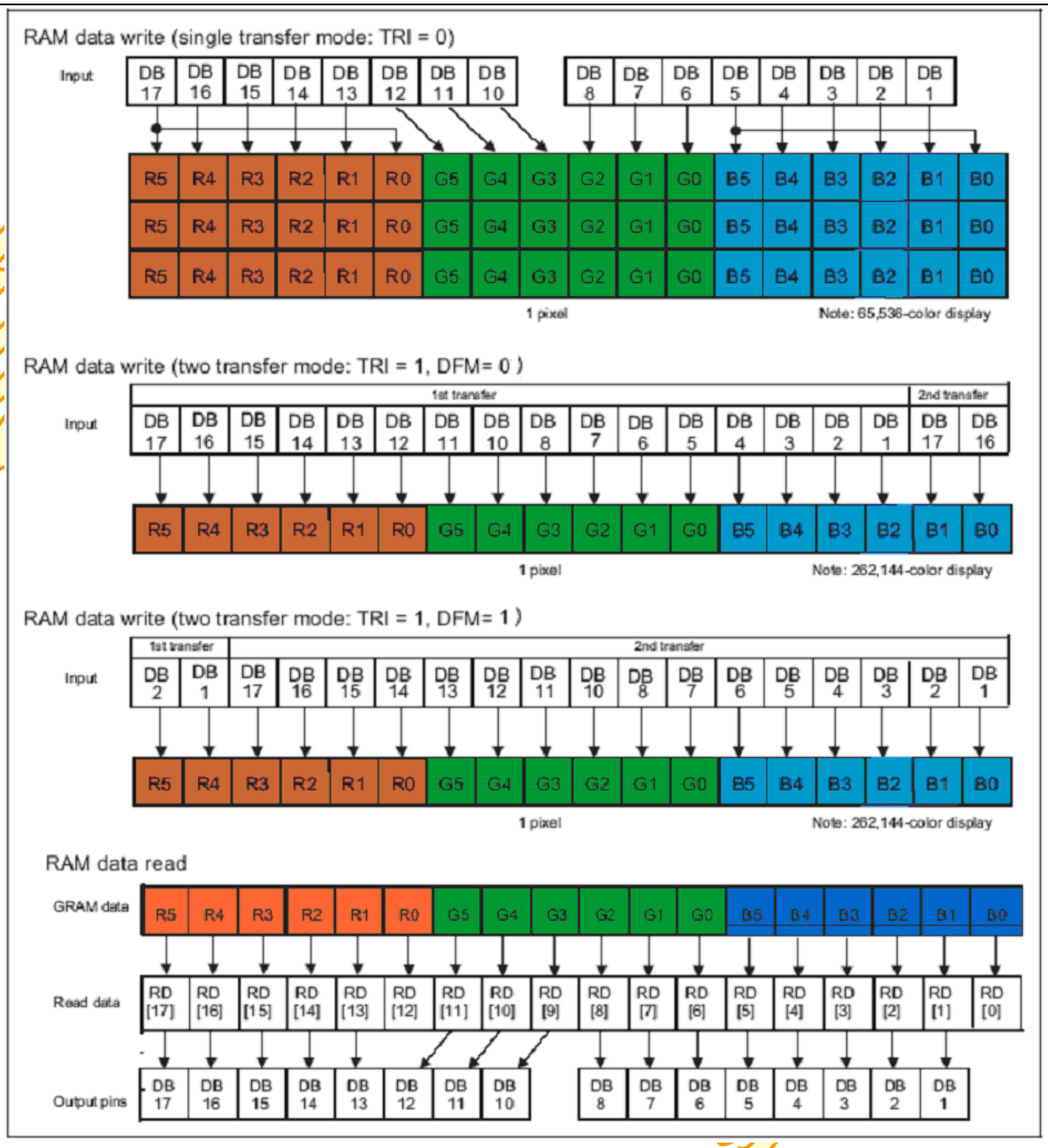


Figure 16: RAM data write/read (16-bit interface)

8.3 80-system 9-bit interface

When transferring 16-bit instruction via 9-bit interface (DB17~DB9), it is divided into upper and lower 8 bits (DB9 is not used) and the upper 8 bits are transferred first. The RAM write data are divided into upper and lower 9 bits and the upper 9 bits are transferred first. The unused DB8-0 pins must be fixed at either IOVcc or GND level. When writing in the index register, make sure to write the upper byte (8 bits).

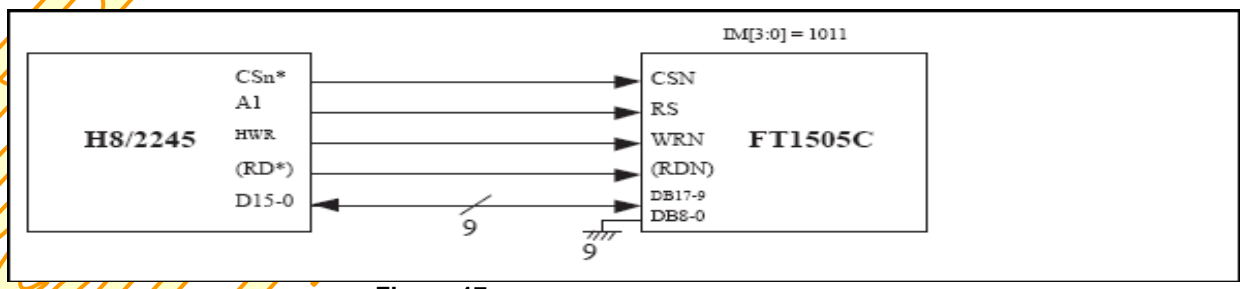


Figure 17

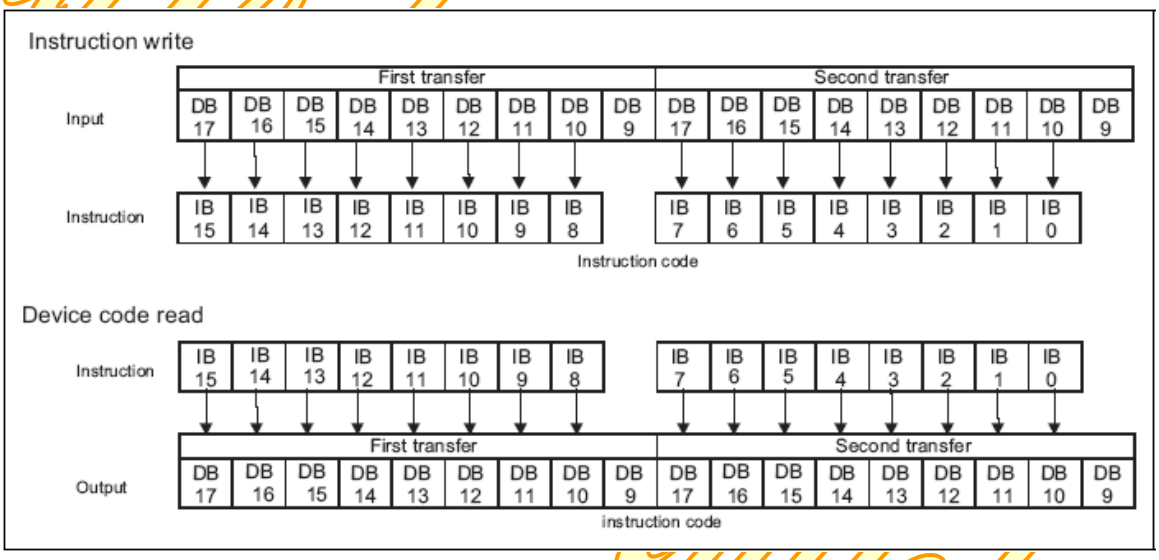


Figure 18: Instruction/Device code read (9-bit interface)

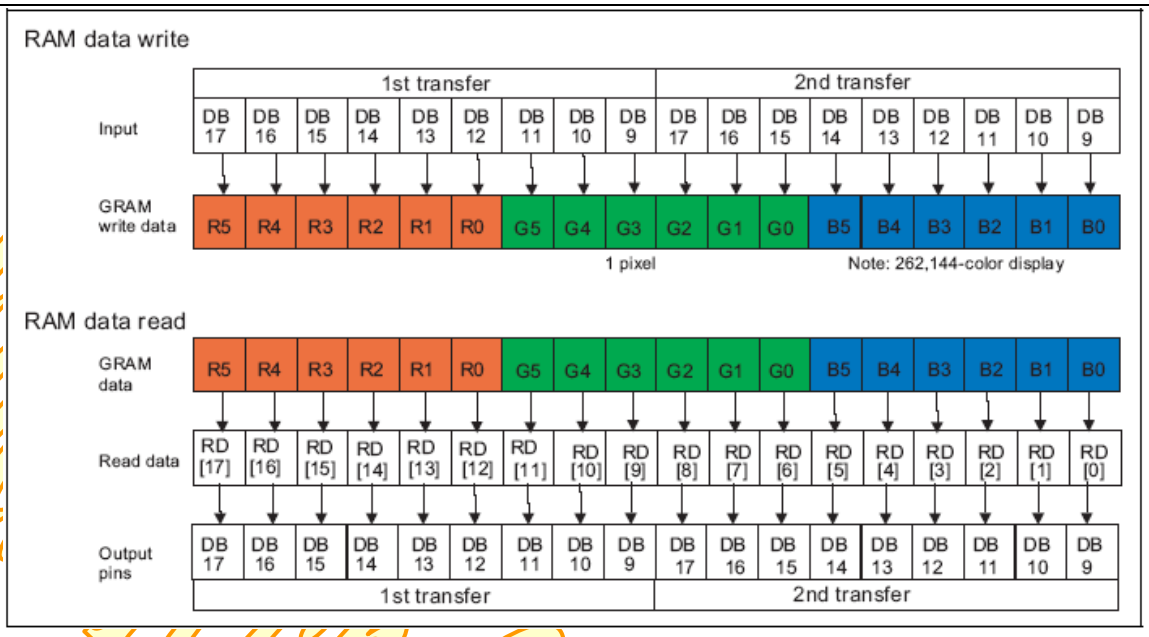


Figure 19: RAM data write/read (9-bit interface)

The FT1505C supports data transfer synchronization function to reset the counters, which count the number of upper and lower 9 bits when transferring data via 9-bit bus interface. If a mismatch occurs in transferring upper and lower 9 bits due to noise and so on, “00”H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 9 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

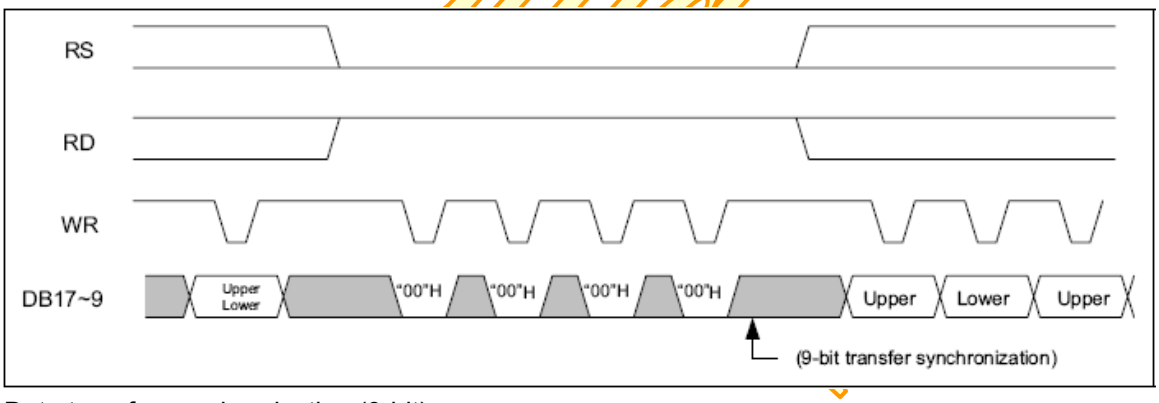


Figure 20: Data transfer synchronization (9-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

8.4 80-system 8-bit interface

When transferring 16-bit instruction via 8-bit interface (DB17~DB10), it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The RAM write data are divided into upper and lower 8 bits and the upper 8 bits are transferred first. The unused DB9-0 pins must be fixed at either IOVcc or GND level. When writing in the index register, make sure to write the upper byte (8 bits).

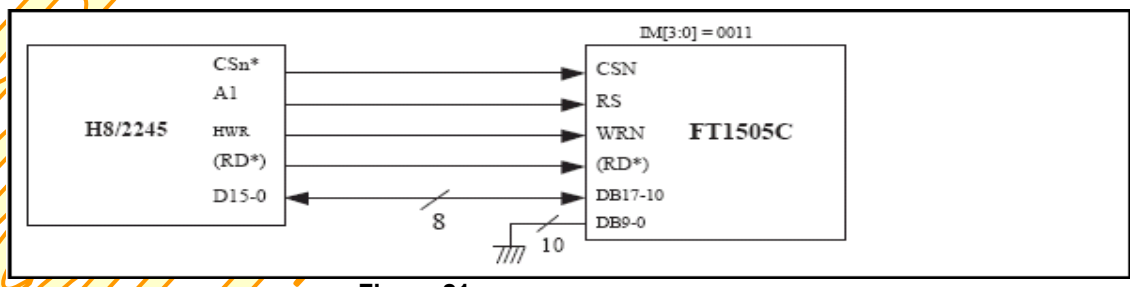
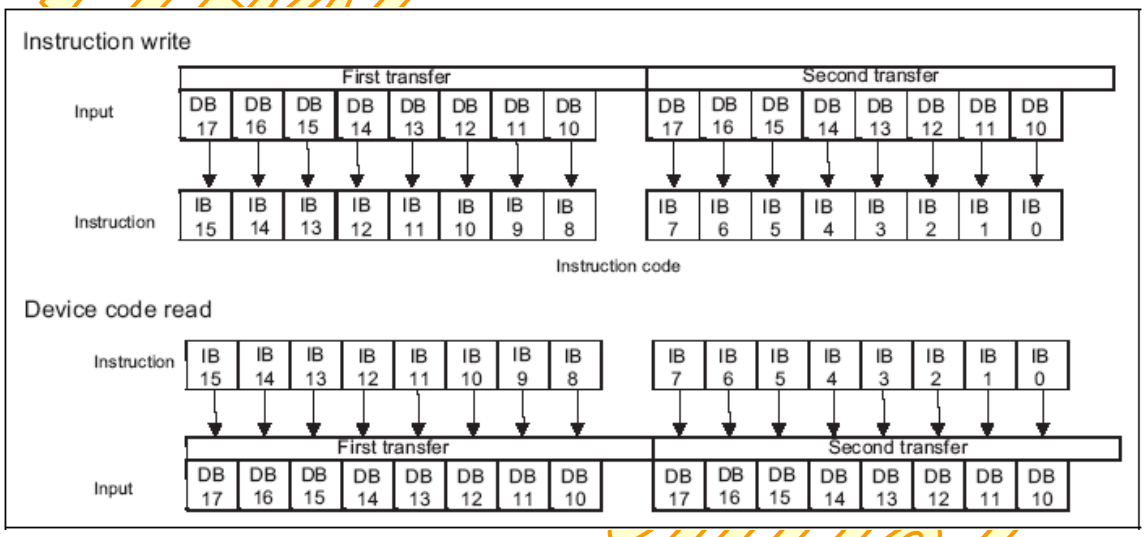
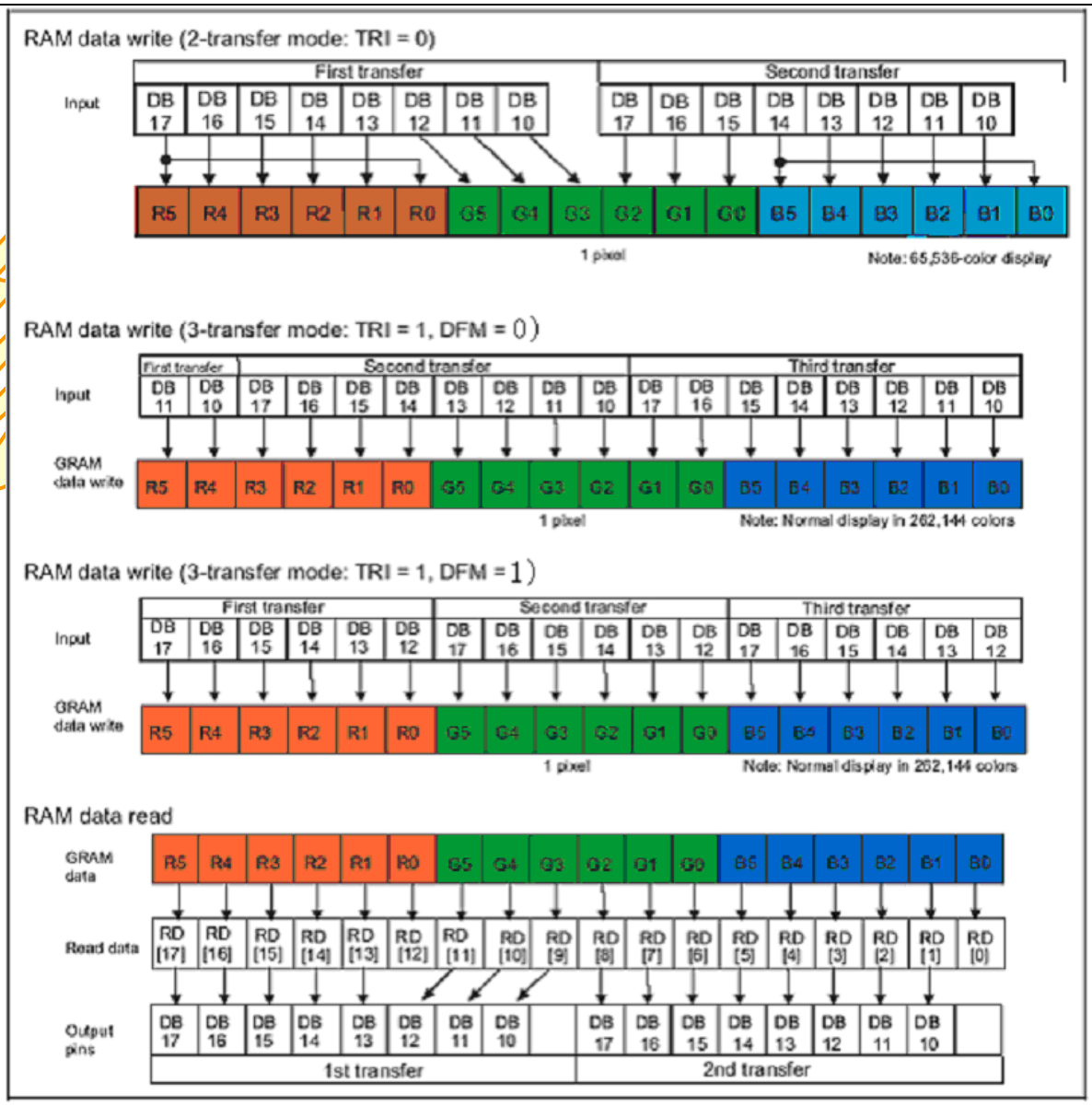


Figure 21



Note: Data cannot be read in 3-transfer mode.

Figure 22: Instruction/Device code read (8-bit interface)



Note: Data cannot be read in 3-transfer mode.

Figure 23: RAM data write/read (8-bit interface)

The FT1505C supports data transfer synchronization function to reset the counters, which count the number of upper and lower 8 bits when transferring data via 8-bit bus interface. If a mismatch occurs in transferring upper and lower 8 bits due to noise and so on, “00”H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 8 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

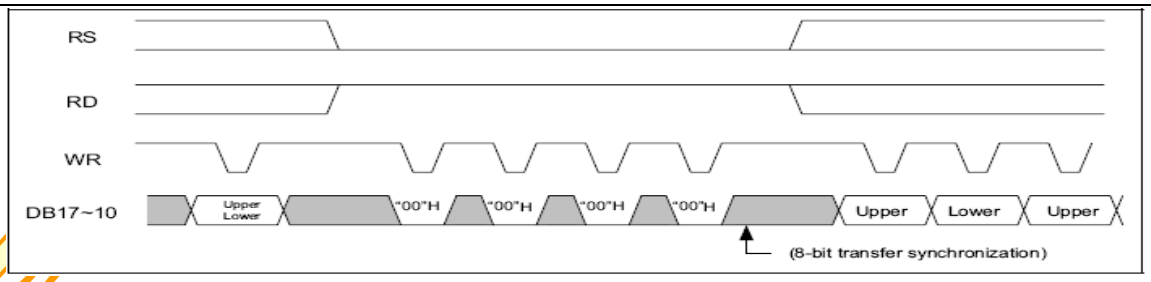


Figure 24: Data transfer synchronization (8-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

8.5 Serial interface

The serial interface is selected by setting the IM3/2/1 pins to GND/IOVcc/GND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The FT1505C recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The FT1505C is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the FT1505C are compared and both 6-bit data match. Then, the FT1505C starts taking in subsequent data. The least significant bit of the device identification code is determined by setting the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the FT1505C because the seventh bit of the start byte is register select bit (RS). When RS = 0, either index register write or status read operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The FT1505C receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The FT1505C writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the FT1505C starts transferring or receiving data in units of bytes. The FT1505C transfers data from the MSB. The FT1505C's instruction consists of 16 bits and it is executed inside the FT1505C after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The FT1505C expands RAM write data into 18 bits when writing them to the internal GRAM. The first byte received by the FT1505C following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the GRAM, valid data is not transferred to the data bus until first five bytes of data are read from the GRAM following the start byte. The FT1505C sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 55 Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The ID bit is selected by setting the IM0/ID pin.

Table 56

RS	R/W	Function
0	0	Set index register
0	1	Read status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

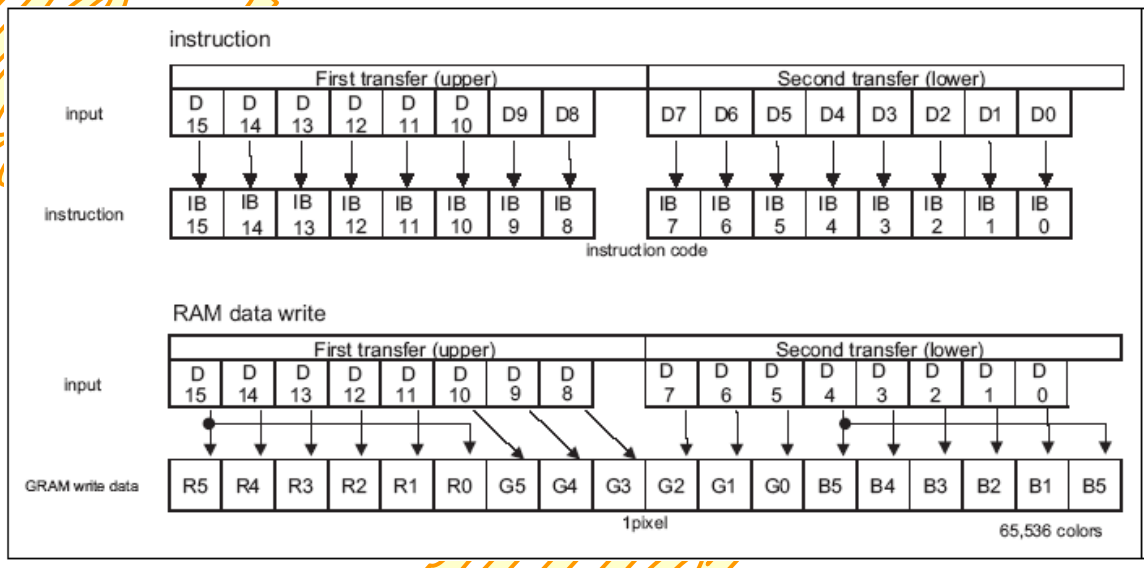


Figure 25

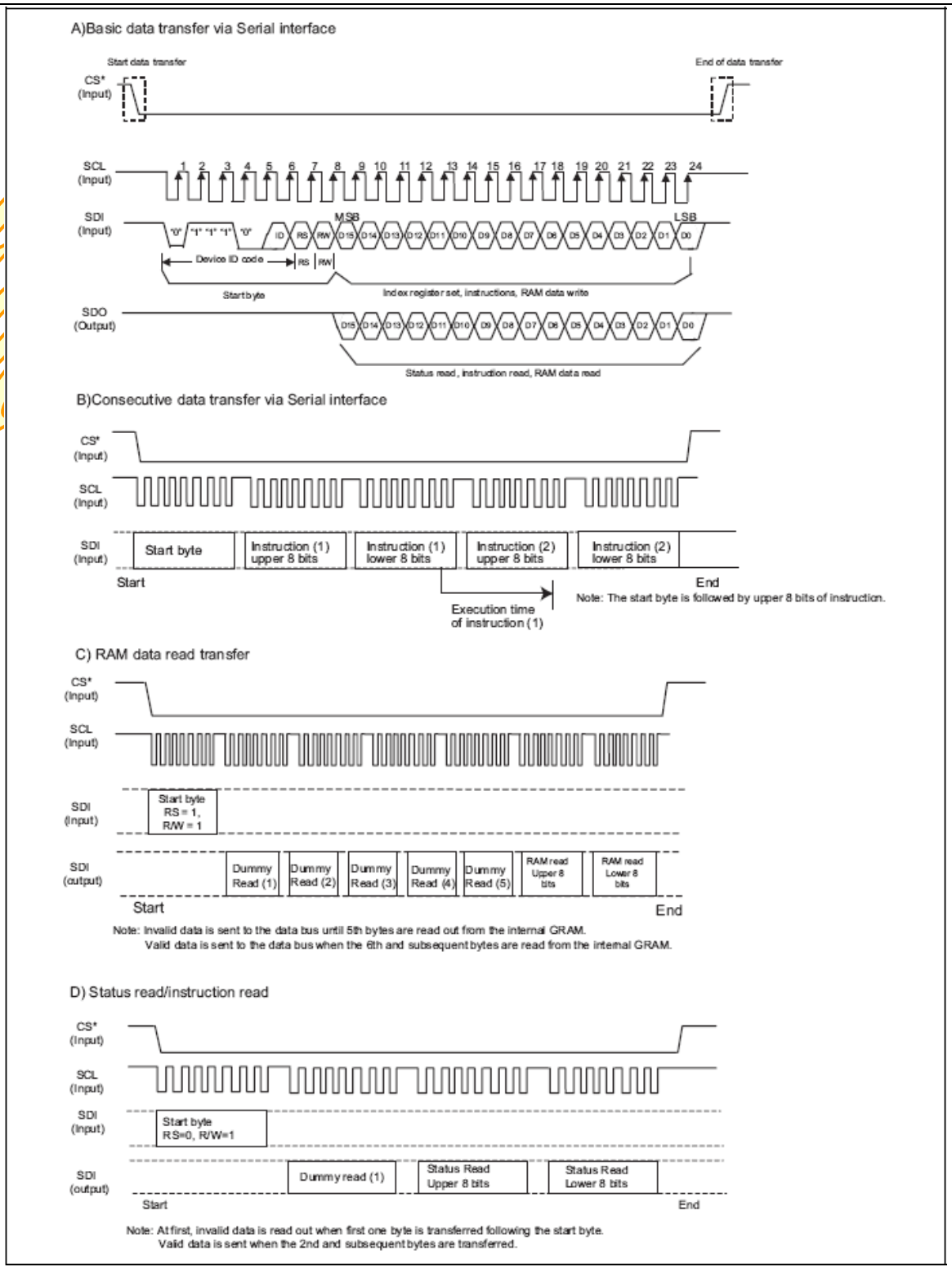


Figure 26: Serial interface data transfer timing

8.6 VSYNC Interface

The FT1505C supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

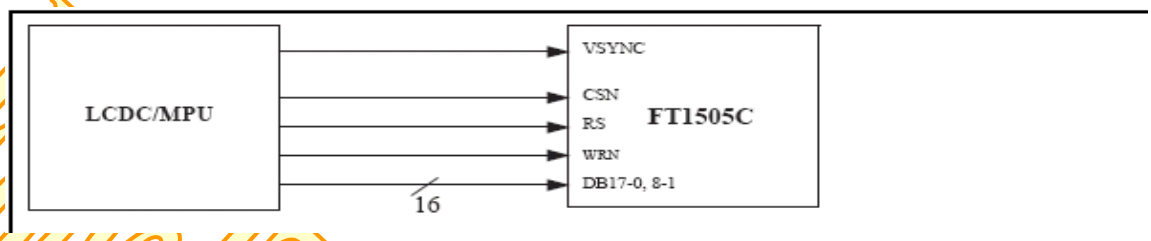


Figure 27: VSYNC interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the FT1505C rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

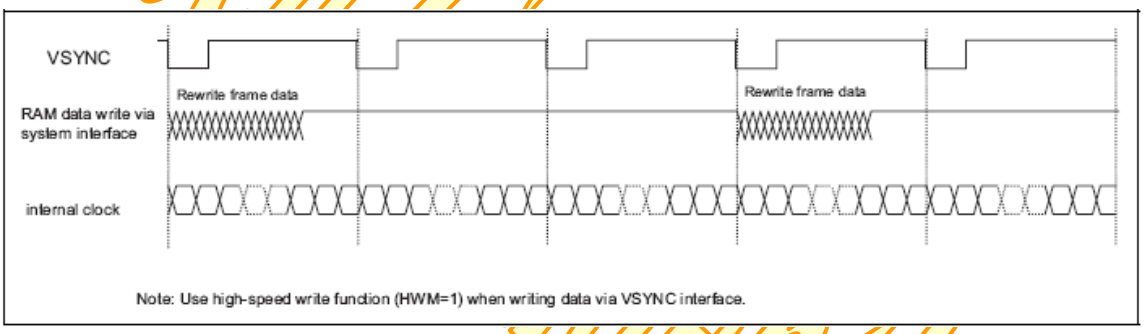


Figure 28: Moving picture data write via VSYNC

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$Internal\ clock\ frequency\ (fosc)\ [Hz]$$
$$= FrameFrequency \times (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) \times 16(clocks) \times \text{variance}$$

$$RAMWriteSpeed(\min.)[Hz] > \frac{240 \times DisplayLines(NL)}{(BackPorch(BP) + DisplayLines(NL) - \text{margins}) \times 16(clocks) \times \frac{1}{fosc}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Display size: 240 RGB × 320 lines

Display lines: 320 lines (NL=6'h27: 320 lines)
Back/front porch: 14/2 lines (BP = 4'b1110/ FP = 4'b0010)
Frame frequency: 60 Hz

Internal clock/oscillator frequency (fosc) [Hz]
= 60 Hz × (320 + 2 + 14) lines × 16 clocks × 1.1 / 0.9 = 394 kHz

Notes: 1. When setting the internal clock/oscillator frequency (through register RC[2:0]), possible causes of fluctuation must also be taken into consideration. In this example, the internal clock/oscillator frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz] > 240 × 320 / {((14 + 320 - 2) lines × 16 clock) /394 kHz} = 5.7 MHz

Notes: 1. In this example, it is assumed that the FT1505C starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the FT1505C has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 5.7MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the FT1505C starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

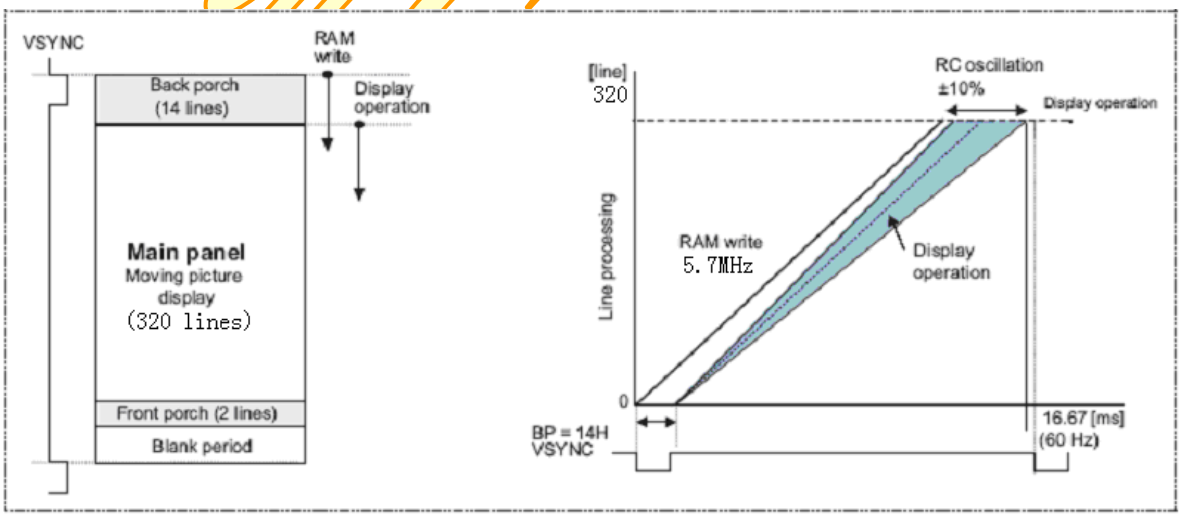


Figure 29: Write/display operation timing via VSYNC interface

Notes to VSYNC Interface operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margins in setting RAM write speed for VSYNC interface operation.
2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

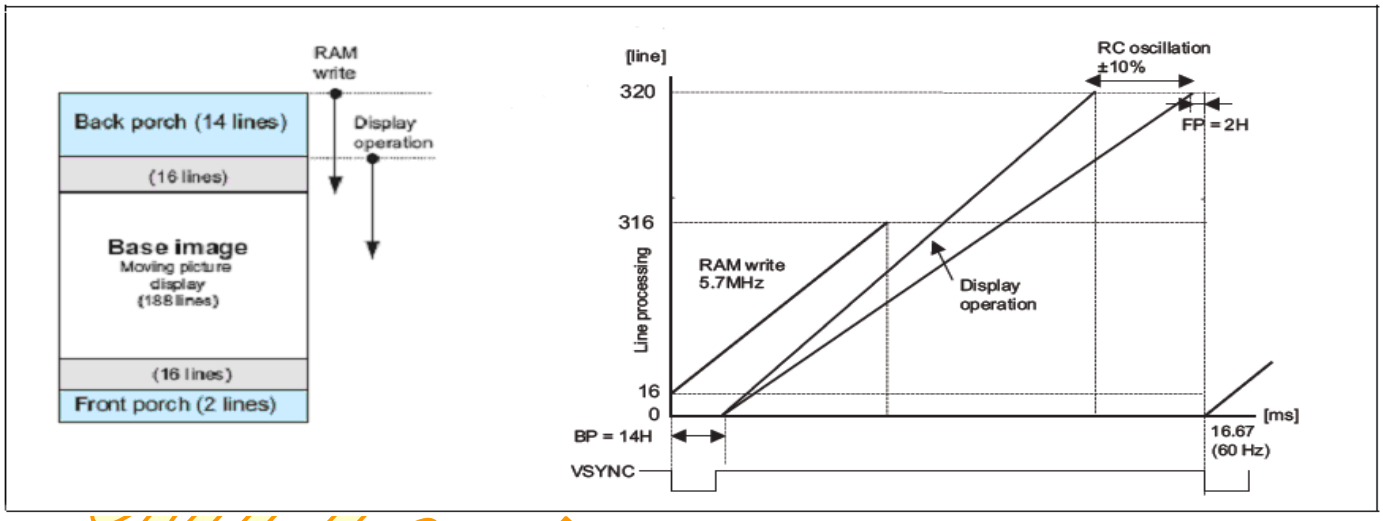


Figure 30: RAM write speed margin

3. The front porch period continues from the end of one frame period to the next VSYNC input.
4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.
5. The partial display and vertical scroll functions and interlaced scan are not available in VSYNC interface operation.
6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.

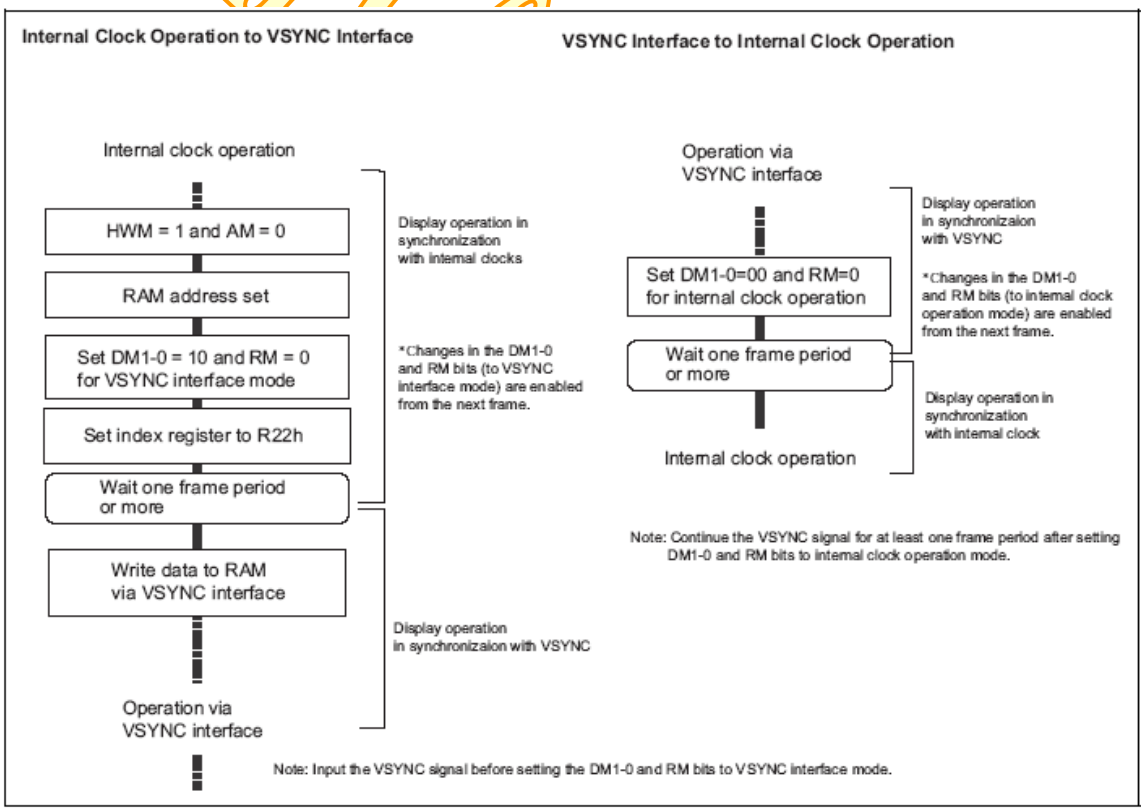


Figure 31: Sequence to switch between VSYNC and Internal clock operation modes

8.7 External Display Interface

8.7.1 RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function and high-speed write mode (HWM = 1). In RGB interface operation, front and back porch periods must be made before and after the display period.

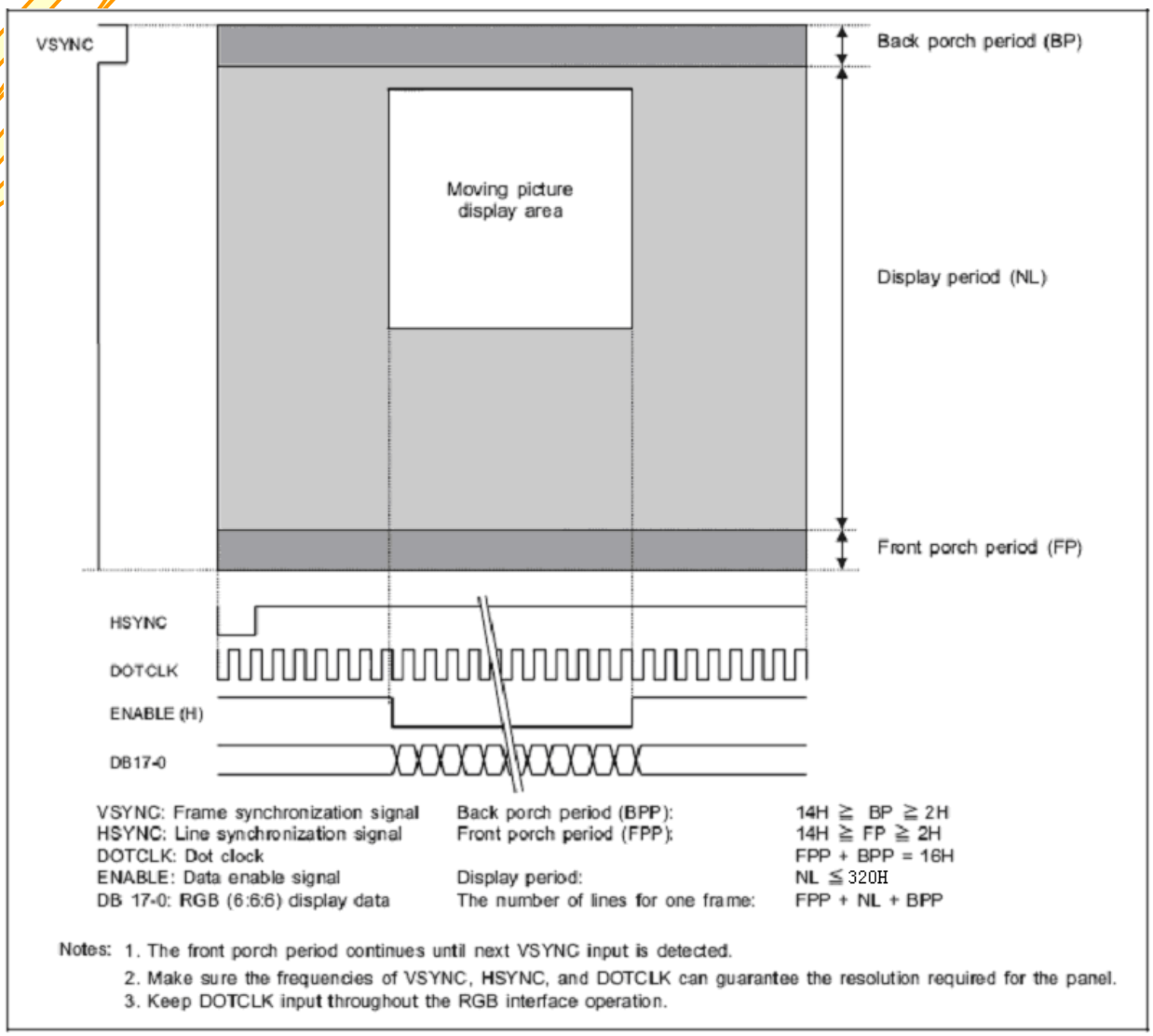


Figure 32: Display Operation Via RGB interface

8.7.2 ENABLE signal function

The following table shows the relationship between the ENABLE, EPL setting and RAM access operation. Whenever the FT1505C performs write operation, ENABLE must be "Low" to allow write operation but this is not the determinant of enabling automatic address update in RAM write operation. EPL controls the active polarity of ENABLE signal.

Table 58

EPL	ENABLE	RAM write	RAM address
0	0	Enable	Update
0	1	Disable	Retain
1	0	Disable	Retain
1	1	Enable	Update

8.7.3 RGB interface timing

Signal timing chart of 16/18-bit RGB interface

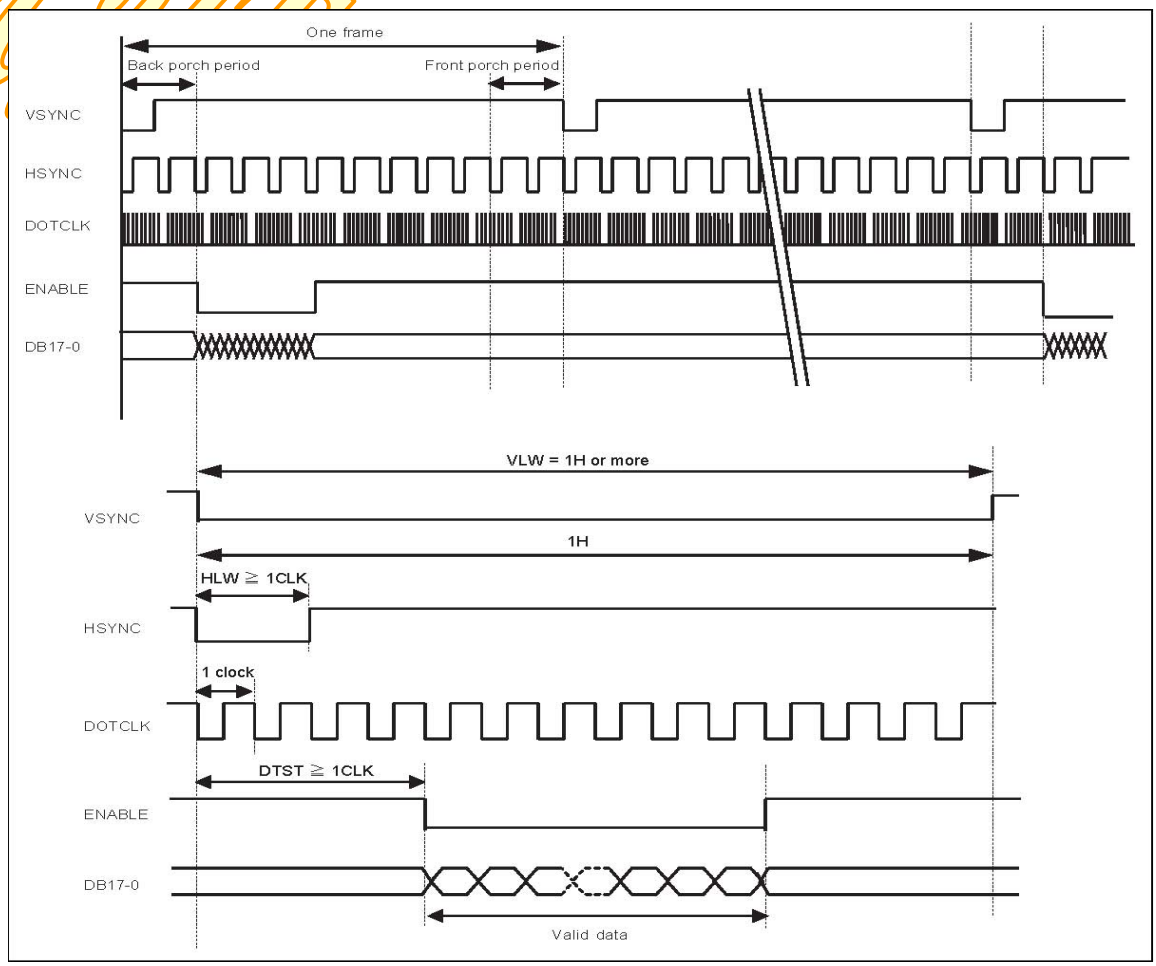


Figure 33

Notes 1: VLW: VSYNC "Low" period HLW: HSYNC "Low" period DTST: data transfer setup time

2: Use high-speed write function (HWM = "1") when writing data via RGB interface.

Timing chart of signals in 6-bit RGB interface operation

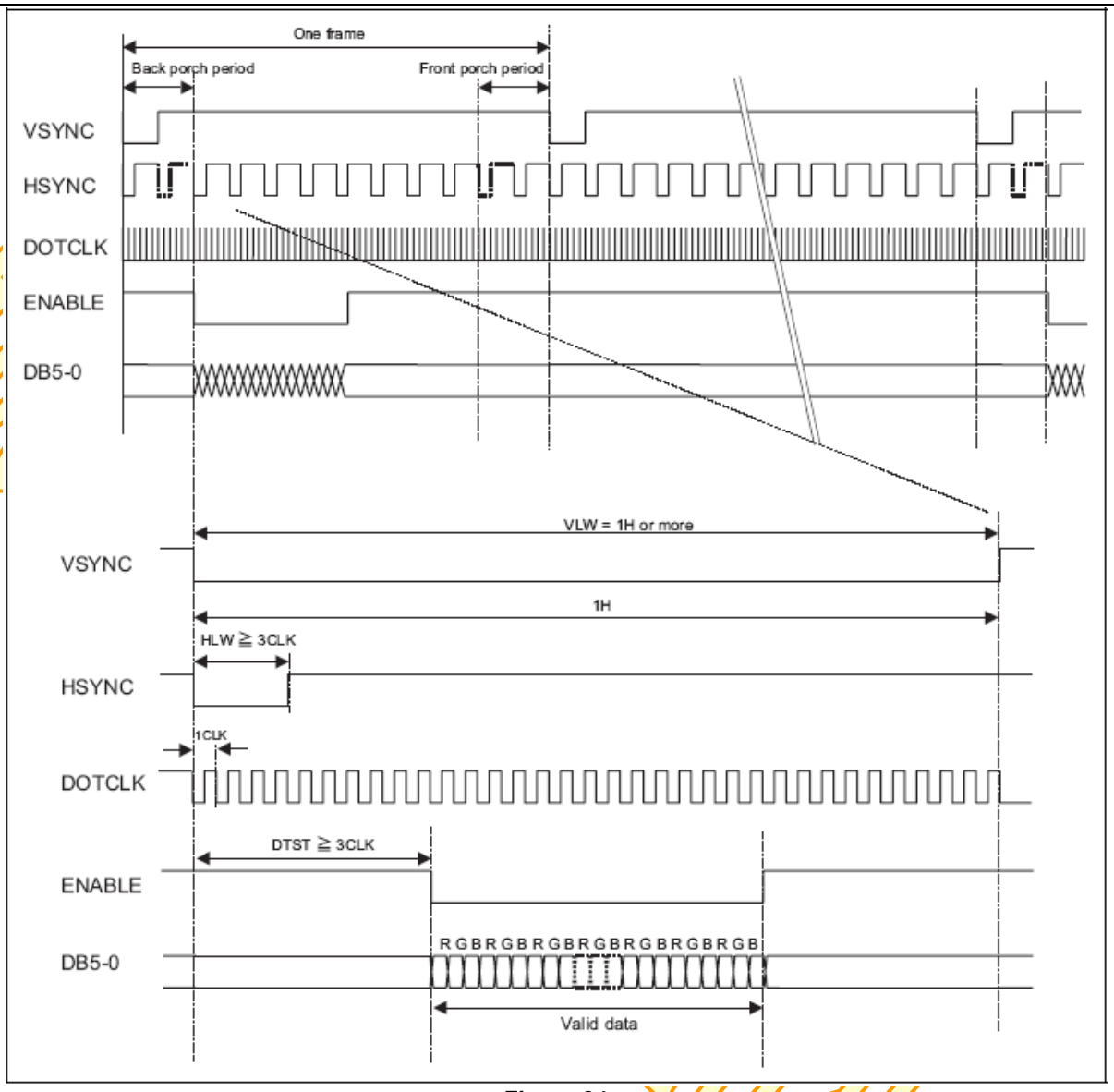


Figure 34

Notes 1: VLW: VSYNC “Low” period HLW: HSYNC “Low” period DTST: data transfer setup time

2: Use high-speed write function (HWM = “1”) when writing data via RGB interface.

3: In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so that one pixel data is transferred in units of three clocks via DB5-0.

8.7.4 Moving Picture Display via RGB Interface

The FT1505C supports RGB interface for moving picture display and incorporates RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. It becomes possible to transfer only the data written over the moving picture area
4. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
5. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

8.7.5 RAM access via system interface in RGB interface operation

The FT1505C allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. Then set RM = "0" to enable RAM access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = "1" and the index register to R22h to start accessing RAM via RGB interface. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

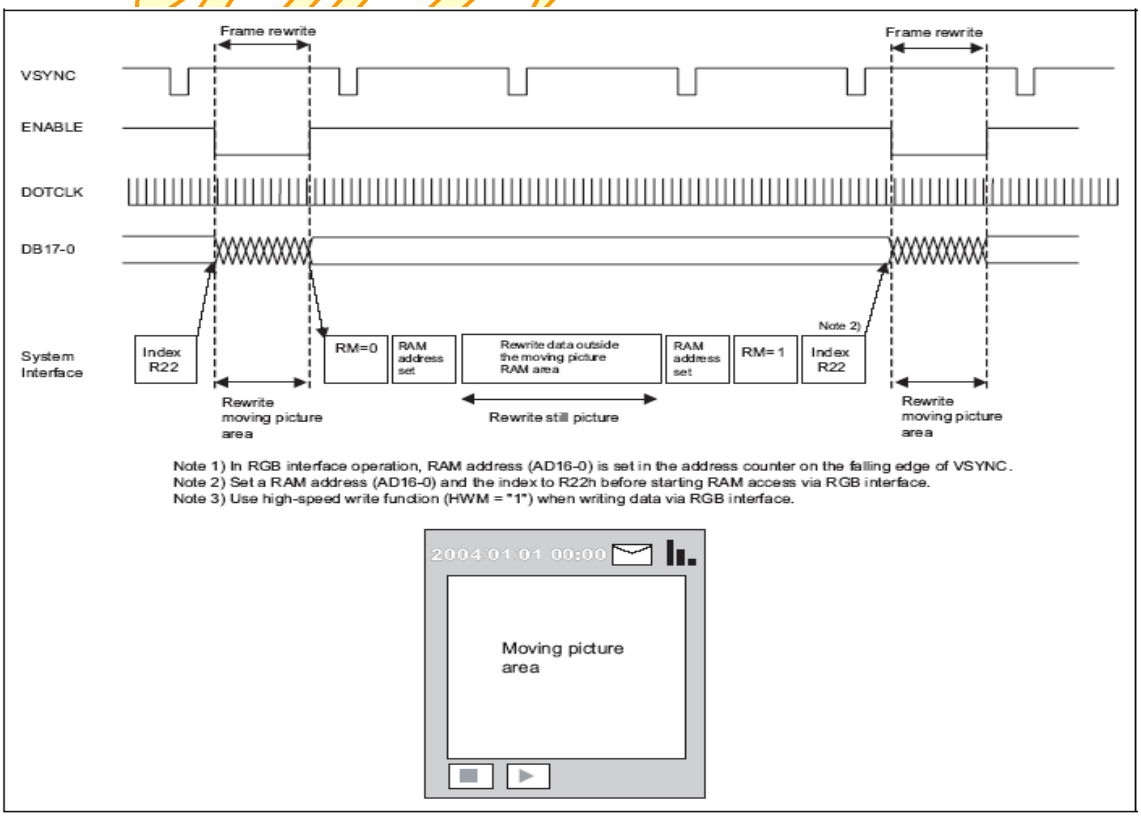


Figure 35: Updating a still picture area while displaying a moving picture

8.7.6 6-bit RGB interface

The 6-bit RGB interface is selected by setting the RIM1-0 bits to 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus (DB5-0) while the data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins (DB17 to 6) must be fixed at either IOVcc or GND level.

Instruction bits can be transferred only via system interface.

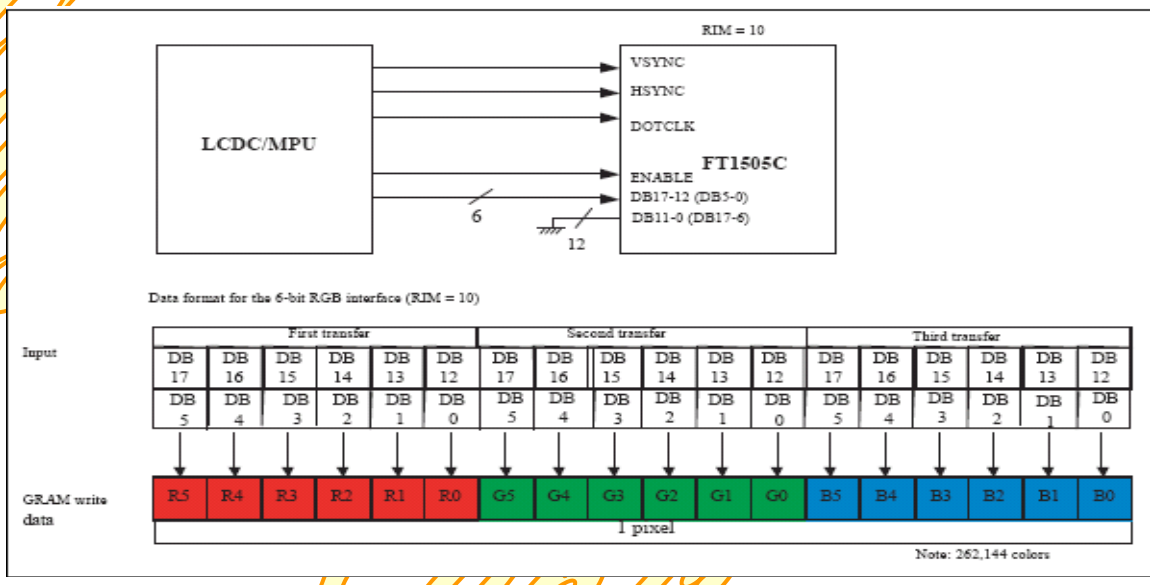


Figure 36: 6-Bit RGB Interface and data format

Data transfer synchronization in 6-bit RGB interface operation

The FT1505C has the counters, which count the first, second, third 6 bit transfers via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

Make sure the internal display operation within the FT1505C is performed in units of pixels and input 3 DOTCLK to transfer one pixel data (RGB) via 6-bit interface. If the number of DOTCLK inputted in one frame period does not satisfy this condition, data transfer mismatch will occur and its effect will be carried over to the next frame.

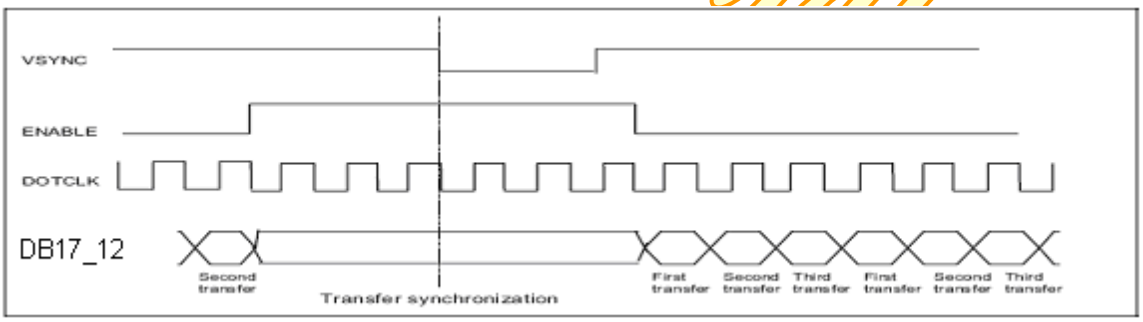


Figure 37: 6-bit Transfer Synchronization

8.7.7 16-bit RGB interface

The 16-bit RGB interface is selected by setting the RIM1-0 bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-10, DB8-1) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

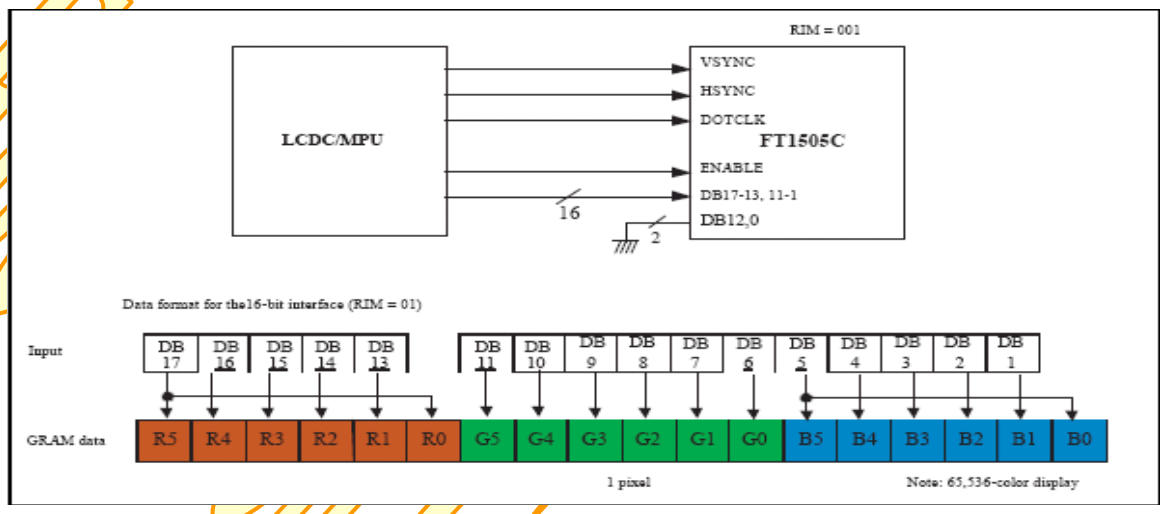


Figure 38: 16-Bit RGB Interface and data format

8.7.8 18-bit RGB interface

The 18-bit RGB interface is selected by setting the RIM1-0 bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

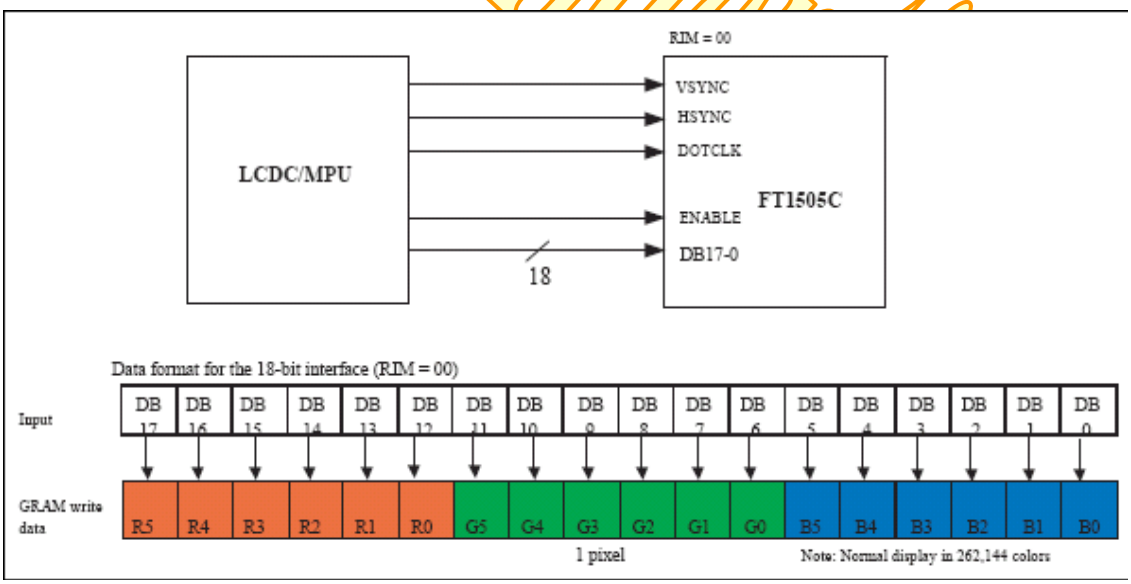


Figure 39: 18-Bit RGB Interface and data format

8.7.9 Notes to external display interface operation

1. The following functions are not available in external display interface operation.

Table 59 Functions Not Available in External Display Interface operation

Function	External Display Interface	Internal Clock Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The reference clock, which is used for determining the periods set by NOE[1:0], STDE[1:0], EQE[1:0] bits in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.
4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel data.
5. In 6-bit RGB interface operation, make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE signals so that the data transfer via DB5-0 is completed in units of pixels.
6. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.
7. In RGB interface operation, front porch period continues after the end of frame period until next VSYNC input is detected.
8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to GRAM.
9. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

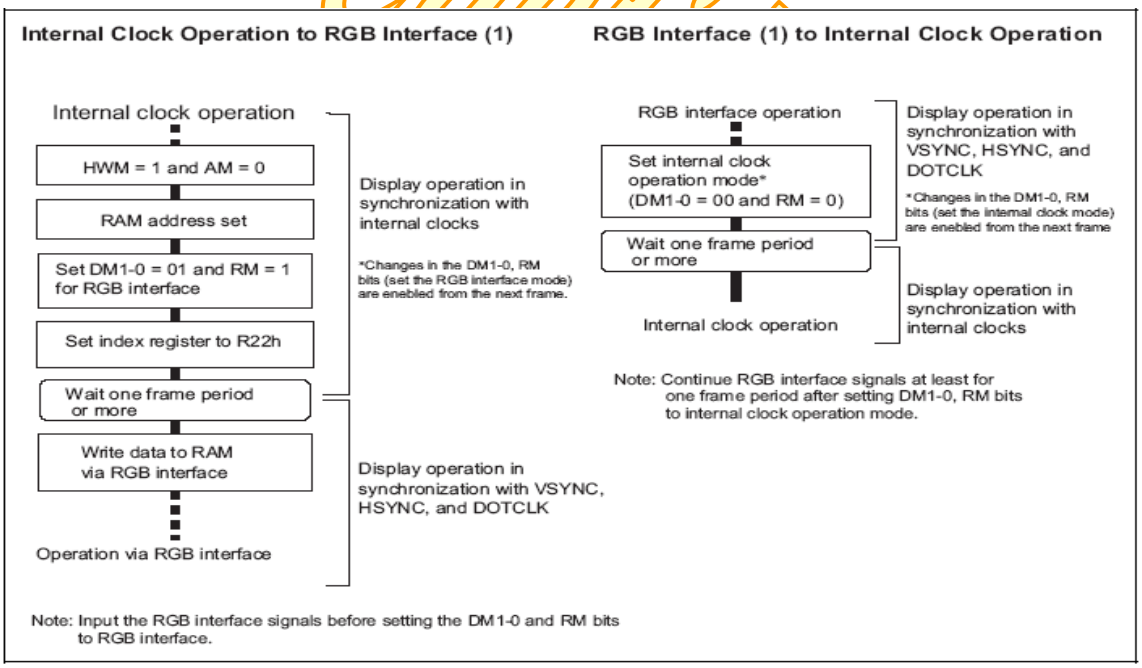


Figure 40: RGB interface operation and internal clock operation transition

9 GRAM Address MAP

Table 11 GRAM Address and Display Position on the Panel (SS= “0”, BGR= “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	……	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			..	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			..	h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			..	h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			..	h002EC			h002ED			h002EE			h002EF		
G4	G317	h00300			h00301			h00302			h00303			..	h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			..	h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			..	h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			..	h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			..	h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			..	h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			..	h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			..	h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			..	h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			..	h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			..	h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			..	h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			..	h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			..	h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			..	h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			..	h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			..	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:			..	:			:			:			:		
G305	G16:	h13000			h13001			h13002			h13003			..	h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			..	h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			..	h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			..	h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			..	h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			..	h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			..	h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			..	h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			..	h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			..	h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			..	h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			..	h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			..	h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			..	h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			..	h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			..	h13FEC			h13FED			h13FEE			h13FEF		

Table 12 GRAM Address and Display Position on the Panel (SS= “1”, BGR= “1”)

S/G pin		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	.....	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			..	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			..	h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			..	h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			..	h002EC			h002ED			h002EE			h002EF		
G4	G317	h00300			h00301			h00302			h00303			..	h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			..	h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			..	h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			..	h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			..	h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			..	h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			..	h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			..	h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			..	h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			..	h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			..	h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			..	h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			..	h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			..	h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			..	h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			..	h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			..	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:			..	:			:			:			:		
G305	G16:	h13000			h13001			h13002			h13003			..	h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			..	h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			..	h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			..	h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			..	h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			..	h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			..	h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			..	h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			..	h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			..	h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			..	h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			..	h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			..	h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			..	h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			..	h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			..	h13FEC			h13FED			h13FEE			h13FEF		

10 Instruction

The FT1505C adopts 18-bit bus architecture to interface to high-performance microcomputer. The FT1505C starts internal processing when the control information sent via 18-, 16-, 9-, 8-bit ports is stored in the instruction register (IR) and the data register (DR). Since the internal operation of the FT1505C is controlled by the signals sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signals (IB15 to IB0) are called instruction. The FT1505C accesses the internal GRAM in units of 18 bits. The instructions of the FT1505C are categorized into the following 8 groups.

1. Index specification
2. Status Read
3. Display control
4. Power management control
5. GRAM address setting
6. Transfer data to/from the internal GRAM
7. γ-correction
8. EPROM control

Normally, the instruction to write data in the GRAM is used the most often. In order to minimize the data transfer and lessen the programming load on the microcomputer, the FT1505C rewrites data only within the window address area and updates internal GRAM address in the address counter automatically as it writes data in the internal GRAM. The FT1505C writes instruction consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycle).

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

10.1 Instruction data format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface as shown below.

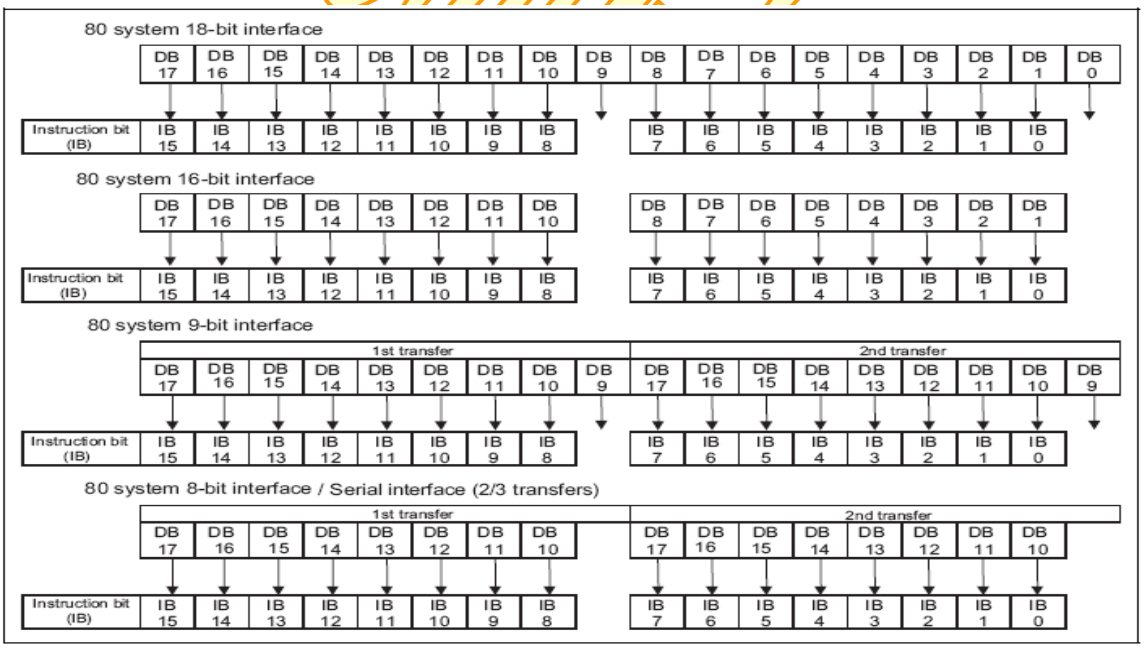


Figure 4: Instruction format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface (see Figure 10 Instruction format).

10.2 Index specification/Status read/Display control instructions

10.2.1 Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register represents the index of the control register to be accessed (R00h ~ RFFh) and for RAM control using binary numbers from “0000_0000” to “1111_1111”. The access to a register and instruction bits in it is prohibited unless the index is specified in the index register.

10.2.2 Status read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The internal status of the FT1505C can be read out from the SR register.

L[7:0]: represents the line where the FT1505C drives liquid crystal.

10.2.3 Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The start oscillation instruction starts the oscillator from a halt in standby mode. After executing this instruction, wait at least 10 ms to stabilize the oscillator before issuing next instruction.

*The device code “0001”H is read out when reading out this register.

10.2.4 Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shift from S1 to S720.

When SS = “1”, the source driver output shift from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S720.

When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S720 to S1.

When changing the SS and BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module. See “Scan mode setting”.

10.2.5 LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

EOR: By setting EOR = "1", the polarity of C pattern waveform (n-line inversion waveform) is inverted according to the result of EOR (exclusive OR) between the odd/even-number frame select signal and the n-line inversion signal. Set EOR = 1 when the number of lines to drive liquid crystal is not compatible with n-line inversion waveform. For details, see "n-line inversion AC drives".

B/C: When B/C = "0", the liquid crystal drive signal becomes frame-inversion waveform and inverts the polarity of liquid crystal in every frame cycle. When B/C = "1", liquid crystal drive signal becomes n-line inversion waveform and inverts the polarity of liquid crystal in every (n+1)-line cycle. For details, see "n-line inversion AC drives".

10.2.6 Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the FT1505C writes data in the internal GRAM.

AM= "0", sets the horizontal direction.

AM = "1", sets the vertical direction.

When a window address area is specified in GRAM, the FT1505C writes data within the window address area in the direction determined by the I/D1-0, AM settings.

I/D[1:0]: The RAM address is automatically incremented (+1) when I/D = "1" and decremented (-1) when I/D = "0" as the FT1505C writes data in the GRAM. The I/D[0] bit sets either increment or decrement of RAM address (AD[7:0]) in horizontal direction. The I/D[1] bit sets either increment or decrement of RAM address (AD[15:8]) in vertical direction. (**Recommended value: I/D[1]="1"**)The AM bit sets either horizontal or vertical direction in updating RAM address automatically when writing data in the internal RAM.

BGR: Reverses the order of assigning 18-bit RGB data to the data bus (DB17-0) from RGB to BGR

DFM: In combination with the TRI setting, sets the interface format to transfer 18-bit data via 80-system 16-/8-bit bus interface. Make sure to set DFM = "0", when not using 16-/8-bit interface.

TRI: Sets the interface format when transferring 18-bit data via 80-system 16-/8-bit interface in combination with DFM bit.

In 8-bit interface operation, TRI =0: 16-bit RAM data is transferred in two transfers via 8-bit interface.

TRI =1: 18-bit RAM data is transferred in three transfers via 8-bit interface.

In 16-bit interface operation, TRI =0: 16-bit RAM data is transferred in one-transfer via 16-bit interface. TRI =1: 18-bit RAM data is transferred in two transfers via 16-bit interface.

Make sure to set TRI = "0", when not using 16-/8-bit interface. Also, set TRI = "0" in read operation.

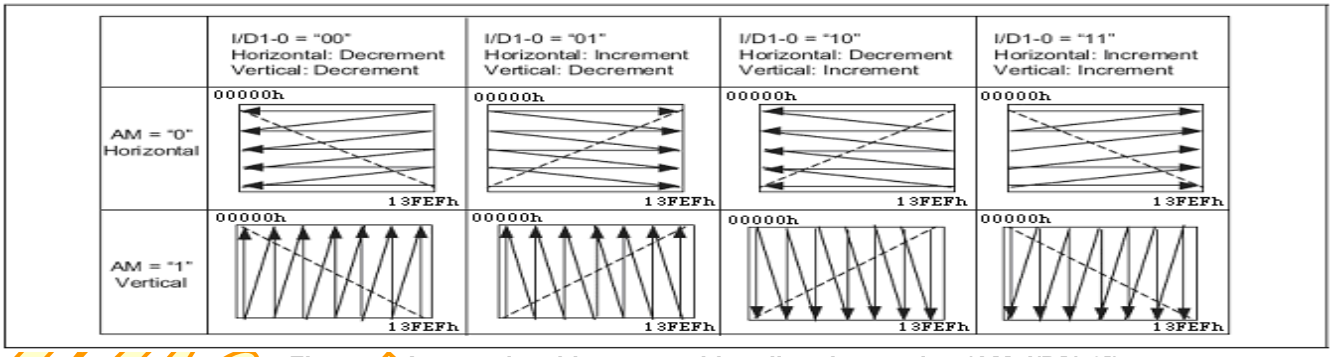


Figure 5: Automatic address transition direction setting (AM, I/D[1:0])

Note: When a window address area is specified in the GRAM, the data is written within the window address area.

10.2.7 Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSZ[1:0]: Sets the resizing factor. When the RSZ bits are set for resizing, the FT1505C writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions, which are contracted according to the factor respectively. See "Resizing function".

Table 13 Resizing factor (RSZ)

RSZ [1:0]	Resizing Scale	RSZ [1:0]	Resizing Scale
2'h0	No resizing (x1)	2'h2	Setting prohibited
2'h1	x 1/2	2'h3	x 1/4

RCH[1:0]: Sets the number of remainder pixels in horizontal direction when resizing a picture. By specifying the number of remainder pixels by RCH bits, the data can be transferred without taking the remainder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

Table 14 Remainder Pixels in Horizontal Direction (RCH) Note: 1 pixel = 1RGB

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

RCV[1:0]: Sets the number of remainder pixels in vertical direction when resizing a picture. By specifying the number of remainder pixels by RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

Table 15 Remainder Pixels in Vertical Direction (RCV) Note: 1 pixel = 1RGB

RCV[1:0]	Number of remainder Pixels in Vertical Direction
2'h0	0 pixels
2'h1	1 pixels
2'h2	2 pixels
2'h3	3 pixels

10.2.8 Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on the panel when writing D[1] = "1", and is turned off when writing D[1] = "0". When writing D[1] = "0", the graphics display data is retained in the internal GRAM and the FT1505C displays the data when writing D[1] = "1". When D[1] = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1-0] = 2'b01, the FT1505C continues internal display operation. When the display is turned off by setting D[1-0] = 2'b00, the FT1505C's internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF. For details, see "Instruction Setting".

Table 16

D[1:0]	BASEE	Source output (S1 ~S720)	FMARK signal	Internal operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-lit display level	Operation	Operation
2'h3	0	Non-lit display level	Operation	Operation
	1	Base image display	Operation	Operation

Notes: 1. The data write operation from the microcomputer to the internal RAM is performed irrespective of the setting of the D[1:0] bits.

2. The internal state of the FT1505C in standby mode become the same as when D[1:0] = 2'b00. This does not mean the D[1:0] setting is changed when setting the standby mode.
3. The D[1:0] setting is valid on both 1st and 2nd displays.
4. The non-lit display level from the source output pins is determined by instruction (PTS).

CL: When CL = "1", the FT1505C enters the 8-color mode. Follow the 8-color mode setting sequence when setting the 8-color mode. In 8-color mode, the grayscale amplifiers other than those for the V0 and V63 level are halted. If used in combination with frame-inversion liquid crystal drive, the power consumption will be further reduced.

Table 17 DTE, GON: Controls the output of liquid crystal panel output signal.

GON	DTE	G1 ~ G320
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

BASEE: Base image display enable bit. When BASEE = "0", no base image is displayed. The FT1505C drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed, and the partial display is inactive. The base image indicates the whole display screen. The D[1:0] setting has precedence over the BASEE setting.

PTDE0: Partial image 1 enable bit

PTDE1: Partial image 2 enable bit

PTDE0/1 = 0: turns off partial image. Only base image is displayed.

PTDE0/1 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

10.2.9 Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default		0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

FP [3:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [3:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Note on Setting BP and FP Set the BP and FP bits as follows in respective operation modes.

Table 18 BP and FP Settings

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Table 19 Front and Back Porch period (Line periods)

FP[3:0] or BP[3:0]	Front or Back Porch period (Line periods)	FP[3:0] or BP[3:0]	Front or Back Porch period (Line periods)
4'h0	2 lines	4'h8	8 lines
4'h1	2 lines	4'h9	9 lines
4'h2	2 lines	4'hA	10 lines
4'h3	3 lines	4'hB	11 lines
4'h4	4 lines	4'hC	12 lines
4'h5	5 lines	4'hD	13 lines
4'h6	6 lines	4'hE	14 lines
4'h7	7 lines	4'hF	14 lines

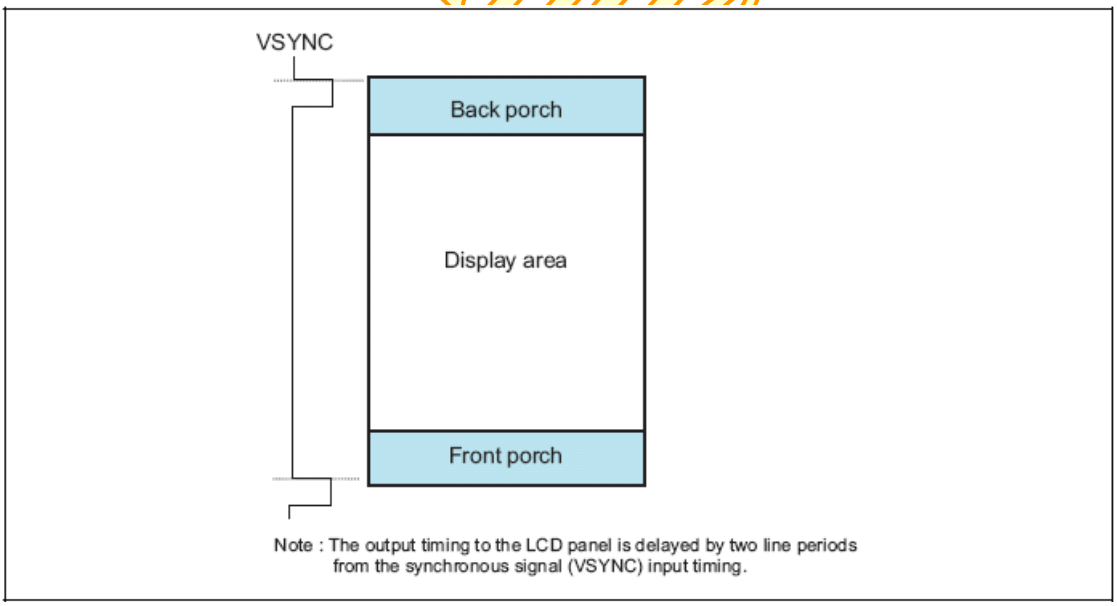


Figure 6: Front, Back Porch periods

10.2.10 Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC[3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 20

ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz	ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz
4'h0	0 frame	-	4'h8	17 frames	284ms
4'h1	3 frames	50ms	4'h9	19 frames	317ms
4'h2	5 frames	84ms	4'hA	21 frames	351ms
4'h3	7 frames	117ms	4'hB	23 frames	384ms
4'h4	9 frames	150ms	4'hC	25 frames	418ms
4'h5	11 frames	184ms	4'hD	27 frames	451ms
4'h6	13 frames	217ms	4'hE	29 frames	484ms
4'h7	15 frames	251ms	4'hF	31 frames	518ms

Table 21 PTG[1:0]: Sets the scan mode in non-display area.

PTG[1]	PTG[0]	Scan mode in non-display area	Source output level in non-display area	Vcom output
0	**0**	Normal scan	PTS[2:0] setting	alternating output
0	**1**	VGL (fixed)	PTS[2:0] setting	alternating output
1	**0**	Interval scan	PTS[2:0] setting	alternating output
1	**1**	Interval scan	PTS[2:0] setting	alternating output

PTS[2:0]: Sets the source output level in non-display area drive period (front/back porch period and blank area between partial displays). When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 22 Source output level and voltage generating operation in non-display drive period

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3'h0	V63	V0	V0 to V63	Register setting (DC0, DC1)
3'h1	V63	V0	V0 to V63	Register setting (DC0, DC1)
3'h2	GND	GND	V0 to V63	Register setting (DC0, DC1)
3'h3	Hi-Z	Hi-Z	V0 to V63	Register setting (DC0, DC1)
3'h4	V63	V0	V0 and V63	1/2 the frequency set by DC0, DC1
3'h5	V63	V0	V0 and V63	1/2 the frequency set by DC0, DC1
3'h6	GND	GND	V0 and V63	1/2 the frequency set by DC0, DC1
3'h7	Hi-Z	Hi-Z	V0 and V63	1/2 the frequency set by DC0, DC1

Notes: 1. The power efficiency improvement from halting grayscale amplifiers and slowing down the step-up clock frequency can be obtained in non-display drive period.

2. The gate output level in non-display area drive period is determined by PTG[1:0].

10.2.11 Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the FT1505C starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits. See "FMARK" for details.

Table 23

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

10.2.12 RGB interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the FT1505C performs display operation.

Table 24 RGB interface operation

RIM[1:0]	RGB Interface operation	Colors
2'h0	18-bit RGB interface (1 transfer/pixel) via DB17—DB0	262,144
2'h1	16-bit RGB interface (1 transfer/pixel) via DB17—DB13, DB11—DB1	65,536
2'h2	6-bit RGB interface (3 transfers/pixel) via DB17—DB12	262,144
2'h3	6-bit RGB interface (3 transfers/pixel) via DB17—DB12	262,144

Notes: 1: Instruction bits are set via system interface.

2: Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the

VSYNC interface operation mode is prohibited.

Table 25 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	VSYNC interface

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 26 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface
1	RGB interface

The FT1505C selects the optimum interface according to the displayed image by setting instruction as follows.

In moving picture display operation via RGB or VSYNC interface, write data in high-speed write mode (HWM = 1) in order to access RAM in high-speed with low power consumption.

Table 27

The state of display	Operation Mode	RAM Access (RM)	Display Operation Mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 2'h0)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 2'h1)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 2'h1)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 2'h2)

Notes:

1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM1-0) while RGB interface is in operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.
5. Use high-speed write function (HWM = 1) when writing data via RGB or VSYNC interface.

ENC[2:0]: Set the GRAM write cycle through the RGB interface

Table 28 GRAM write cycle selection

ENC[2:0]	GRAM write cycle (frame periods)
3'h0	1 Frame
3'h1	2 Frames
3'h2	3 Frames
3'h3	4 Frames
3'h4	5 Frames
3'h5	6 Frames
3'h6	7 Frames
3'h7	8 Frames

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the FT1505C to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the FT1505C according to the instruction settings for these periods.

10.2.13 Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h00, a high-active pulse FMARK is outputted at the start of back porch period for 1H period (IOVcc-GND amplitude signal). FMARK can be used as the trigger signal for frame synchronous write operation. See "FMARK" for details.

Make sure the setting restriction 9'h000 ≤ FMP ≤ BP+NL+FP.

Table 29

FMP[8:0]	FMARK output position
9'h000	0th line
9'h001	1st line
9'h002	2nd line
….	….
9'h14E	334th line
9'h14F	335th line
9'h150~1FF	Setting disabled

10.2.14 RGB display interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of the DOTCLK pin.
DPL = "0" The data is input on the rising edge of DOTCLK
DPL = "1" The data is input on the falling edge of DOTCLK
EPL: Sets the signal polarity of the ENABLE pin.
EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".
EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".
HSPL: Sets the signal polarity of the HSYNC pin.
HSPL = "0" Low active
HSPL = "1" High active
VSPL: Sets the signal polarity of the VSYNC pin.
VSPL = "0" Low active
VSPL = "1" High active

10.3 Power control

10.3.1 Power control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STB: When STB = 1, the FT1505C enters the standby mode. In standby mode, the FT1505C halts RC oscillation and receiving external clock signal to halt the display operation completely. In setting the standby mode, follow the standby mode setting sequence. The instruction register setting is retained in standby mode. The FT1505C accepts only the following instructions in standby mode:
1. Exit standby mode (STB = 0)
2. Start oscillation

SLP: When SLP = 1, the FT1505C enters the sleep mode. In sleep mode, the internal display operation except RC oscillation

is halted to reduce power consumption. No change to the GRAM data and instruction setting is accepted and the GRAM data and the instruction setting are maintained in sleep mode.

DSTB: When DSTB = 1, the FT1505C enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the FT1505C enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = 3'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Table 30 constant current in operational amplifiers

AP[2:0]	Gamma driver amplifiers
3'h0	Halt
3'h1	Disable
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	Disable

Note: The values in the table represent the ratios of currents in respective settings to the current.

APE: Liquid crystal power supply enable bit. Set APE = "1" when starting the generation of liquid crystal power supply according to the liquid crystal power supply startup sequence. After starting up the power supply circuit, set APE = "1".

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

Table 31 Step-up factor for step-up circuits

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Vci1 +Vci	-Vci	3xDDVDH	-(Vci+2 x DDVDH
3'h1	Vci1 +Vci	-Vci		-(2xDDVDH)
3'h2				-(Vci+DDVDH)
3'h3	Vci1+Vci	-Vci	Vci+2xDDVDH	-(Vci+2xDDVDH)
3'h4				-2xDDVDH
3'h5				-(Vci+DDVDH)
3'h6	Vci1 +Vci	-Vci	2xDDVDH	-2xDDVDH
3'h7				-(Vci+DDVDH)

Notes:

1. Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.
2. Set the following voltages within the respective ranges:

DDVDH = 6.0V (max.) VGH = 15.0V (max.)

VGL = -12.5V (max.) VCL = -3.0V (max.)

SAP: Source driver output control
SAP = 0, Source driver is disabled.
SAP = 1, Source driver is enabled.
When starting the charge-pump of LCD in the Power ON stage, make sure that SAP = 0, and set the SAP = 1, after starting up the LCD power supply circuit.

10.3.2 Power control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VC[2:0]: Sets the factor of Vci to generate the reference voltages VciOUT, Vci1.

Table 32 Reference voltage setting (Vci1)

VC[2:0]	VciOUT (reference voltage) Vci1 voltage
3'h0	0.90 x Vci
3'h1	0.80 x Vci
3'h2	0.70 x Vci
3'h3	0.60 x Vci
3'h4	0.50 x Vci
3'h5	0.40 x Vci
3'h6	Vci
3'h7	Vci

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current/power consumption. Adjust the frequency taking the trade-off between the display quality and the current/power consumption into account.

Table 33 operating frequencies of step-up circuits 1/2

DC0[2:0]	Step-up circuit 1 Operating frequency (fDCDC1)	DC1[2:0]	Step-up circuit 2 Operating frequency (fDCDC2)
3'h0	fosc	3'h0	fosc/4
3'h1	fosc/2	3'h1	fosc/8
3'h2	fosc/4	3'h2	fosc/16
3'h3	fosc/8	3'h3	fosc/32
3'h4	fosc/16	3'h4	fosc/64
3'h5	fosc/32	3'h5	fosc/128
3'h6	fosc/64	3'h6	fosc/256
3'h7	Halt set-up circuit 1	3'h7	Halt set-up circuit 2

Note: Make sure $f_{DCDC1} \geq f_{DCDC2}$, when setting the operating frequencies of DC0[2:0] and DC1[2:0]

10.3.3 Power control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VRH[3:0]: Sets the amplifying rate (1.6 ~ 1.9) of Vci to generate the output of VREG1OUT, which is a reference level of VCOM and grayscale voltage.

VRH[3:0]	VREG1OUT
4'h0	Halt(Hi-Z)
4'h1	Vci x1.4
4'h2	Vci x1.45
4'h3	Vci x1.5
4'h4	Vci x1.55
4'h5	Vci x1.6
4'h6	Vci x1.65
4'h7	Vci x1.7
4'h8	Vci x1.75
4'h9	Vci x1.8
4'h10	Vci x1.85
4'h11	Disable
4'h12	Disable
4'h13	Disable
4'h14	Disable
4'h15	Disable

PON: Controls ON/OFF of VGH/VGL. When setting the PON bit, follow the power supply startup sequence.

PON = "0": Stop the step-up operation to generate VGH/VGL.

PON = "1": Start the step-up operation to generate VGH/VGL.

VCMR: Selects either external resistor (VcomR) or internal electric volume (VCM) to set the electrical potential of VcomH.

Table 35

VCMR	VCOMH1 electrical potential
0	VCOMR (variable resistor)
1	Internal electronic volume

Power control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0]: Sets the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.24 x VREG1OUT.

Table 36 VDV: Vcom amplitude

VDV[4:0]	Vcom amplitude	VDV[4:0]	Vcom amplitude
5'h00	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h01	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h02	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h03	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h04	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h05	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h06	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h07	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h08	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h09	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22
5'h0B	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.24
5'h0C	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.26
5'h0D	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.28
5'h0E	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.30
5'h0F	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.32

Note: Set the Vcom amplitude from 2.5V to (DDVDH-0.5)V.

10.4 RAM access instruction

RAM Address set horizontal address (R20h),
RAM Address set vertical address (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Top: R20h, Bottom: R21h

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the AM, I/D[1:0] settings as the FT1505C writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note : In internal clock operation and VSYNC interface operation (RM = “0”), the address AD16-0 is set when executing the instruction.

Table 37 GRAM address range

AD[16:0]	GRAM Setting
17’h00000 ~ 17’h000EF	Bitmap data on the first line
17’h00100 ~ 17’h001EF	Bitmap data on the second line
17’h00200 ~ 17’h002EF	Bitmap data on the third line
17’h00300 ~ 17’h003EF	Bitmap data on the fourth line
:	:
17’h13C00 ~ 17’h13CEF	Bitmap data on the 317th line
17’h13D00 ~ 17’h13DEF	Bitmap data on the 318th line
17’h13E00 ~ 17’h13EEF	Bitmap data on the 319th line
17’h13F00 ~ 17’h13FEF	Bitmap data on the 320th line

10.5 Write/Read RAM data

10.5.1 Write Data to GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation															

WD[17:0]: The FT1505C expands data into 18 bits internally in write operation. The format to expand data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The FT1505C automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. In deep standby mode, GRAM access is disabled. In 8-/16-bit interface operation, the MSBs of R and B dot are written as the LSBs of respective dot to expand data into 18 bits. In this case, 65,536 colors are available.

Table 38 GRAM data and LCD output level (REV = "0")

GRAM data (RGB)	Selected grayscale		GRAM data (RGB)	Selected grayscale	
	Negative	Positive		Negative	Positive
000000	V0	V63	100000	V32	V31
000001	V1	V62	100001	V33	V30
000010	V2	V61	100010	V34	V29
000011	V3	V60	100011	V35	V28
000100	V4	V59	100100	V36	V27
000101	V5	V58	100101	V37	V26
000110	V6	V57	100110	V38	V25
000111	V7	V6	100111	V39	V24
001000	V8	V55	101000	V40	V23
001001	V9	V54	101001	V41	V22
001010	V10	V53	101010	V42	V21
001011	V11	V52	101011	V43	V20
001100	V12	V51	101100	V44	V19
001101	V13	V50	101101	V45	V18
001110	V14	V49	101110	V46	V17
001111	V15	V48	101111	V47	V16
010000	V16	V47	110000	V48	V15
010001	V17	V46	110001	V49	V14
010010	V18	V45	110010	V50	V13
010011	V19	V44	110011	V51	V12
010100	V20	V43	110100	V52	V11
010101	V21	V42	110101	V53	V10
010110	V22	V41	110110	V54	V9
010111	V23	V40	110111	V55	V8

011000	V24	V39	111000	V56	V7
011001	V25	V38	111001	V57	V6
011010	V26	V37	111010	V58	V5
011011	V27	V36	111011	V59	V4
011100	V28	V35	111100	V60	V3
011101	V29	V34	111101	V61	V2
011110	V30	V33	111110	V62	V1
011111	V31	V32	111111	V63	V0

RAM Access via System interface

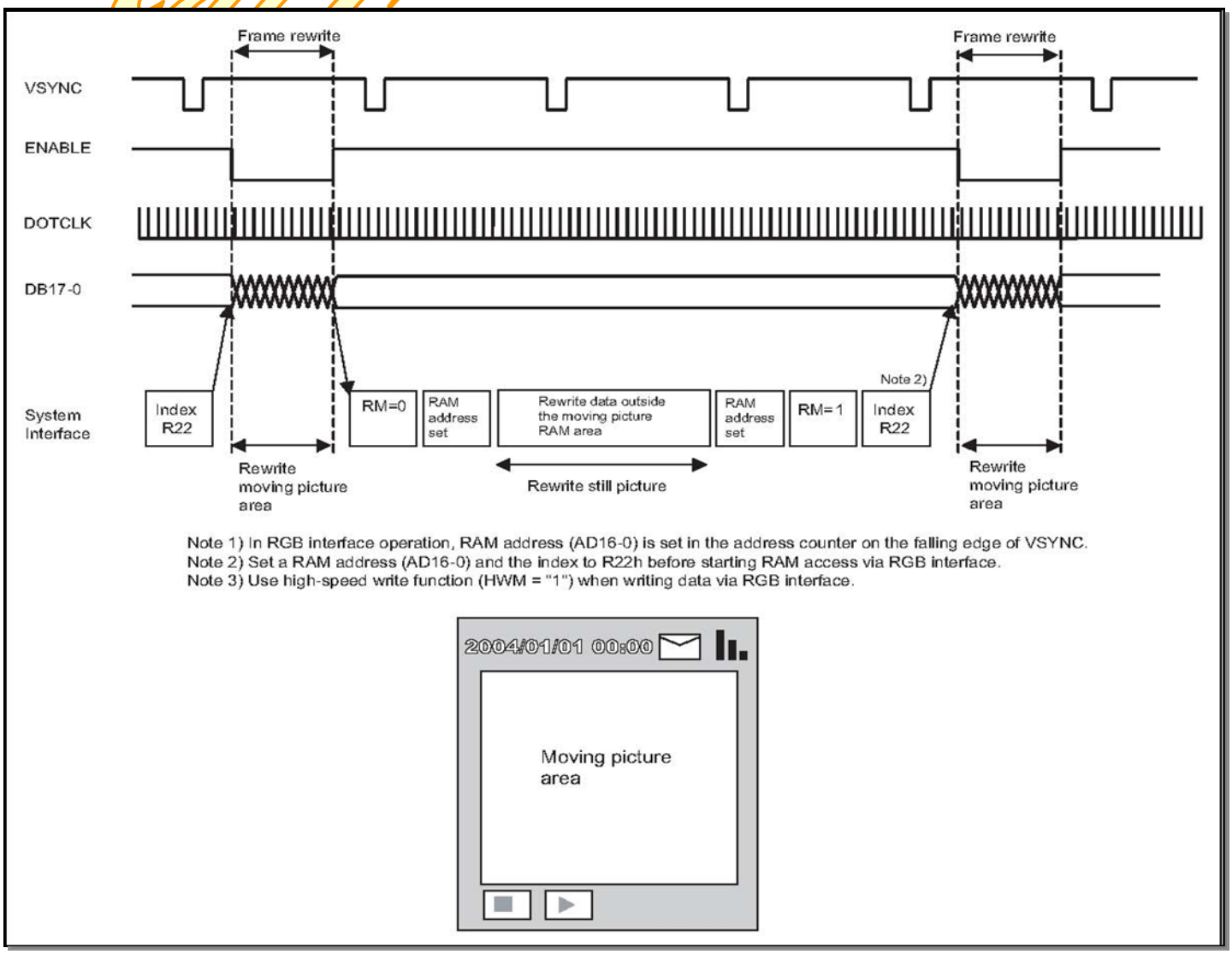


Figure 7

10.5.2 Read Data from GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.															

RD[17:0]: 18-bit data read from the GRAM. RAM read data RD[17:0] is transferred via different data bus in different interface operation.

When the FT1505C reads data from the GRAM to the microcomputer, the first word, which is read immediately after the RAM address set instruction is executed, is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the FT1505C reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

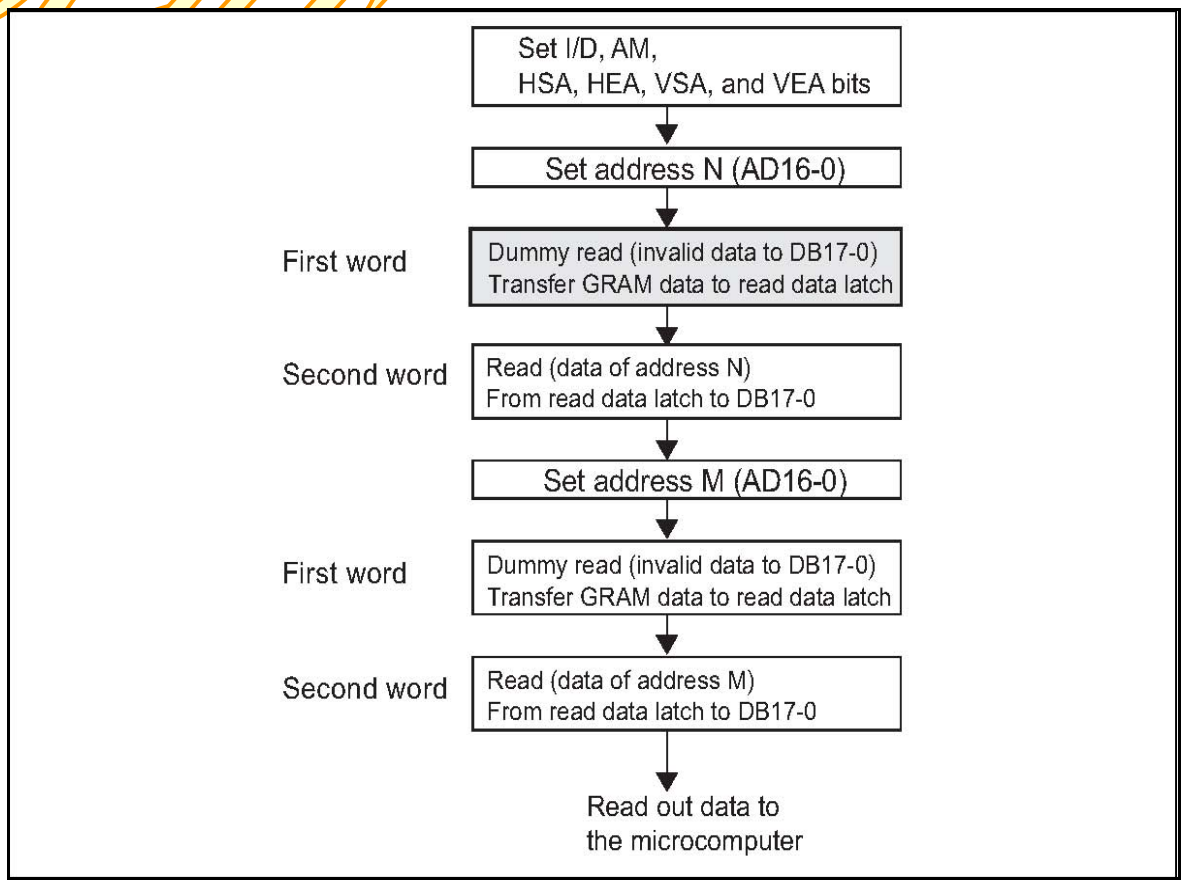


Figure 8: GRAM read sequence

Power control 7 (R29h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM[5:0]: Selects the internal electronic volume applied to VREG1OUT to set the VcomH electrical potential.

Table 39 VCM: internal electronic volume adjustment

VCM[5:0]	VcomH	VCM[5:0]	VcomH
6'h00	VREG1OUT x 0.685	6'h20	VREG1OUT x 0.845
6'h01	VREG1OUT x 0.690	6'h21	VREG1OUT x 0.850
6'h02	VREG1OUT x 0.695	6'h22	VREG1OUT x 0.855
6'h03	VREG1OUT x 0.700	6'h23	VREG1OUT x 0.860
6'h04	VREG1OUT x 0.705	6'h24	VREG1OUT x 0.865
6'h05	VREG1OUT x 0.710	6'h25	VREG1OUT x 0.870
6'h06	VREG1OUT x 0.715	6'h26	VREG1OUT x 0.875
6'h07	VREG1OUT x 0.720	6'h27	VREG1OUT x 0.880
6'h08	VREG1OUT x 0.725	6'h28	VREG1OUT x 0.885
6'h09	VREG1OUT x 0.730	6'h29	VREG1OUT x 0.890
6'h0A	VREG1OUT x 0.735	6'h2A	VREG1OUT x 0.895
6'h0B	VREG1OUT x 0.740	6'h2B	VREG1OUT x 0.900
6'h0C	VREG1OUT x 0.745	6'h2C	VREG1OUT x 0.905
6'h0D	VREG1OUT x 0.750	6'h2D	VREG1OUT x 0.910
6'h0E	VREG1OUT x 0.755	6'h2E	VREG1OUT x 0.915
6'h0F	VREG1OUT x 0.760	6'h2F	VREG1OUT x 0.920
6'h10	VREG1OUT x 0.765	6'h30	VREG1OUT x 0.925
6'h11	VREG1OUT x 0.770	6'h31	VREG1OUT x 0.930
6'h12	VREG1OUT x 0.775	6'h32	VREG1OUT x 0.935
6'h13	VREG1OUT x 0.780	6'h33	VREG1OUT x 0.940
6'h14	VREG1OUT x 0.785	6'h34	VREG1OUT x 0.945
6'h15	VREG1OUT x 0.790	6'h35	VREG1OUT x 0.950
6'h16	VREG1OUT x 0.795	6'h36	VREG1OUT x 0.955
6'h17	VREG1OUT x 0.800	6'h37	VREG1OUT x 0.960
6'h18	VREG1OUT x 0.805	6'h38	VREG1OUT x 0.965
6'h19	VREG1OUT x 0.810	6'h39	VREG1OUT x 0.970
6'h1A	VREG1OUT x 0.815	6'h3A	VREG1OUT x 0.975
6'h1B	VREG1OUT x 0.820	6'h3B	VREG1OUT x 0.980
6'h1C	VREG1OUT x 0.825	6'h3C	VREG1OUT x 0.985
6'h1D	VREG1OUT x 0.830	6'h3D	VREG1OUT x 0.990
6'h1E	VREG1OUT x 0.835	6'h3E	VREG1OUT x 0.995
6'h1F	VREG1OUT x 0.840	6'h3F	VREG1OUT

Notes: Set VcomH from 2.5V to (DDVDH-0.5)V.

Frame Rate and Color Control (R2Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	16M_EN	Dither	0	0	0	0	0	0	0	0	0	0	0	RC2	RC1	RC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RC[2:0]: Set the internal oscillator frequency.

Table 40 RC: OSC frequency

RC2	RC1	RC0	(fosc) OSC frequency (kHz)
0	0	0	452
0	0	1	536
0	1	0	652
0	1	1	821
1	0	0	400
1	0	1	336
1	1	0	284
1	1	1	External RC

16M_EN: Select the color depth. 16M_EN=0 (262K color, default), 16M_EN=1 (16.7M color dither)

Dither: Dithering function control. When the dithering function is enabled, the 24-bit input data will be dithered into 18-bit and the display quality is closed to 16.7M color. Dither=0 (Disable, default), Dither=1 (Enable). The dithering input data transfer format is as below (16M_EN=1, Dither=1).

- 18-bit interface: 2 transfer mode
  - 1st transfer: DB17 ~ DB10, DB8 ~ DB1
  - 2nd transfer: DB17 ~ DB10
- 16-bit interface: 2 transfer mode (TRIREG=1, DFM=0)
  - 1st transfer: DB17 ~ DB10, DB8 ~ DB1
  - 2nd transfer: DB17 ~ DB10
- 8-bit interface: 3 transfer mode (TRIREG=1, DFM=1)
  - 1st transfer: DB17 ~ DB10
  - 2nd transfer: DB17 ~ DB10
  - 3rd transfer: DB17 ~ DB10

10.6 γ Control Instruction

10.7 γ Control (1) ~ (10) (R30h ~ R3Dh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP1 [2]	PKP1 [1]	PKP1 [0]	0	0	0	0	0	PKP0 [2]	PKP0 [1]	PKP0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31	W	1	0	0	0	0	0	PKP3 [2]	PKP3 [1]	PKP3 [0]	0	0	0	0	0	PKP2 [2]	PKP2 [1]	PKP2 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R32	W	1	0	0	0	0	0	PKP5 [2]	PKP5 [1]	PKP5 [0]	0	0	0	0	0	PKP4 [2]	PKP4 [1]	PKP4 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R35	W	1	0	0	0	0	0	PRP1 [2]	PRP1 [1]	PRP1 [0]	0	0	0	0	0	PRP0 [2]	PRP0 [1]	PRP0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R36	W	1	0	0	0	VRP1 [4]	VRP1 [3]	VRP1 [2]	VRP1 [1]	VRP1 [0]	0	0	0	VRP0 [4]	VRP0 [3]	VRP0 [2]	VRP0 [1]	VRP0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R37	W	1	0	0	0	0	0	PKN1 [2]	PKN1 [1]	PKN1 [0]	0	0	0	0	0	PKN0 [2]	PKN0 [1]	PKN0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38	W	1	0	0	0	0	0	PKN3 [2]	PKN3 [1]	PKN3 [0]	0	0	0	0	0	PKN2 [2]	PKN2 [1]	PKN2 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R39	W	1	0	0	0	0	0	PKN5 [2]	PKN5 [1]	PKN5 [0]	0	0	0	0	0	PKN4 [2]	PKN4 [1]	PKN4 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3C	W	1	0	0	0	0	0	PRN1 [2]	PRN1 [1]	PRN1 [0]	0	0	0	0	0	PRN0 [2]	PRN0 [1]	PRN0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3D	W	1	0	0	0	VRN1 [4]	VRN1 [3]	VRN1 [2]	VRN1 [1]	VRN1 [0]	0	0	0	VRN0 [4]	VRN0 [3]	VRN0 [2]	VRN0 [1]	VRN0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KP5-0[2:0] γ fine adjustment register for positive polarity
RP1-0[2:0] gradient adjustment register for positive polarity
KN5-0[2:0] γ fine adjustment register for negative polarity
RN1-0[2:0] gradient adjustment register for negative polarity
VRP0[4:0] amplitude adjustment register for positive polarity
VRP1[4:0] amplitude adjustment register for positive polarity
VRN0[4:0] amplitude adjustment register for negative polarity
VRN1[4:0] amplitude adjustment register for negative polarity
See “γCorrection function” for details.

10.8 Window address control instruction

Window horizontal RAM start address (R50h), Window horizontal RAM end address (R51h) Window vertical RAM start address (R52h), Window vertical RAM end address (R53h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R50	W/R	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	W/R	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	Default		0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1
R52	W/R	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53	W/R	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	Default		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

HSA[7:0]/HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that "00"h ≤ HSA[7:0] < HEA[7:0] ≤ "EF"h and "04"h ≤ HEA - HSA

VSA[8:0]/VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that "000"h ≤ VSA[8:0] < VEA[8:0] ≤ "13F"h.

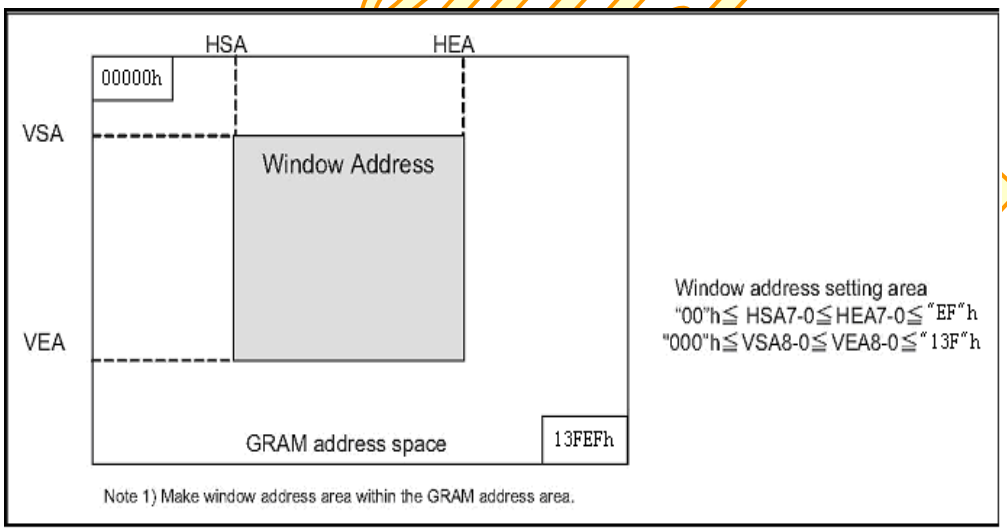


Figure 9: GRAM address map and window address area

10.9 Base image display control instruction

Driver output control (R60h), Base image display control (R61h), Vertical scroll control (R6Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R60	W/R	1	GS	0	NL 5	NL 4	NL 3	NL 2	NL 1	NL0	0	0	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R61	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6A	W/R	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the FT1505C to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 42 GRAM Data-grayscale level inversion

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

GS: Sets the direction of scan by the gate driver in the range determined by SCN[5:0] and NL[5:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.
When GS = 1, the scan direction is from G320 to G1

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 43

NL[5:0]	LCD drive line	NL[5:0]	LCD drive line	NL[5:0]	LCD drive line	NL[5:0]	LCD drive line
6'h00	0 line	6'h0D	112 lines	6'h1A	216 lines	6'h27	320 lines
6'h01	16 lines	6'h0E	120 lines	6'h1B	224 lines	6'h28—6'h3F	320 lines
6'h02	24 lines	6'h0F	128 lines	6'h1C	232 lines		
6'h03	32 lines	6'h10	136 lines	6'h1D	240 lines		
6'h04	40 lines	6'h11	144 lines	6'h1E	248 lines		
6'h05	48 lines	6'h12	152 lines	6'h1F	256 lines		
6'h06	56 lines	6'h13	160 lines	6'h20	264 lines		
6'h07	64 lines	6'h14	168 lines	6'h21	272 lines		
6'h08	72 lines	6'h15	176 lines	6'h22	280 lines		
6'h09	80 lines	6'h16	184 lines	6'h23	288 lines		
6'h0A	88 lines	6'h17	192 lines	6'h24	296 lines		
6'h0B	96 lines	6'h18	200 lines	6'h25	304 lines		
6'h0C	104 lines	6'h19	208 lines	6'h26	312 lines		

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

Table 44

SCN [5:0]	Scan start position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28-6'h3F	Disabled	Disabled	Disabled	Disabled

VLE: When VLE1 = 1, a vertical scroll is performed in the base image from the line (of the physical display) determined

by VL[8:0] bit. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE=0.

VLE	base image
0	Fixed display
1	Scrolling

NDL: Set the source driver output level in the non-display area.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE=0.

NDL	Non-display area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0] in this case. Make sure that VL[8:0] ≤ **160**.

10.10 Partial control instruction

Partial image 1 display position (R80h)

Partial image 1 RAM start address (R81h), Partial image 1 RAM end address (R82h)

Partial image 2 display position (R83h)

Partial image 2 RAM start address (R84h), Partial image 2 RAM end address (R85h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R80	W	1	0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R81	W		0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82	W		0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R83	W	1	0	0	0	0	0	0	0	PTD P1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R84	W	1	0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R85	W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display position of partial image 1.
PTDP1[8:0]: Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting, make sure

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display area: (PTDP0, PTDP0+(PTEA0 – PTSA0))
Coordinates of partial image 2 display area: (PTDP1, PTDP1+(PTEA1 – PTSA1))

If PTDP0 is set to "9'h000", the partial image 1 is displayed from the 1st line of the panel on the base image.

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0]. **Make sure PTSA0[8:0] ≤PTDP0[8:0]**.

PTSA1[8:0] PTEA1[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure PTSA1[8:0] ≤ PTEA1[8:0]. **Make sure PTSA1[8:0] ≤PTDP1[8:0]**.

10.11 Panel interface control instruction

10.11.1 Panel interface control 1 (R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the FT1505C's display operation is synchronized with internal clock signal.

Table 45 Clocks per Line

RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line
5'h00—5'h0F	Disabled	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clock	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

Note: internal clock operation: the frequency of which is determined by instruction (DIVI), from the reference point.

DIVI[1:0]: Sets the division ratio of internal clock frequency. The FT1505C's internal operation is synchronized with the frequency-divided internal clock, the frequency of which is divided by the division ratio set by DIVI[1:0]. When changing the DIVI[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed.

Table 46 Division ratio of the internal operation clock

DIVI[1:0]	Division Ratio	Internal Operation Clock Frequency
2'h0	1/1	fosc / 1
2'h1	1/2	fosc / 2
2'h2	1/4	fosc / 4
2'h3	1/8	fosc / 8

Note: fosc: RC oscillation frequency

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, the frame frequency must be adjusted. See "Frame-Frequency Adjustment Function" for details.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clocks per line x division ratio x (line + BP + FP)}} \quad [\text{Hz}]$$

fosc : RC oscillation frequency
Line: Number of lines to drive the LCD (NL bits)
Division ratio: DIVI
Clocks per line: RTNI

10.11.2 Internal Source output Control (R91h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W								Eqi1	Eqi0						Sdti2	Sdti1	Sdti0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EQI: Define internal source equalize cycles, EQI=0 that is no equalize cycle, otherwise EQI cycles.

SDTI: define internal source output delay based on the gate falling edge, SDTI=0:one cycle, otherwise SDTI+1 cycles.

10.11.3 Panel interface control 2 (R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOI2	NOI1	NOI0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOI[2:0]: Sets the non-overlap period of gate output when the FT1505C's display operation is synchronized with internal clock signal.

Table 47

NOI[2:0]	Gate non-overlap period	NOI[2:0]	Gate non-overlap period
3'h0	0 clocks	3'h4	4 clocks
3'h1	1 clocks	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

10.11.4 Internal Source output Control (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W								LS11	LS10		VCOM_SK2	VCOM_SK1	VCOM_SK0			LS01	LS00
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LS0: Define the source OP work cycle. LS0=0 is one “dfosc” cycle, otherwise LS0+1 cycles.

LS1: Define source overshoot work cycle. LS1=0 is one “dfosc” cycle, otherwise LS1+1 cycles.

VCOM_SK: define VCOM overshoot work cycle. VCOM_SK is a half dfosc cycle, otherwise VCOM_SK/2 cycles.

10.12 EPROM control

EPROM access control 1 (RA0h), EPROM access control 2 (RA1h), Calibration control (RA4h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RA0	W	1	0	0	0	0	0	0	0	0	TE	0	EOP [1]	EOP [0]	0	0	EAD [1]	EAD [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA1	W		0	0	0	0	0	0	0	0	ED [7]	ED [6]	ED [5]	ED [4]	ED [3]	ED [2]	ED [1]	ED [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TE: Enable internal EPROM control bit (EOP). Follow the PROM control sequence when setting TE. When resetting register (loading EOP = 2’h2) and executing calibration, TE is set automatically according to the internal automatic sequence and it does not have to be set.

EOP[1:0]: Internal EPROM control bit. Follow the PROM control sequence when setting EOP[1:0].

Table 51

EOP[1:0]	EPROM control
2’h0	Halt
2’h1	Write
2’h2	Reset register (load)

EAD[1:0]: Internal EPROM address. Set EAD[1:0] = 00 ~ 10 when writing to the internal EPROM. The EAD[1:0] setting determines the register (R28h, R29h, R2Ah) to write the data ED[7:0] (see Table 59).

ED[7:0]: Internal EPROM write data.

Table 52

EAD[1:0]	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
2'h0	0	0	0	0	0	0	0	0
2'h1	EVCME0*	0	0	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
2'h2	EVCME1*	0	0	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

Note*: Make sure to write "1" to EVCME0, EVCME1.

CALB: When CALB = 1, the FT1505C executes calibration to the internal operation. Set CALB = 1 after power-on reset. The CALB setting is automatically returned to "0".

10.13 Instruction list

Main category		Sub category		Upper code								Lower code							
Upper index		index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
IR	index			*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status read			L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
0*	Display control(1)	00h	Start oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
			Device code read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		00h	Start oscillation	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
		01h	Driver output control (1)	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
		02h	LCD driving control	0	0	0	0	0	0	B/C	EOR	0	0	0	0	0	0	0	0
		03h	Entry mode	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	0	0
		04h	Resize control	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
		05h-06h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		07h	Display control (1)	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
		08h	Display control (2)	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
		09h	Display control (3)	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
		0Ah	Display control (4)	0	0	0	0	0	0	0	0	0	0	0	0	EMARKOE	FMI2	FMI1	FMI0
		0Bh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Ch	RGB display interface control (1)	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
		0Dh	Frame Mark Position	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
		0Eh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1*	Power control	10h	Power control (1)	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	STB
		11h	Power control (2)	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
		12h	Power control (3)	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
		13h	Power control (4)	0	0	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
		14h-1Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2*	RAM access	20h	RAM address set (horizontal direction)	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		21h	RAM address set (vertical direction)	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		22h	RAM data write/read	RAM write data(WD17-0)/Read data(RD17-0) bits are transferred via different data bus in different interface operation															
		23h-28h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		29h	Power control (7)	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
		2Ah	EPROM read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		2Bh	Frame rate and color control	16M_E	Dither	0	0	0	0	0	0	0	0	0	0	0	RC2	RC1	RC0
		2Ch-2Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3*	Gamma control	30h	Gamma control (1)	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
		31h	Gamma control (2)	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
		32h	Gamma control (3)	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
		33h-34h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		35h	Gamma control (4)	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
		36h	Gamma control (5)	0	0	0	VRP14	VRP13	VRP 12	VRP11	VRP10	0	0	0	VRP04	VRP03	VRP02	VRP01	VRP00
		37h	Gamma control (6)	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
		38h	Gamma control (7)	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
		39h	Gamma control (8)	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
		3Ah-3Bh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		3Ch	Gamma control (9)	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
		3Dh	Gamma control (10)	0	0	0	VRN14	VRN13	VRN 12	VRN11	VRN10	0	0	0	VRN04	VRN03	VRN02	VRN01	VRN00
		3Eh-3Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Instruction list (continued)

Main category		Sub category		Upper code								Lower code							
Upper index		index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4*		40h-4Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5*	Window address control	50h	Horizontal RAM address start position	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
		51h	Horizontal RAM address end position	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
		52h	Vertical RAM address start position	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

		53h	Vertical RAM address end position	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
		54h-5Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6*	Display control(2) & Base image display control	60h	Driver output control (2)	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
		61h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
		62h-69h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		6Ah	Vertical scroll control	0	0	0	0	0	0	0	VL8	VI7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
		6Bh-6Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7*		70h-7Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8*	Partial image control	80h	Partial image 1 display position	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
		81h	Partial image 1 RAM area start line	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
		82h	Partial image 1 RAM end line	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
		83h	Partial image 2 display position	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
		84h	partial image 2 RAM area start line	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
		85h	Partial image 2 RAM end line	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
		86h-8Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9*	Panel interface control	90h	Panel interface control (1)	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
		91h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		92h	Panel interface control (2)	0	0	0	0	0	NOWI	NOWI1	NOWI0	0	0	0	0	0	0	0	0
		93h-94h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

		95h	Panel interface control (4)	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
		96h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		97h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		98-9Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A*	EPROM control	A0h	EPROM control (1)	0	0	0	0	0	0	0	0	TE	0	EOP1	EOP0	0	0	EAD1	EAD0
		A1h	EPROM control (2)	0	0	0	0	0	0	0	0	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
		A2h	VCN_En	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Vcn_En
		A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
		AE	EPROM read	EVCM4	EVCM3	EVCM2	EVCM1	EVCM0	EVCM4	EVCM13	EVCM12	EVCM11	EVCM10	EVCMEE(	EVCME1	UID3	UID2	UID1	UID0
		A3h,A5-AFh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		2Ah	EPROM read									EVCME1		EVCM11[ ]	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

11 OTP Programming Flow

The FT1505C incorporates 8-bits x 3 addresses EPROM. User identification code is written in the EPROM address 0'h. VcomH setting instruction is written in the EPROM addresses 1'h, 2'h. By preparing two addresses to write VcomH setting, it allows changing the VcomH setting. When writing the VcomH setting for the first time, write the setting in the address 1'h. Write the setting in the address 2'h when writing the setting for the second time. Make sure to write "1" to EVCME0 and EVCME1 bits. When the second VcomH setting is written in the address 2'h, the second setting is enabled.

The VCM_En bit in the RA2h register determines whether the setting in EPROM or the VCM[5:0] setting (externally input instruction) is enabled to set the VcomH level. Set VCM_En = 1, when enabling the EPROM setting. Set VCM_En = 0, when not using the EPROM setting.

When writing the setting to EPROM, make sure to follow the EPROM write sequence.

By performing EPROM read operation, the setting written in EPROM is read out. In this case, follow the EPROM read sequence. In case of setting CALB = 1 (RA4h: calibration to internal operation) after power-on reset, the data written in EPROM is stored in EPROM read register.

EPROM data write control register

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RA0H	0	0	0	0	0	0	0	0	TE	0	EOP[1]	EOP[0]	0	0	EAD[1]	EAD[0]
RA1H	0	0	0	0	0	0	0	0	ED[7]	ED[6]	ED[5]	ED [4]	ED[3]	ED[2]	ED[1]	ED[0]
RA2H																VCM_En

EOP[1:0]	EPROM control bit
2'h0	Halt
2'h1	Write
2'h2	Reset register (load)

EAD[1:0]	EPROM write address
00	User ID code
01	VcomH level setting 1
10	VcomH level setting 1

TE	EPROM write control
0	Data write end
1	Data write start

ED[7:0]	EPROM write data

EAD[1:0]	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
2'h0	0	0	0	0	UID[3]	UID[2]	UID[1]	UID[0]
2'h1	EVCME0	0	EVCM0[5]	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
2'h2	EVCME1	0	EVCM1[5]	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

EPROM data read register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R28H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	UID[3]	UID[2]	UID[1]	UID[0]
RAEH	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]	EVCM14	EVCM13	EVCM12	EVCM11	EVCM10	EVCME0	EVCME1	UID[3]	UID[2]	UID[1]	UID[0]		
R2A	0	0	0	0	0	0	0	0	EVCME1	0	EVCM1[5]	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]		

EVCME1/0	
01	Enable EVCM0[4:0] setting(R29h)
11/10	Enable EVCM1[4:0] setting(R2Ah)

VCM_En	
0	Enable VCM[5:0] setting(R13h)
1	Enable EVCM0[4:0] or EVCM1[4:0] setting

EPROM write sequence

(1)EAD=01;

Item	Instructions	Value	Note
1	Power supply, VCI=IOVCC=2.80V DDVDH: No external voltage		
2	Reset		
3	Initial code setup		
4	EPROM CONTROL (RA0)	0x00A0 0x0011	Set EPROM Write function & EPROM write address
5	DDVDH: external 7.5V		
6	Wait 10ms or more		
7	EPROM CONTROL (RA0)	0x00A0 0x0011	Set EPROM Write function & EPROM write address
8	EPROM DATA (RA1)	0x00A1 0x00A0	Set EPROM Write DATA & Set EVCME0=1, SET DATA=20h(for example data=20h).
9	Wait 1ms or more		
10	EPROM CONTROL (RA0)	0x00A0 0x0091	Set EPROM Start Write function
11	Wait 10ms or more		
12	DDVDH: no external voltage		
13	Wait 100ms or more		
14	EPROM CONTROL (RA0)	0x00A0 0x0021	Loading EPROM data
15	EPROM CONTROL (RA0)	0x00A0 0x0001	Loading EPROM data end
16	Wait 1ms or more		
17	Load data (RA2)	0x00A2 0x0001	Loading the EPROM data to replace the R29h register data. VCM_EN=1
18	Wait 1ms or more		
19	Read the data	0x00AE	See the datasheet "EPROM data write control register" section.

(2)EAD=02;

Item	Intructions	Value	Note
1	Power supply, VCI=IOVCC=2.80V DDVDH: No external voltage		
2	Reset		
3	Initial code setup		
4	EPROM CONTROL (RA0)	0x00A0 0x0012	Set EPROM Write function & EPROM write address
5	DDVD: external 7.5V voltage		
6	Wait 10ms or more		
7	EPROM CONTROL (RA0)	0x00A0 0x0012	Set EPROM Write function & EPROM write address
8	EPROM DATA (RA1)	0x00A1 0x00AB	Set EPROM Write DATA & Set EVCME1=1, SET DATA=2Bh(for example data=2bh)
9	Wait 1ms or more		
10	EPROM CONTROL (RA0)	0x00A0 0x0092	Set EPROM Start Write function
11	Wait 10ms or more		
12	DDVDH: No external voltage		
13	Wait 100ms or more		
14	EPROM CONTROL (RA0)	0x00A0 0x0022	Loading EPROM data
15	EPROM CONTROL (RA0)	0x00A0 0x0002	Loading EPROM data end
16	Wait 1ms or more		
17	Load data (RA2)	0x00A2 0x0001	Loading the EPROM data to replace the R29h register data. VCM_EN=1
18	Wait 1ms or more		
19	Read the data	0x002A	See the datasheet "EPROM data write control register" section.

(3)EAD=00;Write/Read USER ID

Item	Instructions	value	Note
1	Power supply, VCI=IOVCC=2.80V DDVDH: No external voltage		
2	Reset		
3	Initial code setup		
4	EPROM CONTROL (RA0)	0x00A0 0x0010	Set EPROM Write function & EPROM write address
5	DDVDH: external7.5V voltage		
6	Wait 10ms or more		
7	EPROM CONTROL (RA0)	0x00A0 0x0010	Set EPROM Write function & EPROM write address
8	EPROM DATA (RA1)	0x00A1 0x0083	Set EPROM Write DATA & Set EVCME0=1, SET UID=0011h(for example)
9	Wait 1ms or more		
10	EPROM CONTROL (RA0)	0x00A0 0x0090	Set EPROM Start Write function
11	Wait 10ms or more		
12	DDVDH: No external voltage		
13	Wait 100ms or more		
14	EPROM CONTROL (RA0)	0x00A0 0x0020	Loading EPROM data
15	EPROM CONTROL (RA0)	0x00A0 0x0000	Loading EPROM data end
16	Wait 1ms or more		
17	Load data (RA2)	0x00A2 0x0001	Loading the EPROM data to replace the R29h register data. VCM_EN=1
18	Wait 1ms or more		
19	Read USER ID	0x0028	Read out the USER ID.The LSB is the USER ID.

Figure 77: EPROM write sequence

12 Window Address Function

The FT1505C has memory to store display data of 240RGB x 320 lines. The FT1505C incorporates a circuit to control partial display, which allows switching driving methods between full-screen display mode and partial display mode.

The FT1505C makes display design setting and panel driving position control setting separately and specifies RAM area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image by setting PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

   Normal display BASEE = 1
   Partial display BASEE = 0, PTDE0/1 = 1
5. Change BASEE, PTDE0/1 setting to switch display modes (full-screen and partial display modes).

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing RAM data.

Table 60

	Display ENABLE	Numbers of lines	RAM area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h0DB)

Notes 1: The base image is displayed from the first line of the panel.

2: Make sure NL ≤ 320 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h0DB, respectively.

Table 61

	Display ENABLE	Display position	RAM area
Partial image 1	PTDE0	PTDP0	(PTSA0, PTEA0)
Partial image 2	PTDE1	PTDP1	(PTSA1, PTEA1)

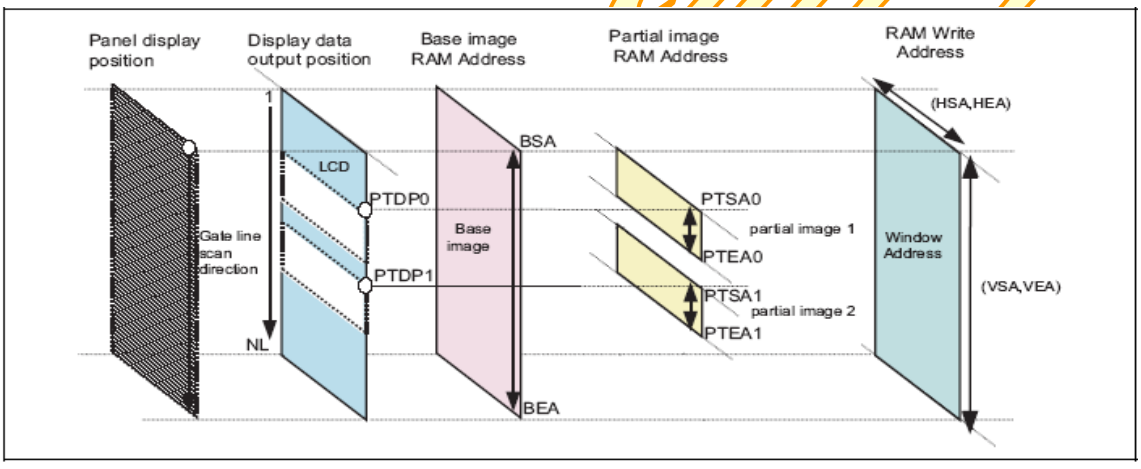


Figure 41: RAM Address, display position and drive position

12.1 Restrictions in setting display control instruction

Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partial images can be controlled independently.

$0 \le PTDP0 \le PTDP0 + (PTEA0 - PTSA0) < PTDP1 \le PTDP1 + (PTEA1 - PTSA1) \le NL$

The following figure shows the relationship among the RAM address, display position, and the lines driven for the display.

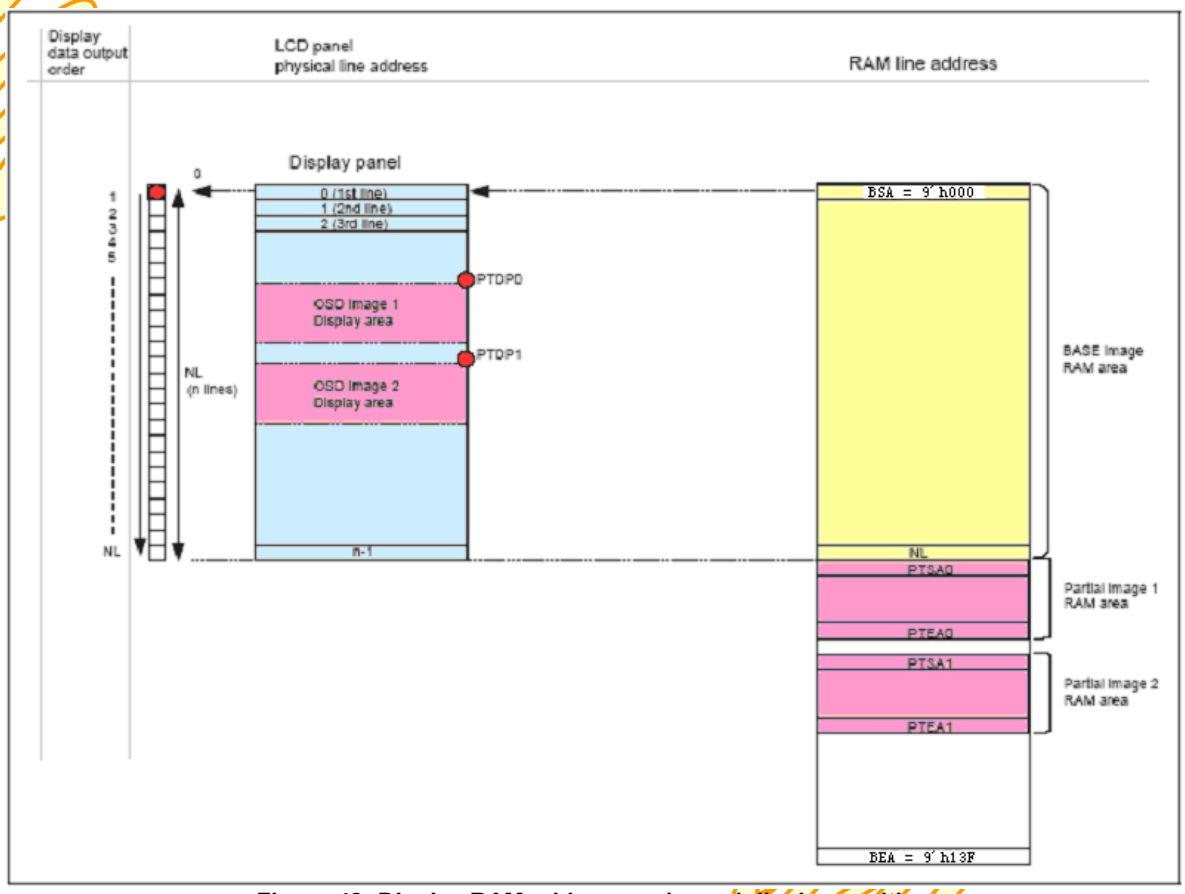


Figure 42: Display RAM address and panel display position

Note: This figure shows the relationship between RAM line address and the display position on the panel. In the FT1505C's internal operation, the data is written in the RAM area specified by the window address setting (HEA/HSA[8:0], VEA/VES[8:0]).

12.2 Instruction setting example

The followings are examples of display design setting for 240(RGB) x 320(lines) panels.

1. Full screen display (no partial)

The following is an example of full screen display setting.

Table 62

Base image display instruction	
BASEE	1
NL[5:0]	6'h27

PTDE0	0
PTDE1	0

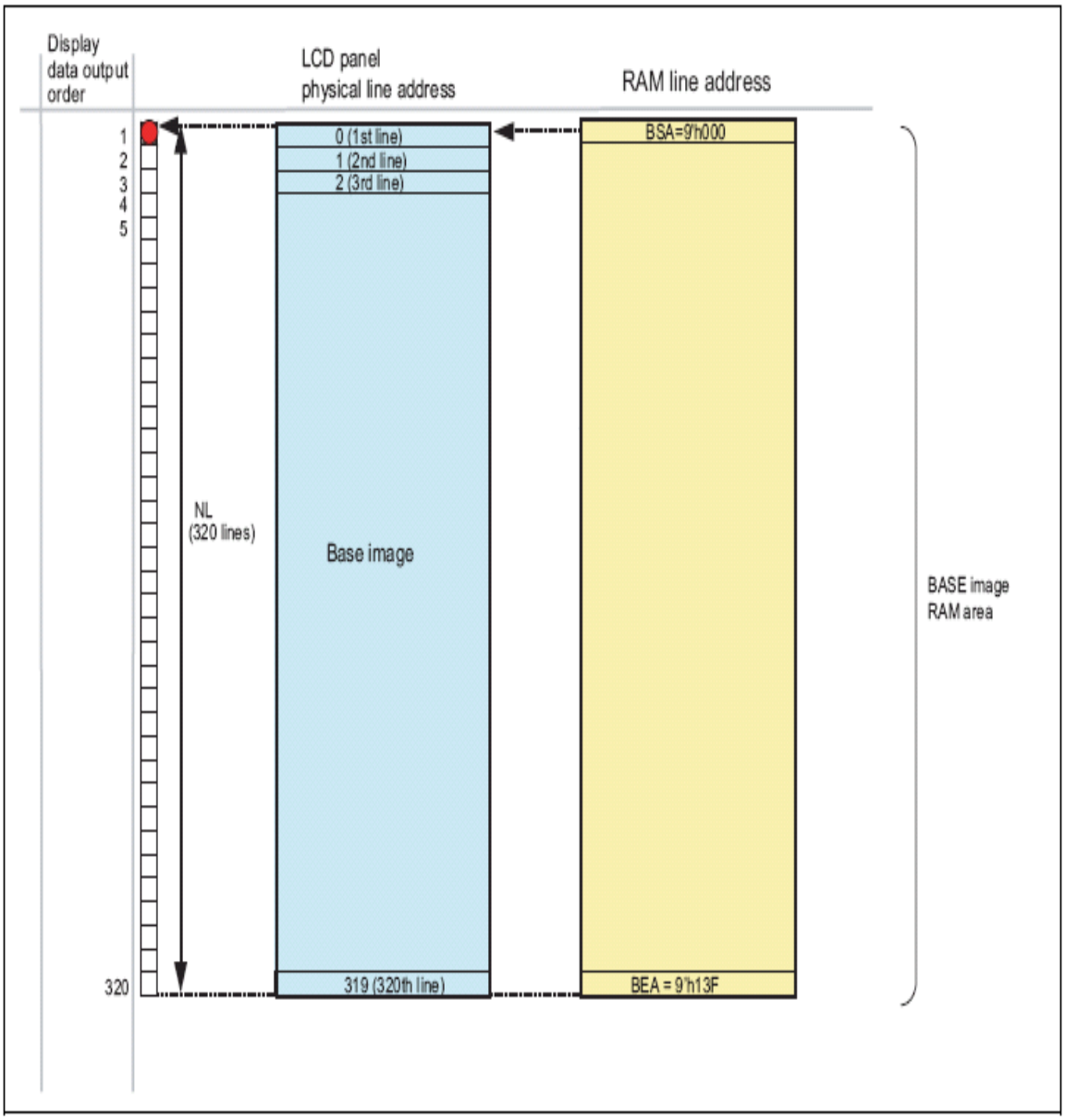


Figure 43: Full screen display (no partial)

2. Partial only

The following is an example of setting for partial image 1 only and turning off the base image. The partial image 1 is displayed at the position specified by PTDP0 bit.

Table 63

Base image display instruction	
BASEE	0
NL[5:0]	6'h27

Partial image 1 display instruction	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080

Partial image 2 display instruction	
PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000

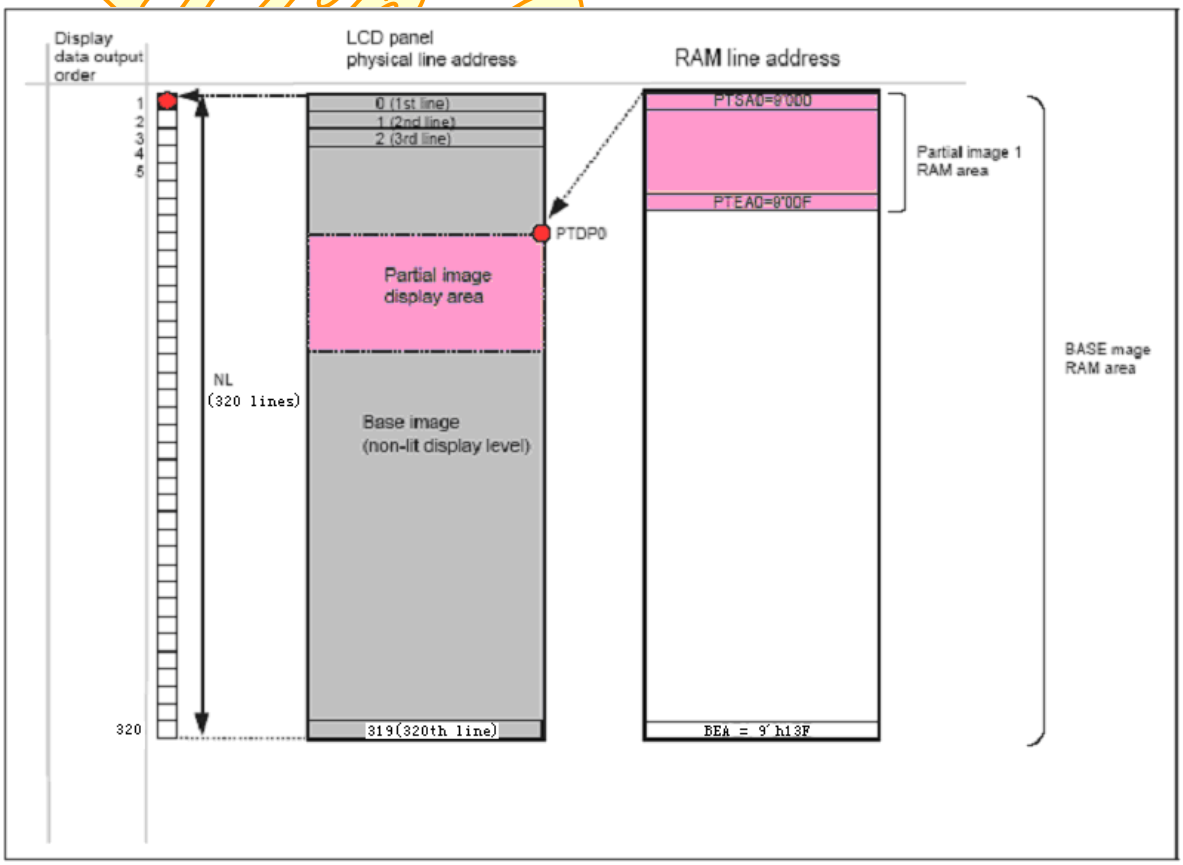


Figure 44: Partial display

13 Gamma Correction

The FT1505C provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels. Furthermore, since the gradient adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

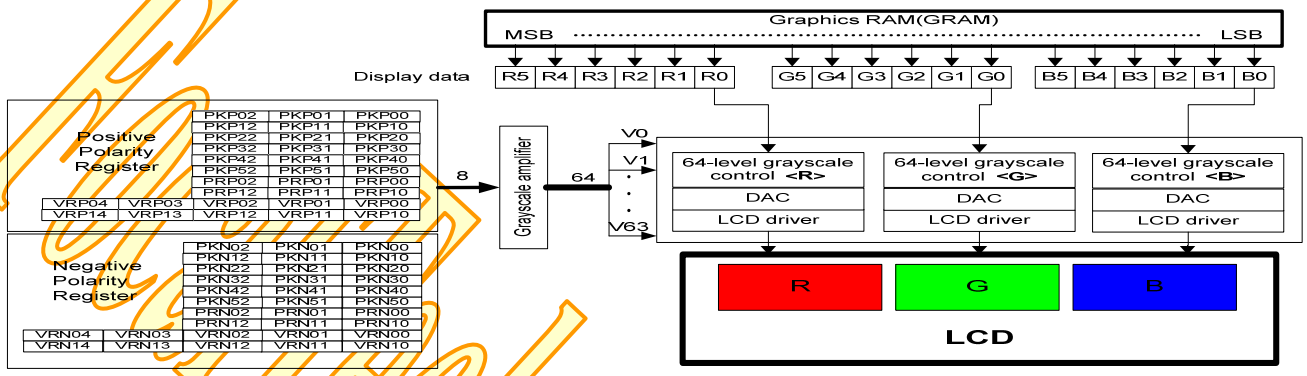


Figure 66: Grayscale control

RAM data (RGB dot data bits) and the source output level

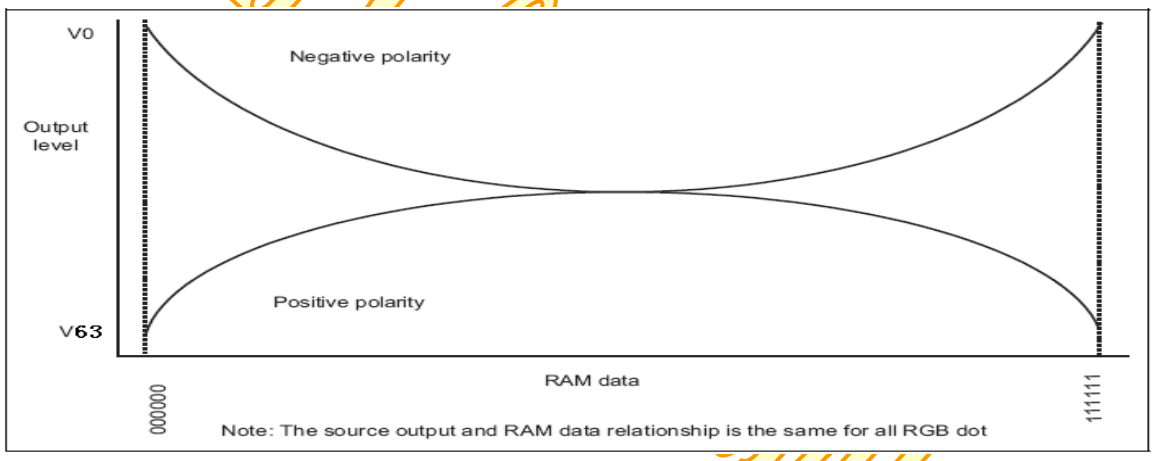


Figure 67

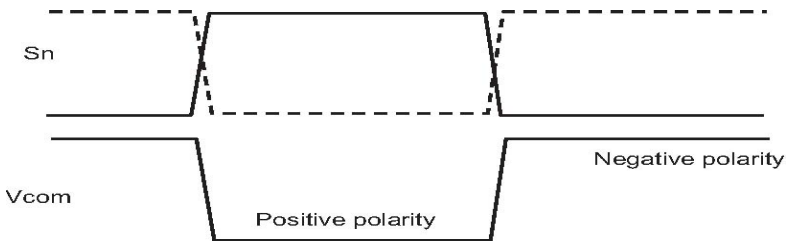


Figure 68: Source output waveform and Vcom polarity

14 Application

14.1 Reset Function

The FT1505C is initialized by the RESET input. During reset period, the FT1505C is in a busy state and instruction from the MPU and GRAM access are not accepted. The FT1505C's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 10 ms). During this period, GRAM access and initial instruction setting are prohibited.

1. Initial state of instruction bits (default)

See the instruction tables. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (D1-0 = "00").

3. Output pin initial state (see note)

1. LCD driver S1~S720 : GND
   G1~G320 : VGL (= GND)
2. Vcom : GND
3. VcomH : Vci
4. VcomL : GND
5. VREG1OUT : VGS
6. VciOUT : Hi-z
7. DDVDH : Vci
8. VGH : DDVDH (= Vci)
9. VGL : GND
10. VCL : GND
11. FMARK : Halt (GND output)
12. Oscillator : Oscillate
13. SDO : High-level (IOVcc) when IM[3:1]=010(serial interface),
    : Hi-z when IM[3:1]<>010(other than serial interface).

4. Initial state of input/output pins* see Note

1. C11A : Hi-z
2. C11B : Hi-z
3. C12A : Hi-z
4. C12B : Hi-z
5. C13A : Vci1 (= Hi-z)
6. C13B : GND
7. C21A : DDVDH (= Vci)
8. C21B : GND
9. C22A : DDVDH (= Vci)
10. C22B : GND
11. VDD : 1.7v

Note: The initial states of output and input pins become the state mentioned above when the FT1505C's power supply circuit is connected as exemplified in "Connection example".

5. Note on Reset function

- When a RESET input is entered into the FT1505C while it is in deep standby mode, the FT1505C starts up the internal logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable. For this reason, do not enter a RESET input in deep standby mode.
- When transferring instruction and data in either two or three transfers via 8-/9-/16-bit interface, make sure to execute data transfer synchronization after reset operation.

14.2 Resizing function

The FT1505C supports resizing function (x 1/2, x 1/4), executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit, which sets the contraction factor (x1/2 or x1/4) of the image. This function enables the FT1505C to write the resized image data （Original resolution < 240*320）directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The FT1505C processes the contraction of an image simply by selecting pixels from original image data. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.

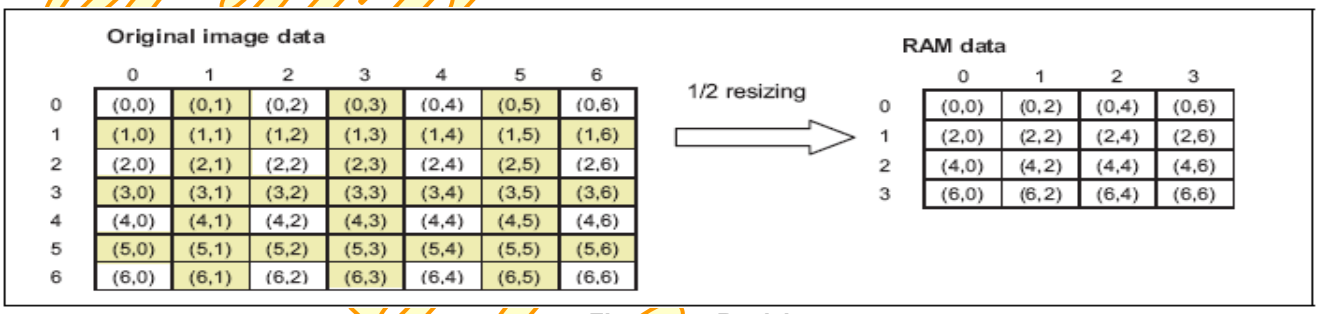


Figure 45: Resizing

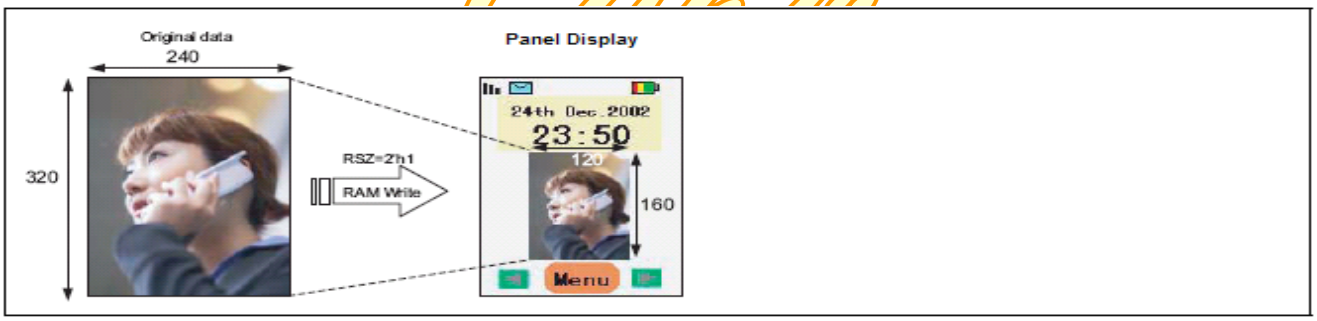


Figure 46: Resizing transfer, display example

Table 64

Original image size (X x Y)	Resized image size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
240x320 (QVGA)	120x160	60x80
176x220 (QCIF)	88x110	44x55
120x160	60x80	30x40
132x176	66x88	33x44

14.2.1 Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

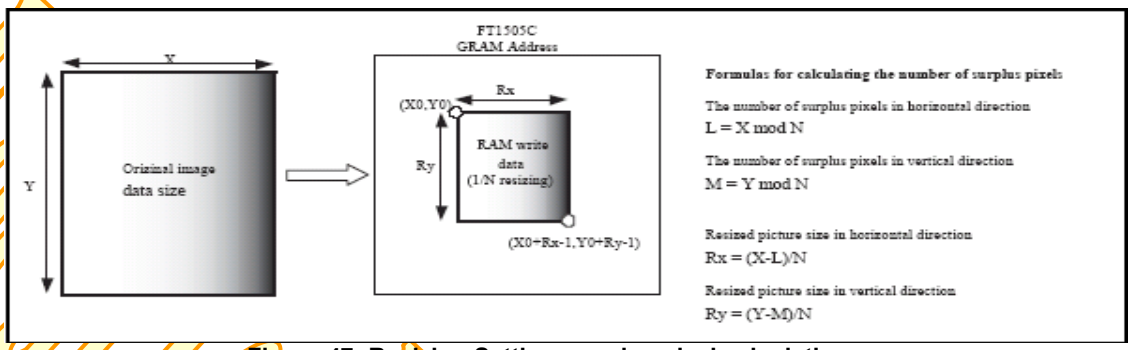


Figure 47: Resizing Setting, surplus pixel calculation

Table 65

Image (before resizing)	
Number of data in horizontal direction	X
Number of data in vertical direction	Y
Resizing ratio	1/N

Register setting in the FT1505C		
Resizing setting	RSZ	N-1
Number of data in horizontal direction	RCV	L
Number of data in vertical direction	RCH	M

RAM writing start address	AD	(X0, Y0)
RAM window address	HSA	X0
	HEA	X0+Rx - 1
	VSA	Y0
	VEA	Y0+Ry - 1

14.2.2 Example of 1/2 resizing

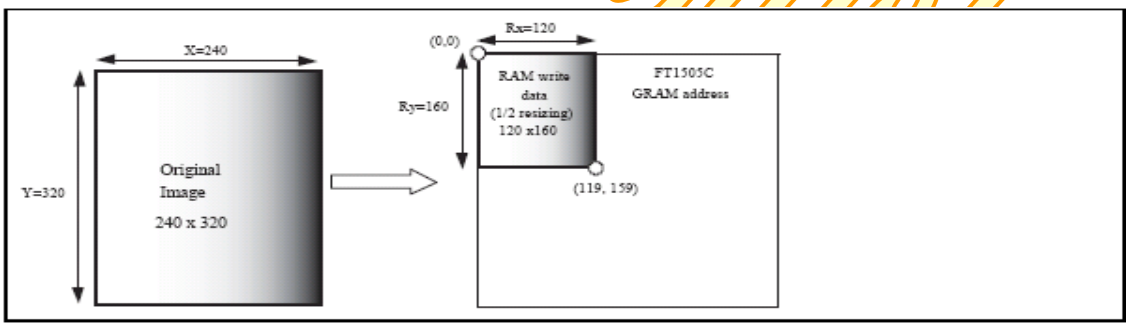


Figure 48: Resizing setting example (x 1/2)

Table 66

Image to transmit

Number of data in horizontal direction	X	176
Number of data in vertical direction	Y	320
Resizing ratio	1/N	1/2

Register setting in the FT1505C

Resizing setting	RSZ	2'h1
Number of data in horizontal direction	RCV	2'h0
Number of data in vertical direction	RCH	2'h0

RAM writing start address	AD	17'h00000
RAM window address	HSA	8'h00
	HEA	8'h77
	VSA	9'h000
	VEA	9'h09F

14.2.3 Resizing instruction bits

Table 67 Resizing factor

RSZ[1:0]	Contraction factor
2h'0	No resizing (x 1)
2h'1	1/2 resizing (x 1/2)
2h'2	Setting disabled
2h'3	1/4 resizing (x 1/4)

Table 68 Surplus pixels

Vertical direction 1 pixel = 1 RGB

RCV[1:0]	Surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

horizontal direction 1 pixel = 1 RGB

RCH[1:0]	Surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

14.2.4 Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

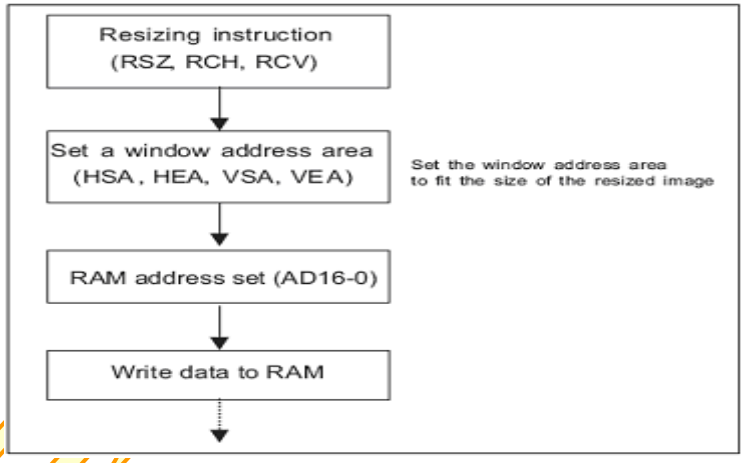


Figure 49: RAM write with resizing

14.3 FMARK Function

The F1505 outputs an FMARK pulse when the FT1505C is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

The FMARK output interval is set by FMI[2:0] bits. Set FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. Set FMARKOE = 1 when outputting FMARK pulse from the FMARK pin.

Table 69

FMP[8:0]	FMARK output position
9'h000	0th line
9'h001	1st line
9'h002	2nd line
….	….
9'h14E	334th line
9'h14F	335th line
9'h150~1FF	Setting disabled

Table 70

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

FMP setting example

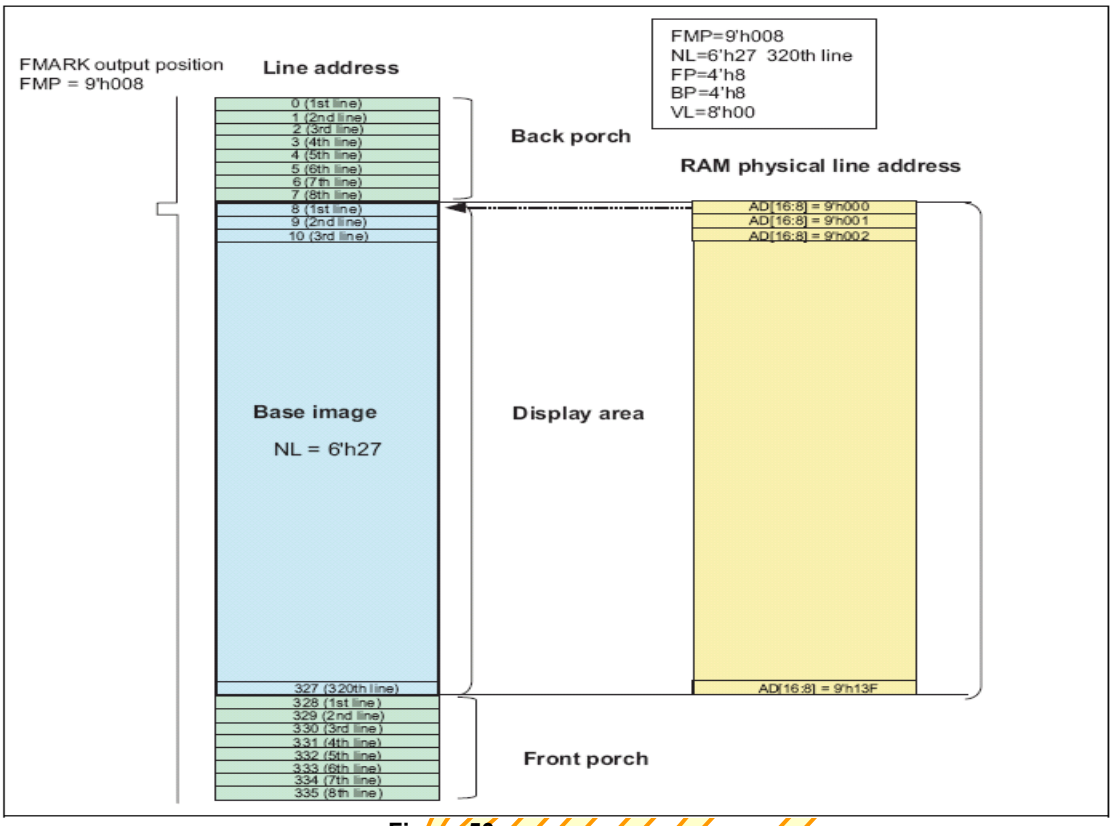


Figure 50

Display operation synchronous data transfer using FMARK

The FT1505C uses FMARK signal as a trigger signal to start writing data to the internal GRAM in synchronization with display scan operation.

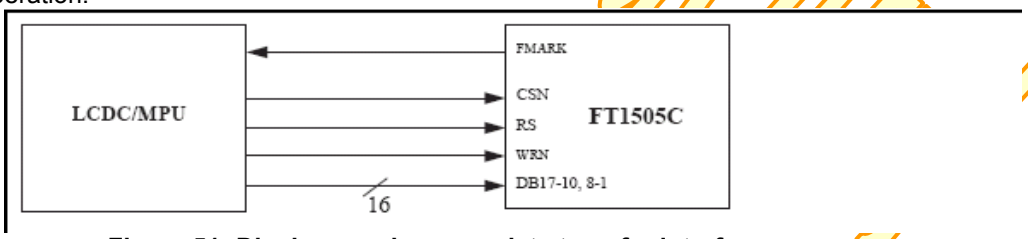


Figure 51: Display synchronous data transfer interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture GRAM area without causing flicker on the display. The data is written in the internal GRAM in order to transfer only the data written over the moving picture display area and minimize the data transfer required for moving picture display.

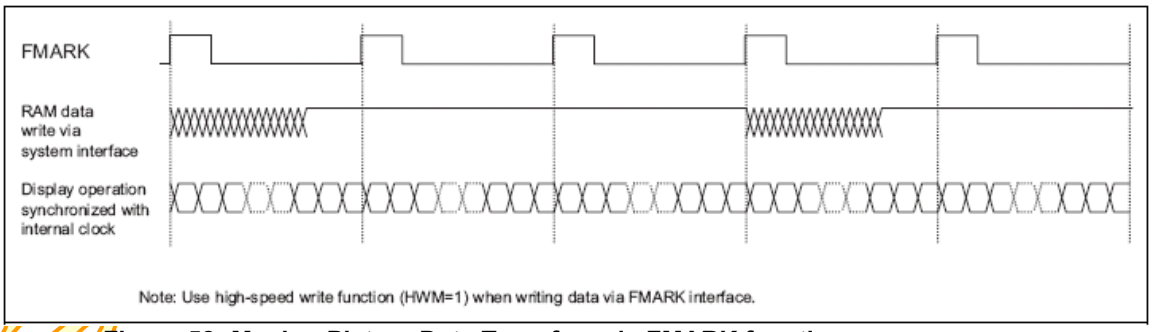


Figure 52: Moving Picture Data Transfers via FMARK function

When transferring data in synchronization with FMARK signal, minimum GRAM data write speed and internal clock frequency must be taken into consideration. They must be more than the values calculated from the following equations.

Internal clock/oscillator frequency (fosc) [Hz]
*= FrameFrequency * (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) * 16(clocks) * variance*

RAMWrieSpeed(min.)[Hz] >

$$\frac{240 * \text{DisplayLines (NL)}}{(\text{FrontPorch (FP)} + \text{BackPorch (BP)} + \text{DisplayLines (NL)} - \text{margin}) * 16 \text{ (clocks)} * \frac{1}{\text{fosc}}}$$

Note: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Examples of calculating minimum RAM data write speed and internal clock frequency is as follows.

[Example]	
Panel size	240 RGB * 320 lines (NL = 6'h13)
Total number of lines (NL)	320 lines
Back/front porch	14/2 lines (BP = 4h'E, FP = 4'h2)
Frame marker position (FMP)	Display end line: 320th (FMP = 9'h14E)
Frame frequency	60Hz

Internal clock/oscillator frequency (fosc) [Hz] = 60 Hz * (320 + 2+ 14) lines * 16 clocks * 1.1 / 0.9 = 394 kHz

Notes:
1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one FMARK cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM write [Hz] > 240 * 320 / {((2+14+320-2) lines * 16 clocks) * 1/394 kHz} = 5.67 MHz

Notes:
1. In this example, it is assumed that the FT1505C starts writing data in the internal RAM on the rising edge of FMARK.
2. There must be at least a margin of 2 lines between the line to which the FT1505C has just written data and the line where display operation on the LCD is performed.
3. The FMARL signal output position is set to the line specified by FMP[8:0] bits.

In this example, RAM write operation at a speed of 5.67 MHz or more, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the FT1505C starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

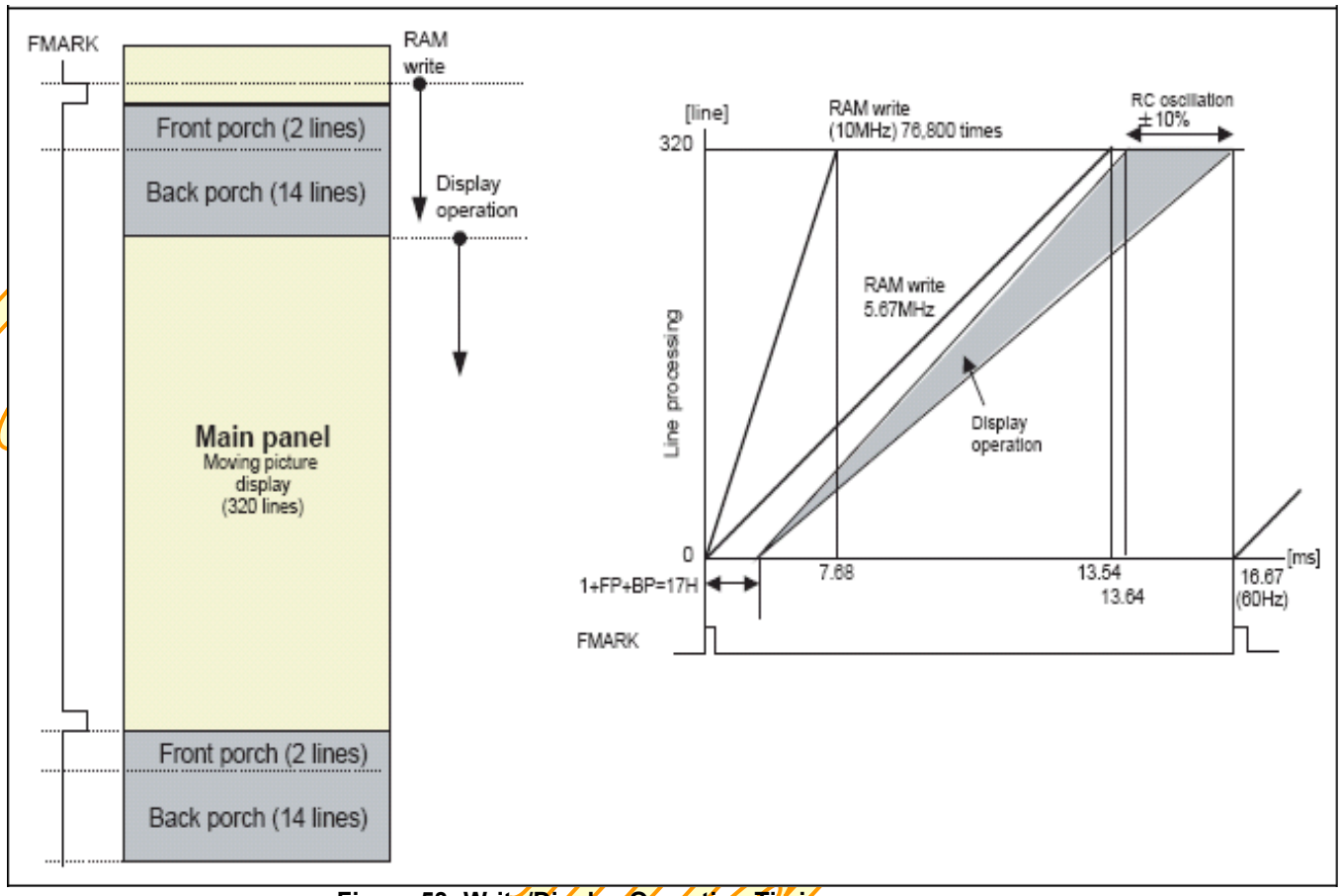


Figure 53: Write/Display Operation Timing

Notes to display operation synchronous data transfer using FMARK signal

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make an enough margin in setting RAM write speed for this operation.

14.4 Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the FT1505C to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area]	
(horizontal direction)	8'h00 ≤ HSA ≤ HEA ≤ 8'hEF
(vertical direction)	9'h000 ≤ VSA ≤ VEA ≤ 9'h13F
[RAM address (AD16-0)]	
(RAM address)	HSA ≤ AD7-0 ≤ HEA VSA ≤ AD16-8 ≤ VEA

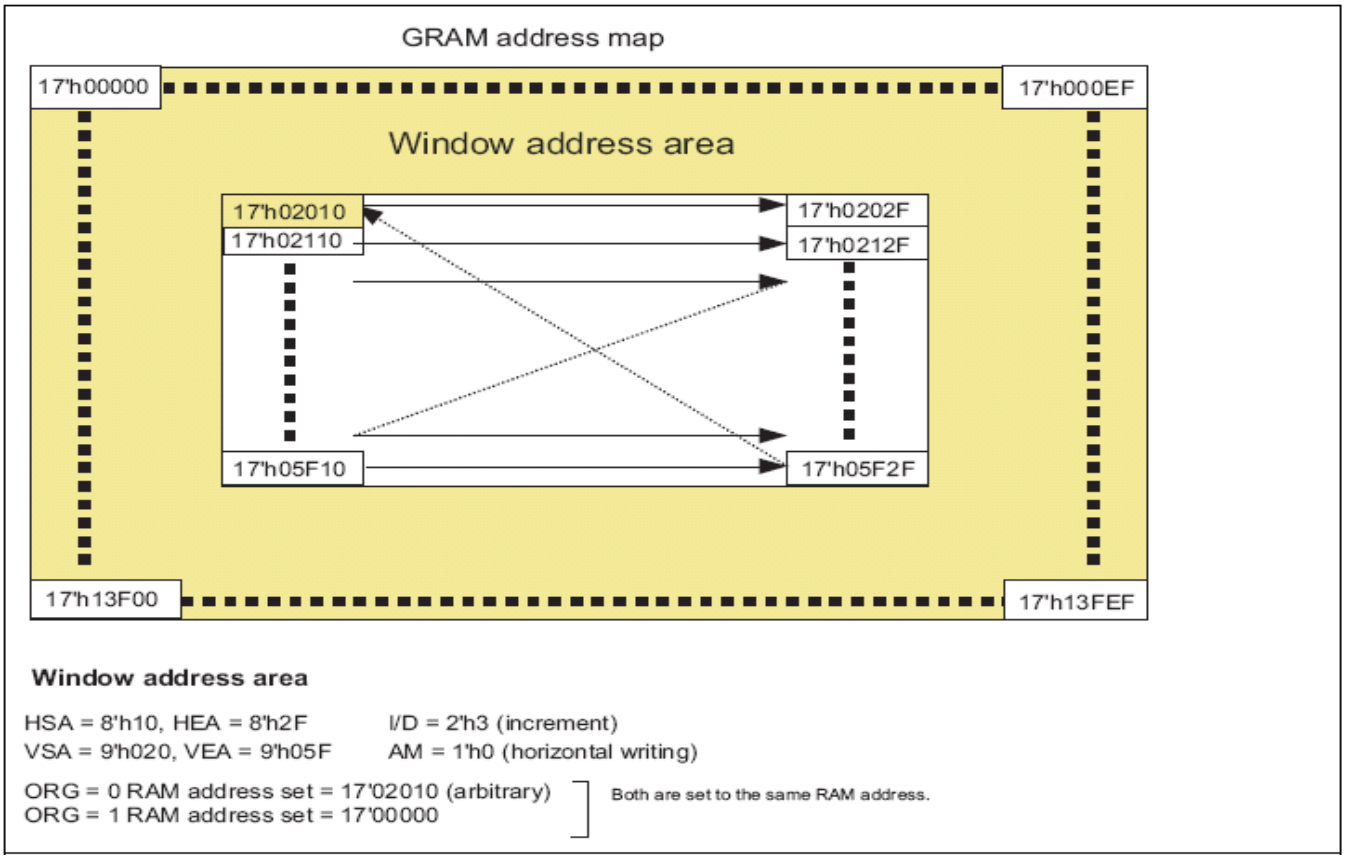


Figure 57: Automatic address update within a Window Address Area

14.5 Scan Mode Setting

The FT1505C allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the FT1505C and the LCD panel.

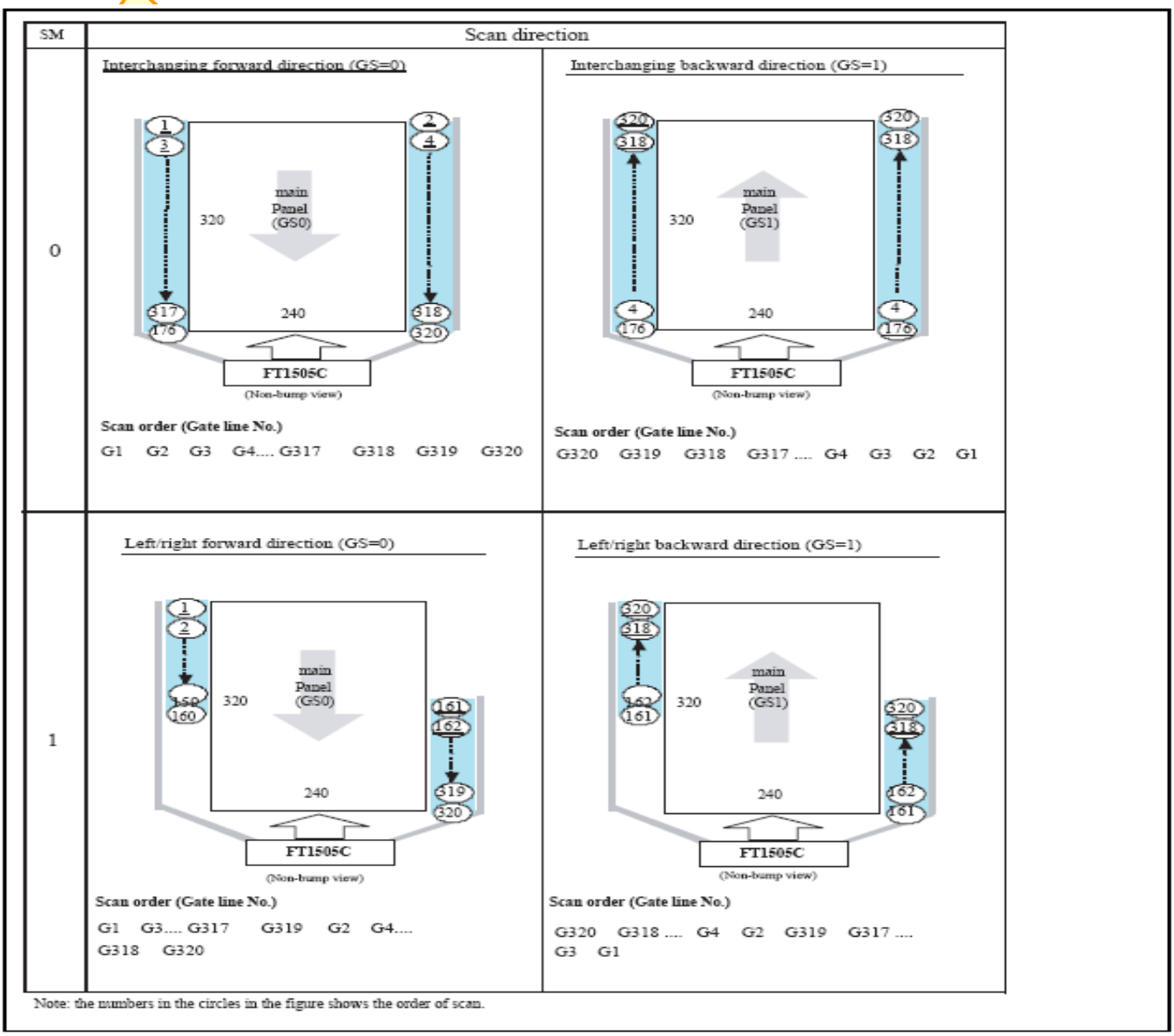


Figure 58

14.6 8-color Display Mode

In 8-color display mode, the γ-adjustment registers PKP0-PKP5, PKN0-PKN5, PRP0, PRP1, PRN0, PRN1 are disabled and the power supplies to V1 to V62 are halted. The FT1505C **does** require GRAM data rewrite for 8-color display by writing the MSB to the rest in each dot data to display in 8 colors.

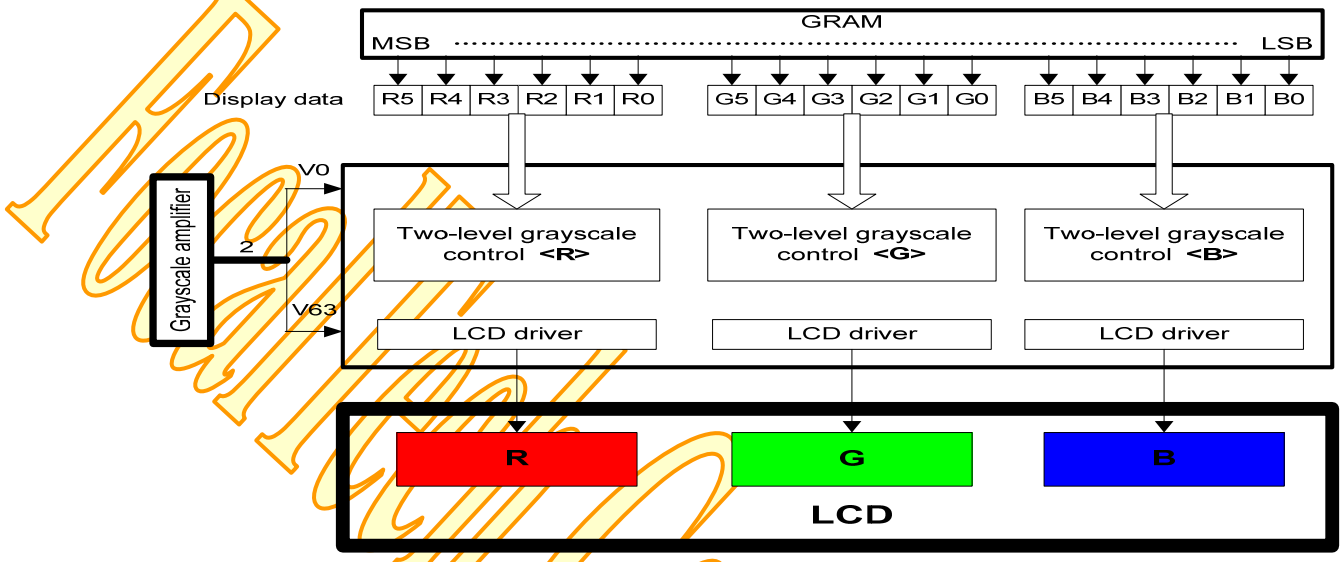


Figure 59

14.7 n-line Inversion AC Drive

The FT1505C, in addition to the frame-inversion liquid crystal alternating current drive, supports the n-line inversion alternating current drive to invert the polarity of liquid crystal in every n-line periods, where n takes a number from 1 to 64. The n-line inversion can provide a solution when there is a need to improve the display quality.

In determining "n" (the value represented by NW bits +1), check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.

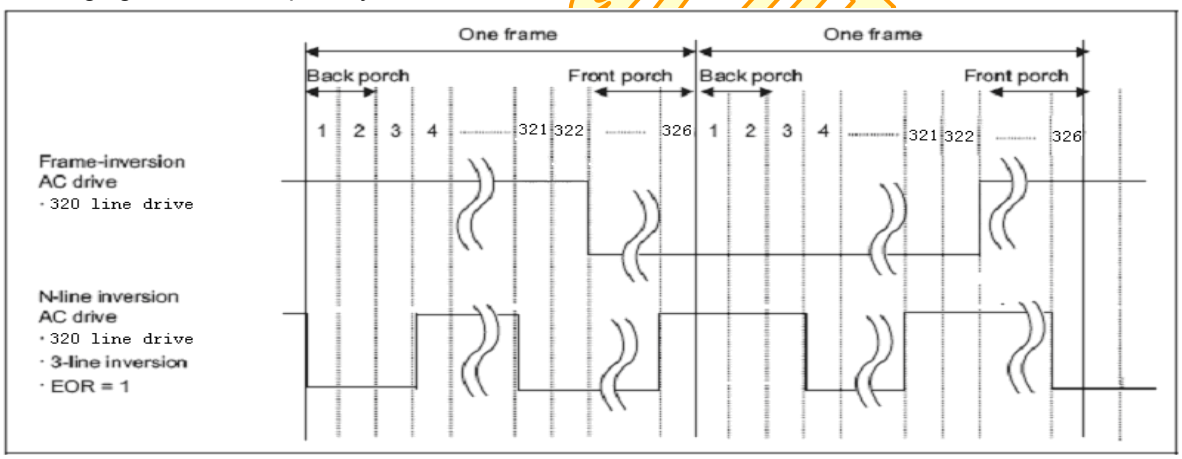


Figure 60

Note: Make sure to set EOR = "1" to prevent direct bias on liquid crystal when selecting n-line inversion drive.

14.8 Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the FT1505C draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of n-line inversion AC drive, polarity is inverted as the FT1505C draws n line, and a blank period lasting for (BP+FP) periods is inserted when the FT1505C draws one frame.

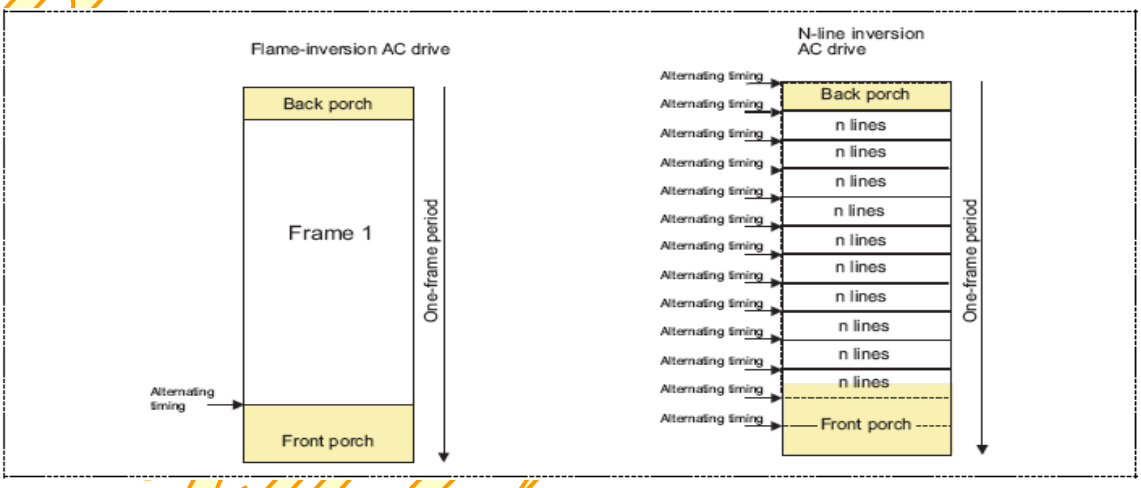


Figure 61

14.9 Frame-Frequency Adjustment Function

The FT1505C supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIVI, RTNI bits without changing the oscillation frequency.

The FT1505C allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIVI and RTNI settings, the FT1505C can operate at high frame frequency when displaying a moving picture, which requires the FT1505C to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between liquid crystal drive duty and frame frequency

The following equation represents the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTNI) and the operation clock frequency division ratio setting bit (DIVI).

(Formula to calculate frame frequency)

Frame frequency = fosc/[Clock cycles per line × division ratio × (Line+BP+FP)] [Hz]

fosc: RC oscillation frequency
Line: number of lines to drive a panel (NL bits)
Clock cycles per line: RTNI bits
Division ratio: DIVI bits
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive a panel: 320 lines
1H period: 16 clock cycles (RTNI4-0 = “10000”)
Operation clock division ratio: 1/1
Front porch (FP): 2 line periods
Back porch (BP): 14 line periods

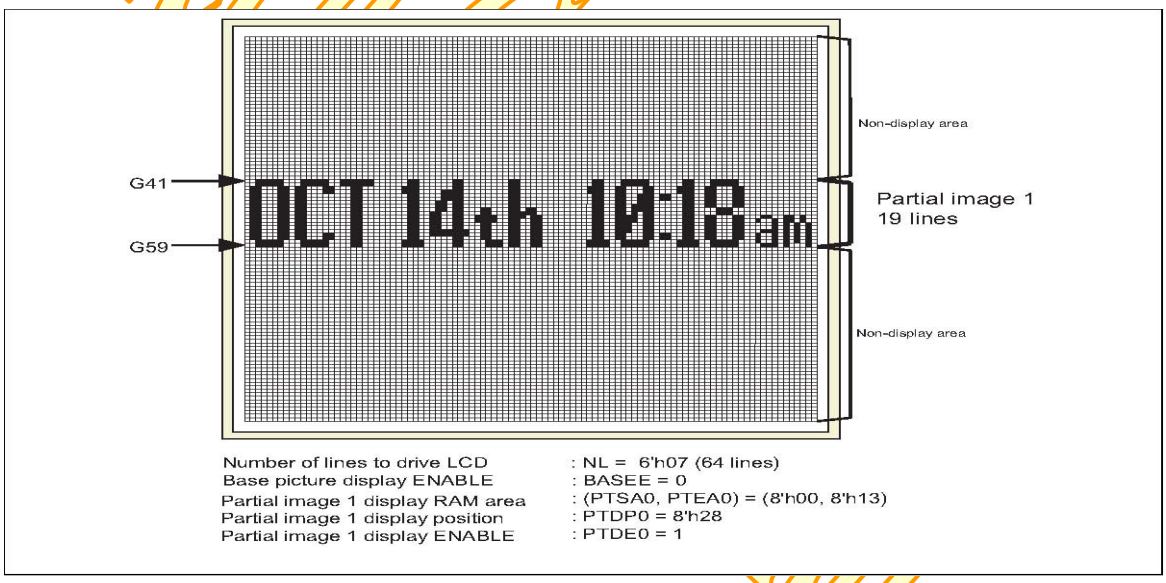
$$fosc = 60\ (Hz) \times (0+16)\ (clocks) \times 1/1 \times (320 + 2 + 14)\ (lines) = 323\ (kHz)$$

In this case, the RC oscillation frequency is 323k Hz. Set register (RB0h) RC[2:0] = “100” for internal oscillator or adjust the external RC oscillator to set the frequency to 323k Hz.

14.10 Partial Display Function

The partial display function allows the FT1505C to drive lines selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.



Note: See the “RAM Address and Display Position on the Panel” for details on the relationship between the display position on the panel and the RAM area setting for partial image.

Figure 62

14.11 Low power consumption drive settings

The FT1505C supports the following low power consumption drive methods to drive the panel with less power requirement. Generally, there is a trade-off between power efficiency and quality of display. Also, the power efficiency depends on the characteristics of the panel. Check which of the following methods can achieve the optimal balance between power consumption and display quality.

1. 8-color display mode (COL)

In this mode (CL = "1"), the FT1505C halts power supplies except for V0 and V63. In this mode, the FT1505C display in 8 colors to save power.

2. Partial display

In this mode, the data is displayed as partial image and the base image is turned off (BASEE = 0). The normal display operation is limited to the partial display area to save power.

The source output level in non-display area can be changed by instruction (PTS[2:0]). The PTS[2:0] setting allows halting the operation of grayscale voltage generating amplifiers except for V0, V63 and slowing down the clock frequency for step-up operation to half the normal operation frequency.

Table 72 Source outputs in non-display area

PTS[2:0]	Source output in non-display area		Non-display area Grayscale amp operation	Non-display area Step-up clock frequency
	Positive polarity	Negative polarity		
3'h0	V63	V0	V0 to V63	Set by DC0, DC1 bits
3'h1	Setting disabled	Setting disabled	-	-
3'h2	GND	GND	V0 to V63	Set by DC0, DC1 bits
3'h3	Hi-Z	Hi-Z	V0 to V63	Set by DC0, DC1 bits
3'h4	V63	V0	V0, V63	1/2 the frequency set by DC0, DC1 bits
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0, V63	1/2 the frequency set by DC0, DC1 bits
3'h7	Hi-Z	Hi-Z	V0, V63	1/2 the frequency set by DC0, DC1 bits

See also "Partial Display Function" for details.

3. Frame frequency setting

The FT1505C allows changing the liquid crystal polarity inversion cycle by changing the frame frequency by setting DIVI, RTNI bits. To improve power efficiency, set a lower frequency in partial display operation, which requires small power consumption. See also "Frame-Frequency Adjustment Function" for details.

Generally, there is a trade-off between power efficiency and quality of display. The power efficiency also depends on the characteristics of the panel. Check the optimal balance between the quality of display on the panel and the power efficiency before use.

4. Liquid crystal inversion drive

The FT1505C allows selecting liquid crystal inversion drive method from frame-inversion AC drive or line-inversion AC drive by setting B/C, NW bits. Select either appropriate LCD driving method for the kind of display on the panel. Also, see "n-line

Inversion AC Drive" for details.

Generally, there is a trade-off between power efficiency and quality of display. The power efficiency also depends on the characteristics of the panel. Check the optimal balance between the quality of display on the panel and the power efficiency before use.

5. Optimizing step-up factor

There are cases that power loss in driving liquid crystal can be minimized by optimizing the step-up factor. Whether this method proves to be effective or not depends on the characteristics of the liquid crystal panel. The step-up factor is set by BT[3:0].

14.12 LCD panel interface timing

The following are the relationships between external display interface signals and LCD panel signals when the display operation is synchronized with the internal clock signal.

Internal clock operation

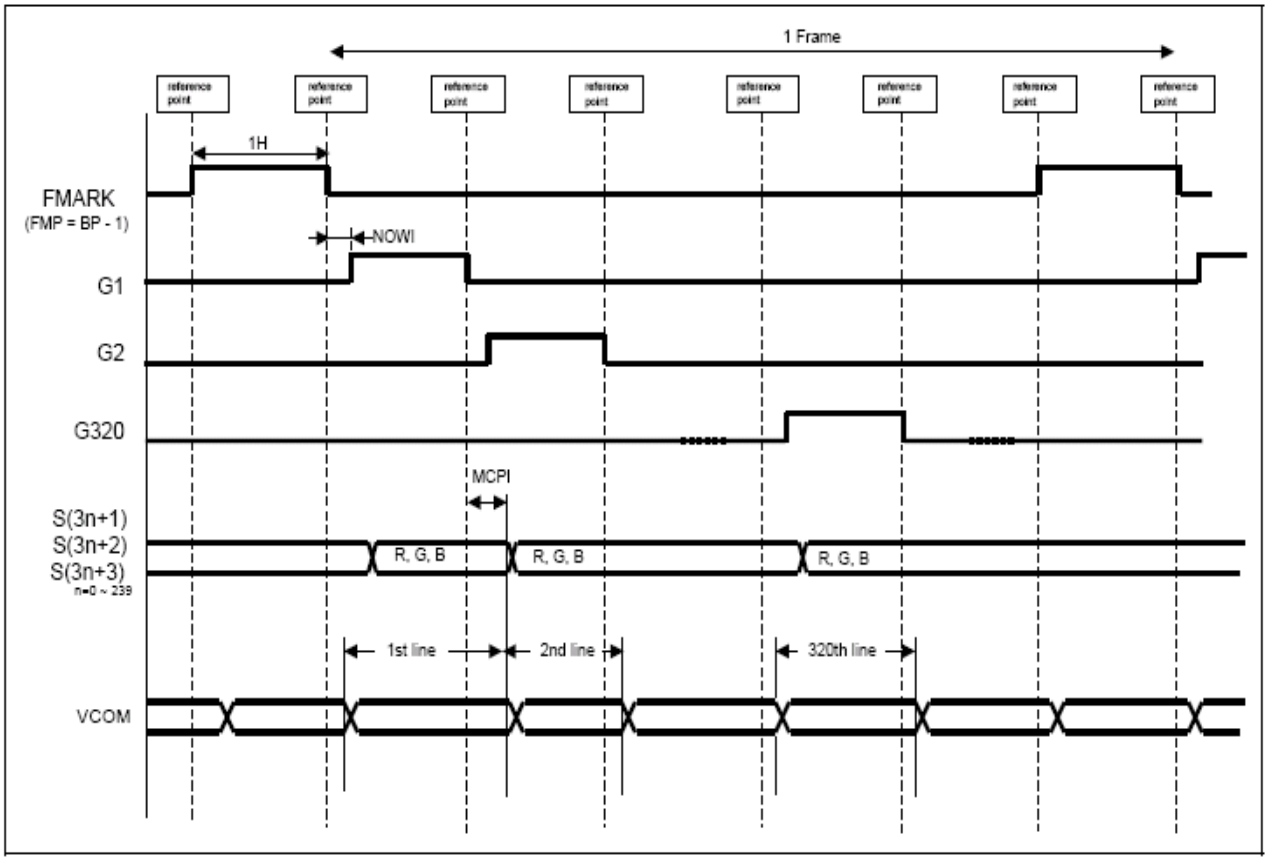


Figure 63

14.13 Power Supply Generating Circuit

The following is the configuration of LCD drive voltage generating circuit of the FT1505C.

15 Power supply circuit connection example1 (Vci1=VciOUT)

The VciOUT output circuit changes the VciOUT level in this example.

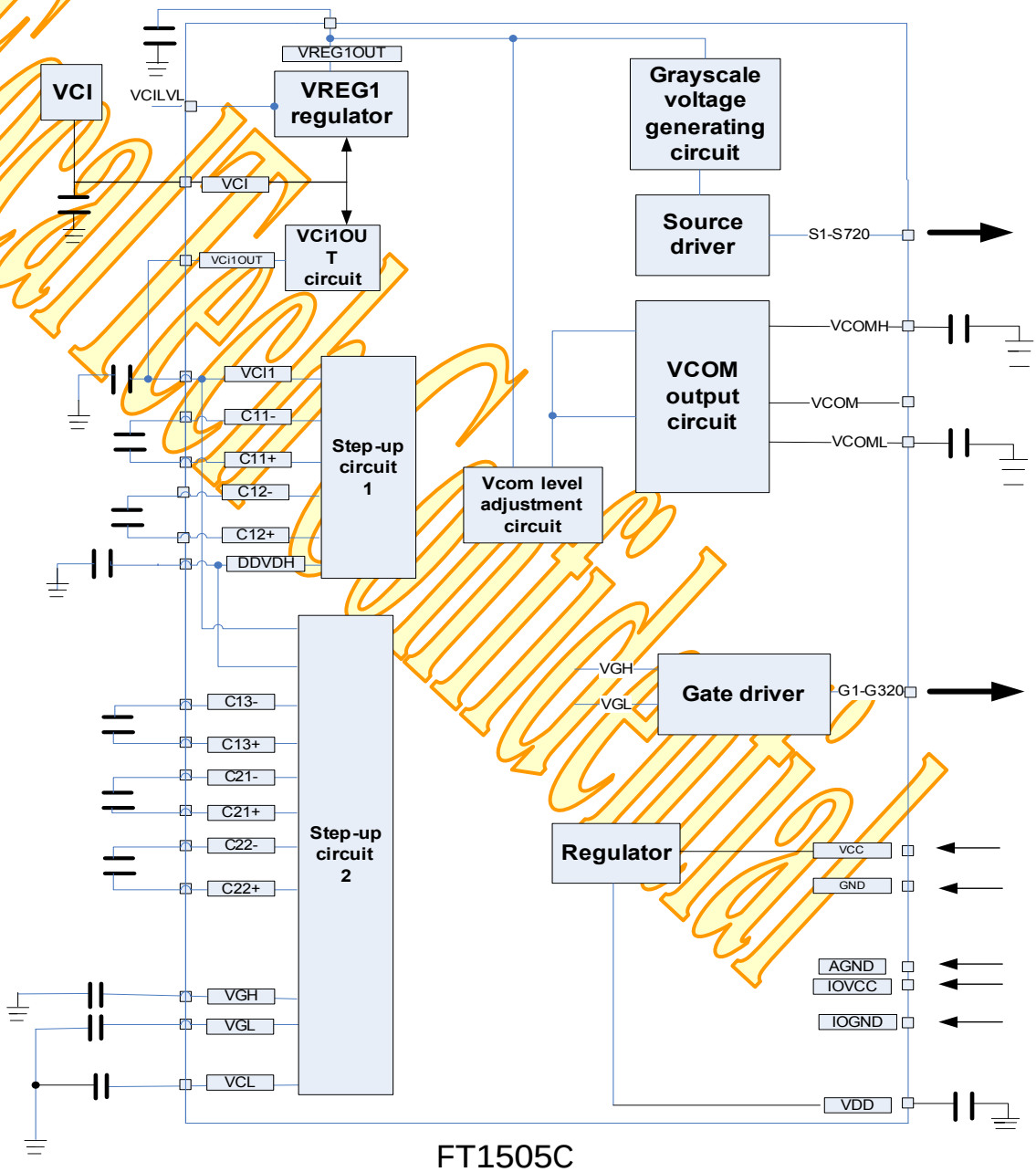


Figure 69

15.1 Specifications of external elements for the power supply circuit

The specifications of external elements connected to the power supply circuit of the FT1505C are as follows.

Table 73 Capacitor

Capacitance	Upper voltage limit	Pin connection
1μF Characteristics B	6V	Vci，VCL，VREG1OUT, VciOUT, VcomH， VcomL, C11B/A, C12B/A, C13B/A
	10V	DDVDH, C21B/A，C22B/A
	25V	VGH, VGL

Notes: 1. Checking with the LC module is required.
2. The numbers in the parentheses correspond to the numbers in Figure 79 and Figure 80.

Table 74 Schottky diode

Specification	Pin connection
VF ＜ 0.4V/20mA@25℃, VR≧25V (Recommended diode: HSC226)	**NO NEEDED ！**

Table 76 Internal logic power supply

Capacitor	Recommended voltage proof	Pin connection
lμF (B characteristics)	**3V**	**VDD**

15.2 Voltage generation diagram

The following are the diagrams of voltage generation in the FT1505C and the TFT display application voltage waveforms and electrical potential relationship.

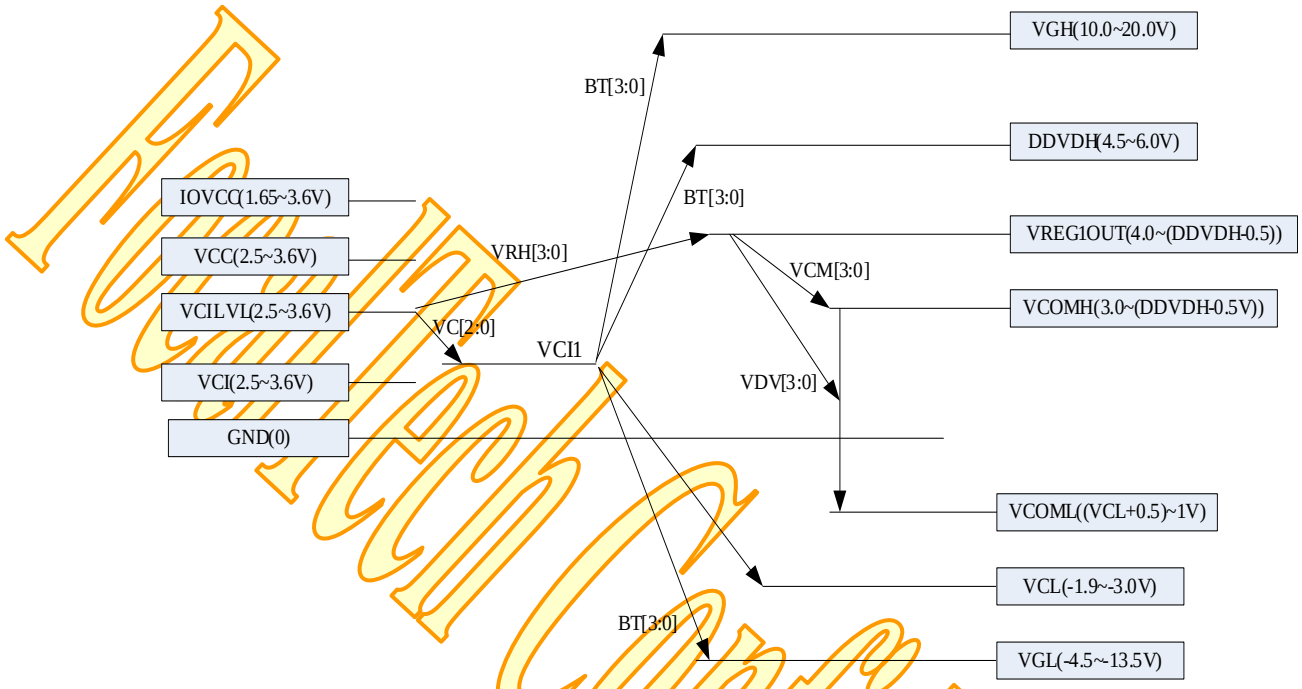


Figure 71: Pattern diagram for voltage setting

Notes: 1. The DDVDH, VGH, VGL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage levels in operation do not conflict with the following conditions: (DDVDH – VREG1OUT) > 0.5V, (DDVDH – VcomH) > 0.5V, (VcomL – VCL) > 0.5V. When the alternating cycle of Vcom is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. In operation, setting voltages within the respective voltage ranges are recommended.

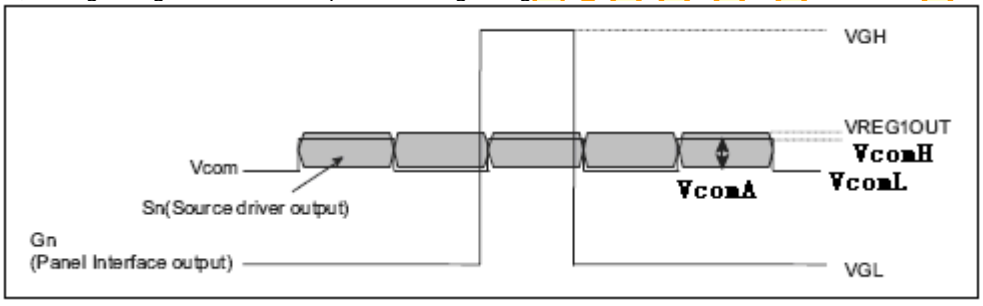


Figure 72: TFT display application voltage waveform and electrical potential

15.3 Power Supply Setting sequence

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences (in case of not using internal power supply sequencer).

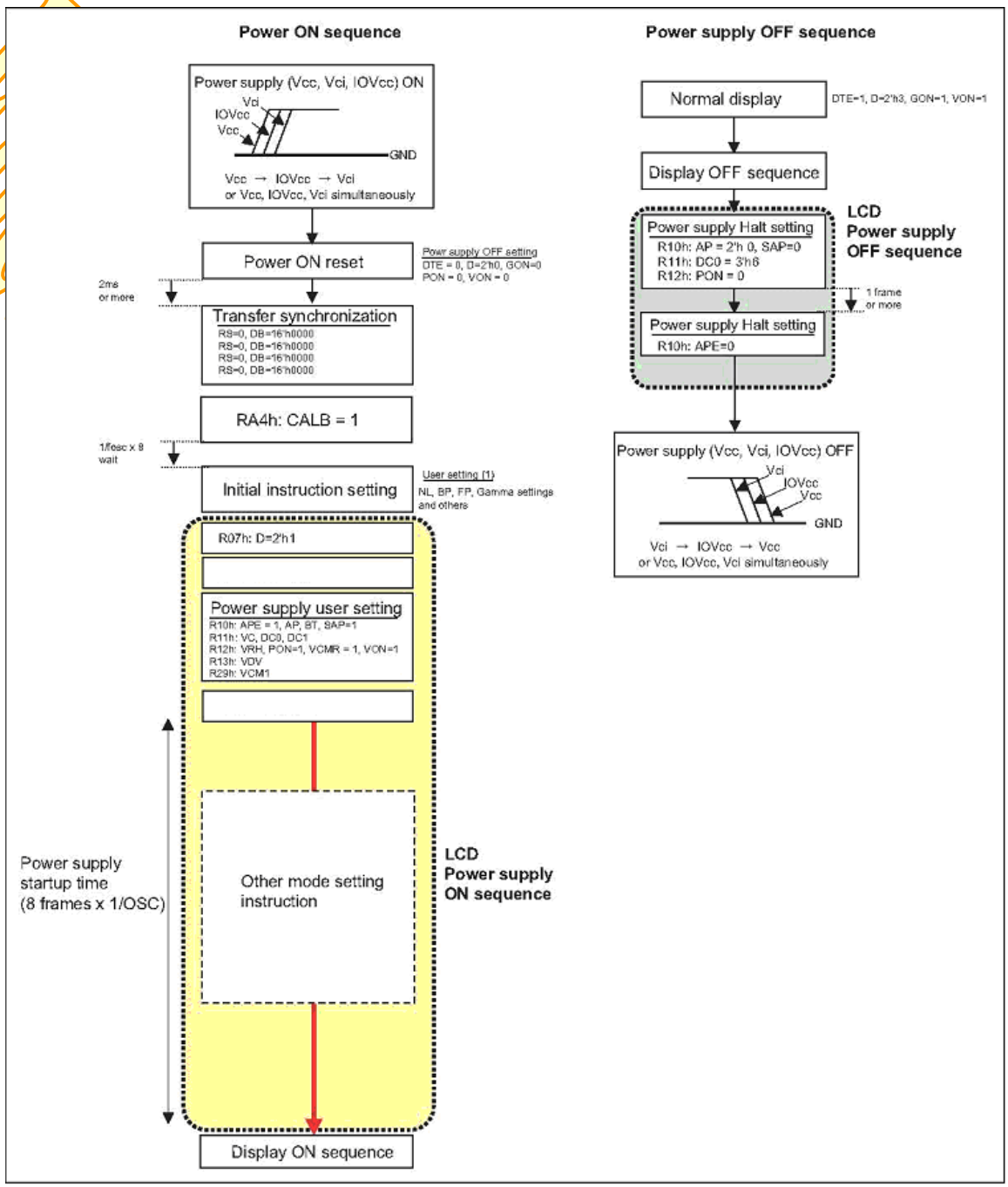


Figure 73

15.4 Instruction Setting

The following are the sequences for various instruction settings. When setting instruction in the FT1505C, follow the sequence below.

15.4.1 Display ON/OFF

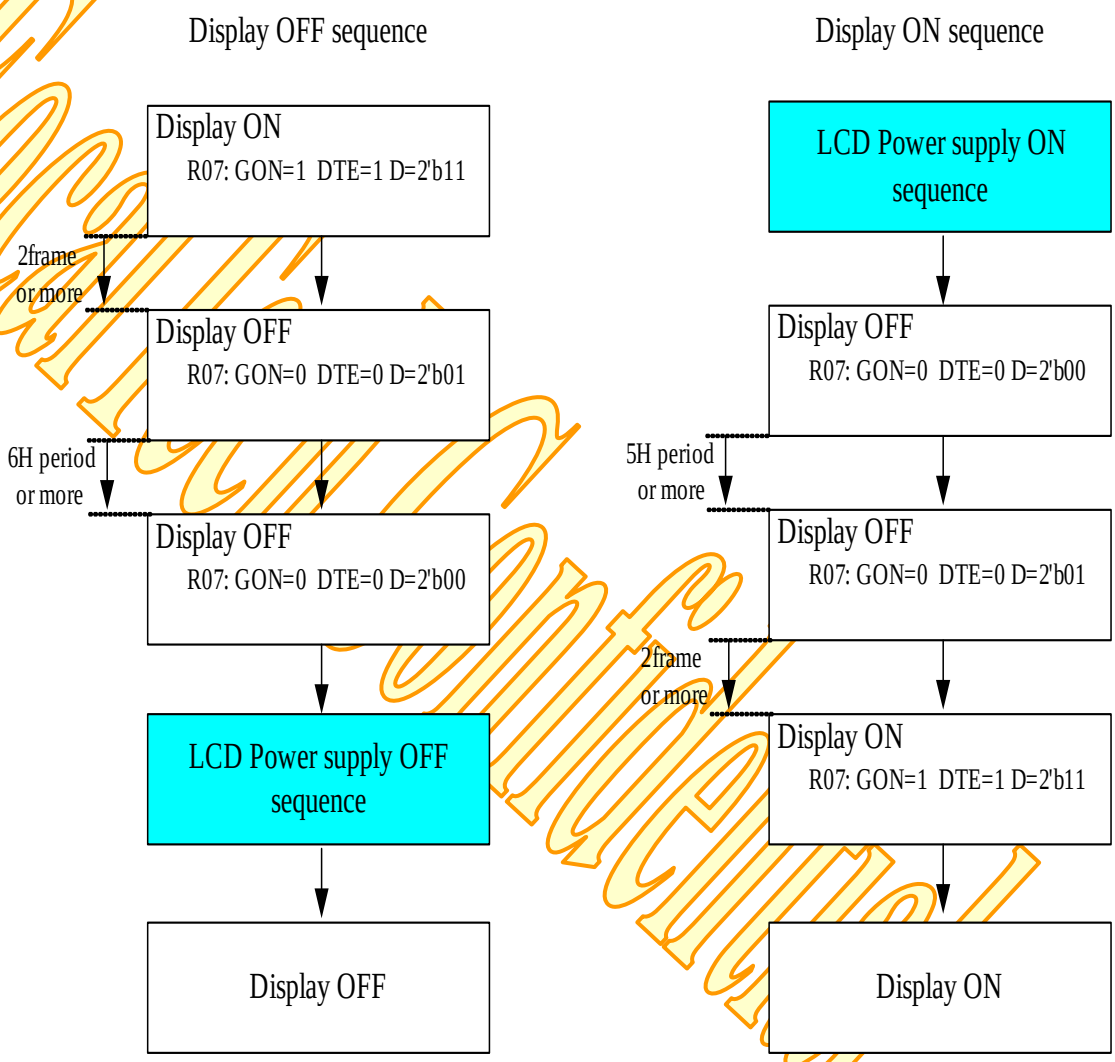


Figure 74

15.4.2 Sleep/Standby mode

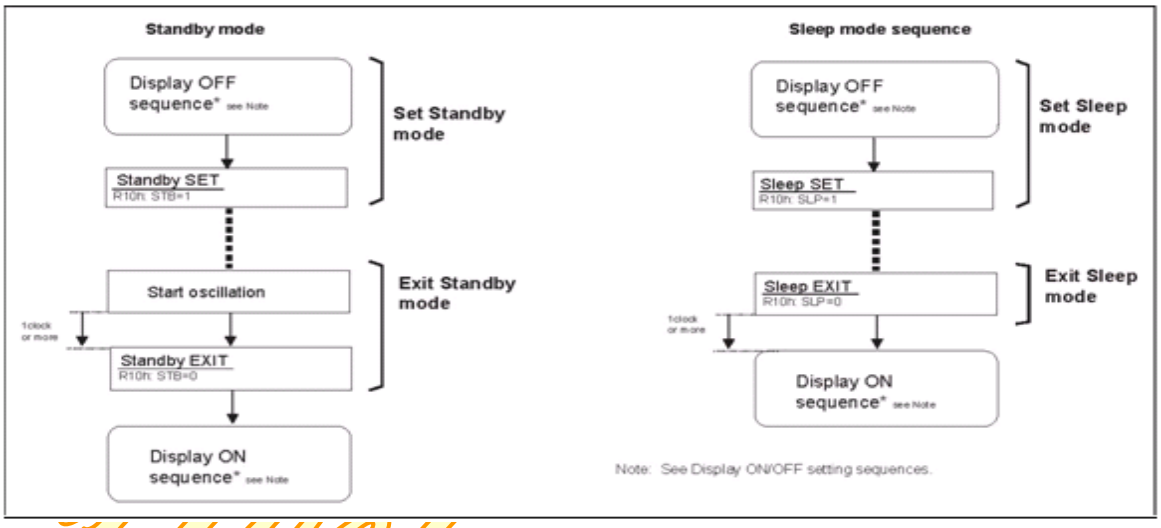


Figure 75

15.4.3 Deep standby mode

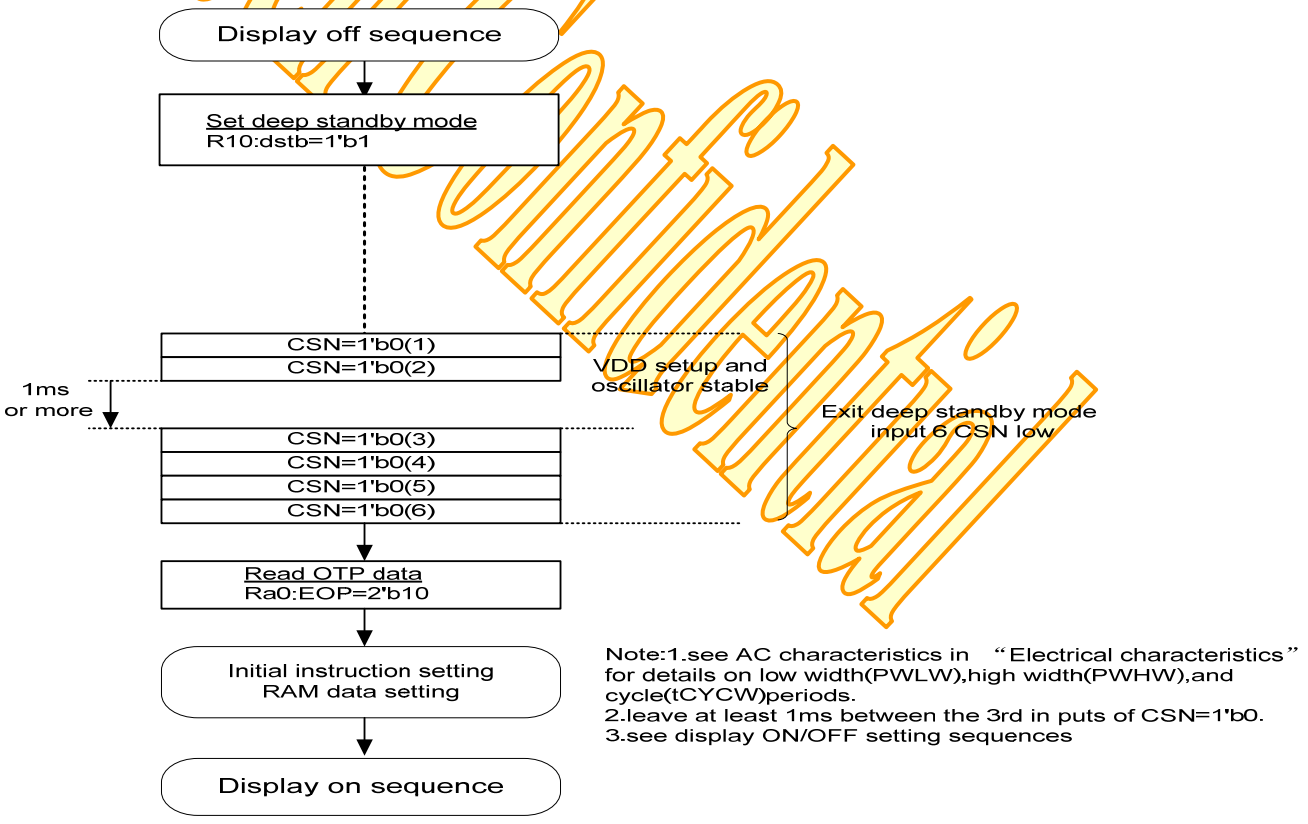


Figure 76

15.5 FT1505C Recommended resistance and connection example

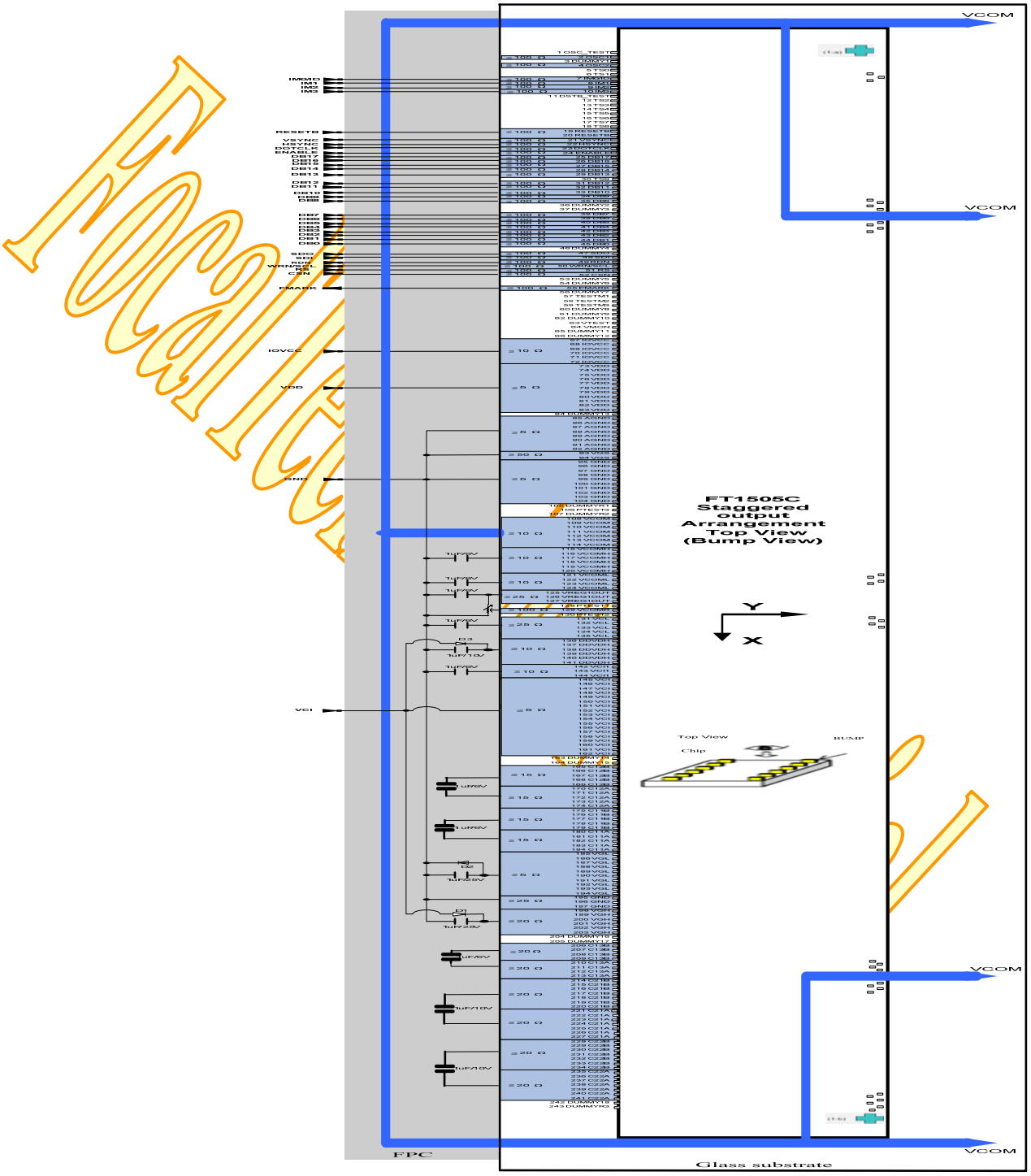


Figure 78

16 Electrical Characteristics

16.1 Absolute Maximum Ratings

Table 77

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	IOVcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci -AGND	V	-0.3 ~ + 4.6	1, 3
Power supply voltage (3)	DDVDH - AGND	V	-0.3 ~ + 6.5	1, 4
Power supply voltage (4)	VGH - VGL	V	+11.0 ~ + 27.0	1, 4
Power supply voltage (5)	AGND - VGL	V	+3.0 ~ +13.0	1, 7
Power supply voltage (6)	DDVDH - VGL	V	+7.0 ~ +19.0	1, 5
Power supply voltage (7)	Vci - VGL	V	+5.5 ~ +16.8	1, 7
Input voltage	Vt	V	-0.3 ~ Vci + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 8
Storage temperature	Tstg	°C	-55 ~ + 110	1

Notes: 1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure Vci (high) ≥ GND (low) and IOVcc (high) ≥ GND (low).
3. Make sure Vci (high) ≥ AGND (low).
4. Make sure DDVDH (high) ≥ AGND (low).
5. Make sure DDVDH (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ AGND (low).
7. Make sure AGND (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

16.2 DC Characteristics

Table 78 **(Vci = 2.4V ~ 3.3V, IOVcc = 1.65V ~ 3.3V, Ta = -40°C ~ 85°C)** see Note 1

Item	Symbol	Unit	TestCondition	Min.	Typ.	Max.	Notes
Input high-level voltage	VIH	V	IOVcc = 1.65V ~ 3.3 V	0.8 x IOVcc	—	IOVcc	2, 3
Input low-level voltage	VIL	V	IOVcc = 1.65V ~ 3.3 V	– 0.3	—	0.2 x IOVcc	2, 3
Output high voltage (DB0-17 pins, FMARK)	VOH	V	IOVcc = 1.65V ~ 3.3 V IOH = -0.1mA	0.8 x IOVcc	—	—	2
Output low voltage (DB0-17 pins, FMARK)	VOL	V	IOVcc = 1.65V ~ 3.3 V IOL = 0.1mA	—	—	0.2 x IOVcc	2
I/O leak current	ILi	µA	Vin = 0 ~ IOVcc	–1	—	1	4
Current consumption: (IOVcc-GND) Normal operation mode, 262K color	IOP1	µA	fosc=358kHz (320 lines), fFLM=70Hz, IOVcc=Vci= 3.0V, Ta=25°C, RAM data: 18'h00000	—	175	295	5, 6
Current consumption: (IOVcc-GND) 8-color mode, 64-line partial display	IOP2	µA	fosc=358kHz (64 line partial), fFLM=40Hz, IOVcc=Vci= 3.0V, Ta=25°C, RAM data: 18'h00000	—	140	—	5, 6
Current consumption: (IOVcc-GND) RAM access mode 1 normal operation mode	IRAM1	mA	tCYCW=150ns, IOVcc=2.40V,Vci= 2.4V, Ta=25°C, 80-8bit I/F, TRI=1, Consecutive RAM access during display VCM1=5'h1D, AP=3'h3, BC0=0, FP=5, BP=8, gamma registor:0 (default) CL=0 (8 color)	—	2.0	—	6
Current consumption: (IOVcc-GND)+(Vci-GND) Sleep mode	ISLP	µA	Vcc=Vci=3.00V SLP='1' Ta=25c		45		

Current consumption: (IOVcc-GND)+(Vci-GND) Standby mode	ISTB	μA	Vcc=Vci=3.00V STB='1' Ta=25c		20		
Current consumption: (IOVcc-GND)+(Vci-GND) Deep Standby mode	IDST	μA	Vcc=Vci=3.00V DSTB='1' Ta=25c	—	0.1	1.0	5

16.3 DC Characteristics

Item	Symbol	Unit	TestCondition	Min.	Typ.	Max.	Notes
LCD power supply current (VCI-GND) 260k color display	Ici1	mA	IOVcc=Vci=3.0V, fosc =358kHz (320 lines), fFLM=70Hz, Ta=25°C, RAM data:18'h00000, REV=0, SAP=1, AP=100, DC0=000, DC1=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 B/C=0, BT=001, VC=001, VRH=0011, VCM=100110, VDV=100000, CL=0 No load on the panel	—	2.8	3.3	5, 6
LCD power supply current (VCI-GND) 8-color mode	Ici2	mA	IOVcc=Vci=3.0V, fosc =358kHz (64 lines) fFLM=40Hz, Ta=25°C, RAM data:18'h00000, REV=0, SAP=1, AP=010, DC0=001, DC1=011, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 B/C=0, BT=001, VC=001, VRH=0011, VCM=100110, VDV=011100, CL=1, PTG=10, ISC=0111 No load on the panel	—	1.0	—	5, 6
Source Output voltage dispersion	ΔVo	mV	—	—	5	—	7
Source Average output voltage variance	ΔV	mV	—	-35	—	35	8

16.4 Step-up circuit Characteristics

Table 79

Item		Unit	Test Condition	Min	Typ	Max	Notes
Step-up output voltage	DDVDH	V	IOVcc=Vci= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=001 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, Iload1 = -1[mA]	4.57	4.84	—	11
	VGH	V	IOVcc=Vci= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=000,DC1=010 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, Iload1 = -100[mA]	13.72	14.40	—	11
	VGL	V	IOVcc=Vci= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=000,DC1=010 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, Iload1 = +100[mA]	-6.86	-7.13	—	11
	VCL	V	IOVcc=Vcc= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=000,DC1=010 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, Iload1 = 200[mA]	-2.25	-2.30	—	—
Input voltage	Vci	V		2.4	—	3.3	—

16.5 AC Characteristics

(Vci=2.4V ~ 3.3V, IOVcc = 1.65V ~ 3.3V, Ta = – 40°C ~ +85°C*) * see Note 1

Table 80 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
RC oscillation clock	fOSC	kHz	IOVcc=Vci=3.0V 25°C	250	400	630	9

16.6 80-system Bus Interface Timing Characteristics (18/16-bit I/F)

Table 81 Normal write operation
IOVcc = 1.65V ~ 3.3V, Vci= 2.4V ~ 3.3V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure 87	125	-	-
	Read	tCYCR	ns	Figure 87	450	-	-
Write low-level pulse width		PWLW	ns	Figure 87	45	-	-
Read low-level pulse width		PWLR	ns	Figure 87	170	-	-
Write high-level pulse width		PWHW	ns	Figure 87	70	-	-
Read high-level pulse width		PWHR	ns	Figure 87	250	-	-
Write/Read rise/fall time		tWRr, WRf	ns	Figure 87	-	-	25
Setup time	Write (RS~CSN, WRN)	tAS	ns	Figure 87	0	-	-
	Read (RS~CSN, RDN)				10		
Address hold time		tAH	ns	Figure 87	2	-	-
Write data setup time		tDSW	ns	Figure 87	25	-	-
Write data hold time		tHWR	ns	Figure 87	10	-	-
Read data delay time		tDDR	ns	Figure 87	-	-	150
Read data hold time		tDHR	ns	Figure 87	5	-	-

16.7 80-system Bus Interface Timing Characteristics (9/8-bit I/F)

Table 83 Normal Write function

IOVcc = 1.65V ~ 3.3V, Vci= 2.4V ~ 3.3V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure 87	70	-	-
	Read	tCYCR	ns	Figure 87	450	-	-
Write low-level pulse width		PWLW	ns	Figure 87	50	-	-
Read low-level pulse width		PWLR	ns	Figure 87	170	-	-
Write high-level pulse width		PWHW	ns	Figure 87	25	-	-
Read high-level pulse width		PWHR	ns	Figure 87	250	-	-
Write/Read rise/fall time		tWRr, WRf	ns	Figure 87	-	-	25
Setup time	Write (RS~CSN, WRN)	tAS	ns	Figure 87	0	-	-
	Read (RS~CSN, RDN)				10		
Address hold time		tAH	ns	Figure 87	2	-	-
Write data setup time		tDSW	ns	Figure 87	25	-	-
Write data hold time		tHWR	ns	Figure 87	10	-	-
Read data delay time		tDDR	ns	Figure 87	-	-	150
Read data hold time		tDHR	ns	Figure 87	5	-	-

16.8 Serial interface Timing Characteristics

16.8.1 Table 84 IOVcc = 1.65V ~ 3.3V, Vci = 2.4V ~ 3.3V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	tSCYC	ns	Figure 88	100	-	20,000
	Read (transmitted)	tSCYC	ns	Figure 88	350	-	20,000
Serial clock high-level pulse width	Write (received)	tSCH	ns	Figure 88	40	-	-
	Read (transmitted)	tSCH	ns	Figure 88	150	-	-
Serial clock low-level pulse width	Write (received)	tSCL	ns	Figure 88	40	-	-
	Read (transmitted)	tSCL	ns	Figure 88	150	-	-
Serial clock rise/fall time		tSCr, tSCf	ns	Figure 88	-	-	20
Chip select setup time		tCSU	ns	Figure 88	20	-	-
Chip select hold time		tCH	ns	Figure 88	60	-	-
Serial input data setup time		tSISU	ns	Figure 88	30	-	-
Serial input data hold time		tSIH	ns	Figure 88	30	-	-
Serial output data delay time		tSOD	ns	Figure 88	-	-	130
Serial output data hold time		tSOH	ns	Figure 88	5	-	-

16.9 Reset Timing Characteristics

16.9.1 Table 85 IOVcc = 1.65V ~ 3.3V, Vci= 2.4V ~ 3.3V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Resetlow-levelwidth	tRES	ms	Figure89	1	—	—
Resetrisetime	trRES	μs	Figure89	—	—	10

16.10 LCD driver output Characteristics

Table 88

Item	Symbol	Unit	Test condition	Min	Typ	Max	Note
Source Driver output delay time	tdds	μs	Vci=IOVcc =3.0V, DDVDH=5.5V, VREG1OUT=5.0V, fosc=358kHz (320 lines), Ta=25°C REV=0, SAP=010, AP=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 Load resistance R=10kΩ, Load capacitance C=20pF Time to reach the target voltage level ±35mV from the timing of Vcom polarity inversion Transition from the same grayscale level at all source pins	—	17	—	10
VCOM output delay time	tddv	μs	Vci=IOVcc =3.0V, DDVDH=5.5V, VREG1OUT=5.0V, fosc =358kHz (320 lines), Ta=25°C REV=0, SAP=010, AP=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 Load resistance R=100Ω, Load capacitance C=20pF Time to reach the target voltage level ±35mV from the timing of Vcom polarity inversion Transition from the same grayscale level at all source pins	—	17	—	11

Table 89 Display test

Item	Symbol	Unit	TestCondition	Min.	Typ.	Max.	Notes
LCD power supply current Partial 32-Line Display Load 2.8” Panel White pattern	Ipartial1	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010,	—	3.7	—	
LCD power supply current Partial 32-Line Display Load 2.8” Panel Black Pattern	Ipartial2	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010,	—	4.5	—	
LCD power supply current Partial 32-Line Display Load 2.8” Panel Snow Pattern	Ipartial3	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010,	—	4.2	—	
LCD power supply current 8-color mode Load 2.8” Panel Black pattern	Ipartial1	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010, R91=0300, R98=0103	—	7	—	
LCD power supply current Normal Display Load 2.8” Panel Black Pattern	Ipartial2	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010, R91=0300, R98=0103	—	10	—	

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following figures illustrate the configurations of input, I/O, and output pins.

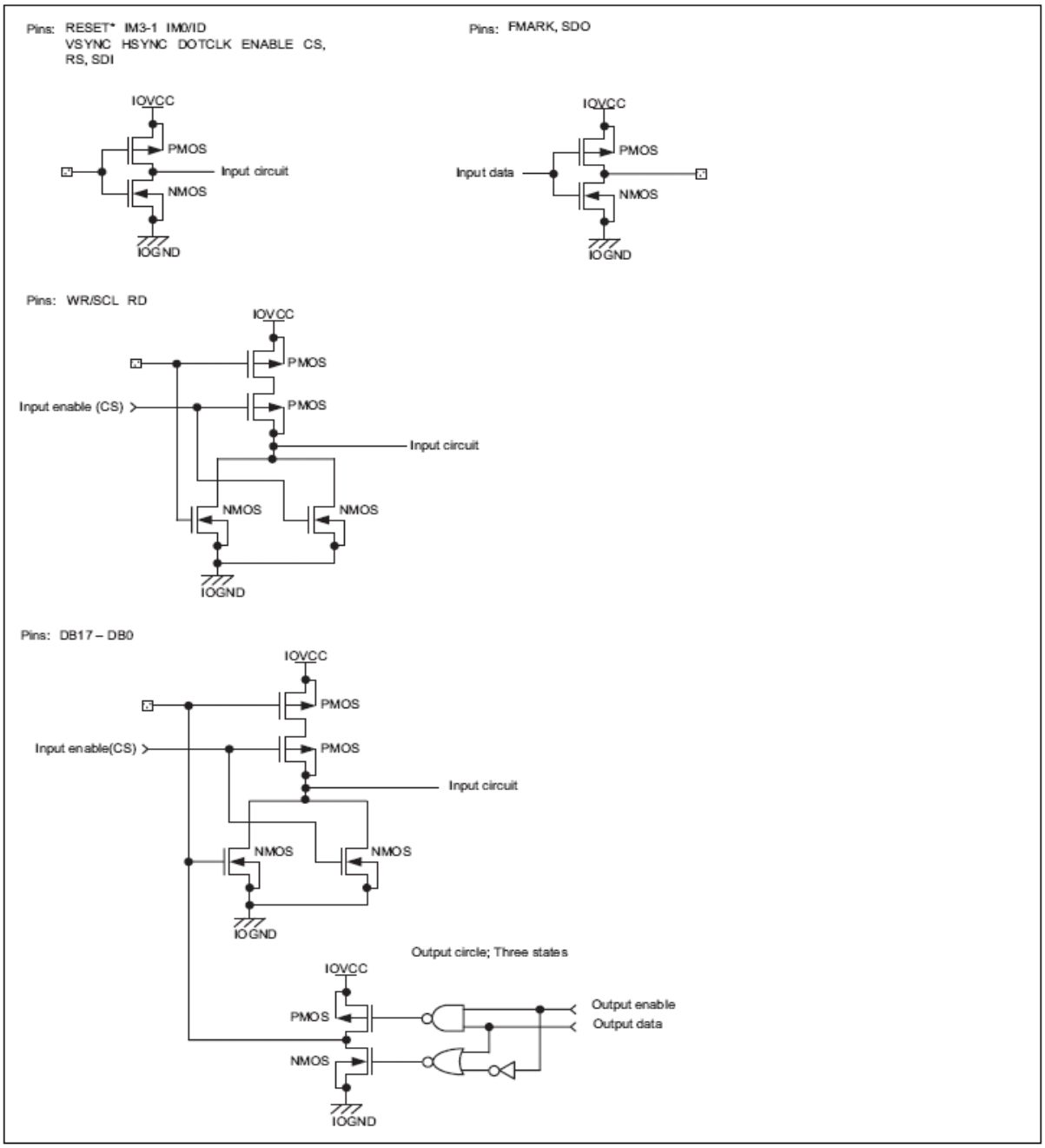


Figure 79

3. The TEST1, TEST2 pins must be grounded (GND). The IM3/2/1 and IM0/ID pins must be fixed at either IOVcc or GND.
4. This excludes the current in the output-drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a

middle range level. The current consumption is unaffected by whether the CSN pin is "High" or "Low" while not accessing via interface pins.

6. The relationship between voltages and the current consumption is as follows.

T.B.D.

Figure 80

7. The output voltage deviation is the difference in the voltages from adjacent source pins for the same display data. This value is shown just for reference.
8. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for each chip with same display data.
9. This applies to internal oscillators when using external oscillation resistor Rf.

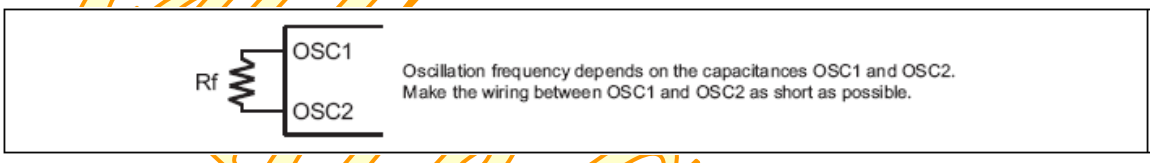


Figure 81

10. Just for reference. The wiring resistance when the FT1505C is mounted on the glass substrate is not taken into consideration. No load is applied on pins except those for measurement. See the reference data "Load current characteristics (T.B.D.)".
11. Just for reference. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality of display on the actual panel in use.
12. Just for reference. The "DDVDH-VREGOUT≥0.5V" should be mostly followed in normal case, but the actual DDVDH will be a little lower than idea DDVDH due to different loading pattern, so it may be little loose sometimes, meanwhile that "DDVDH-VREG1OUT>0.3V" should be always followed in all actual case.

T.B.D.

Figure 82

Test Circuits

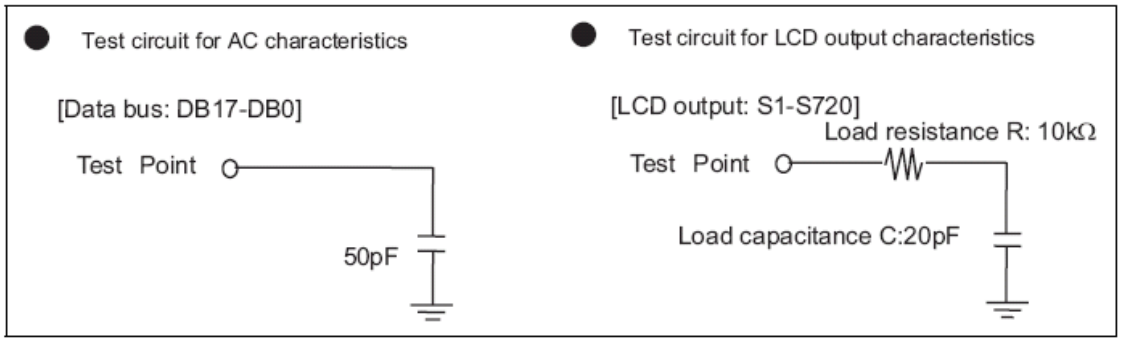


Figure 83

16.11 Timing Characteristics 80-system Bus Interface

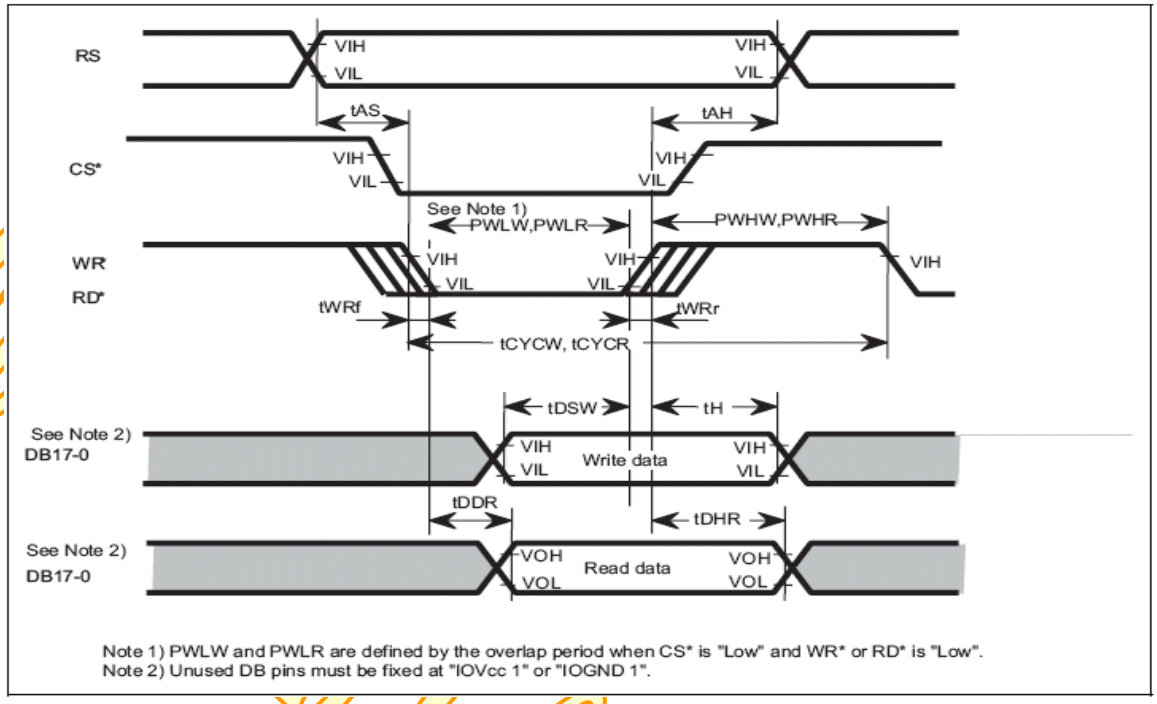


Figure 84

16.12 Clock synchronous serial interface

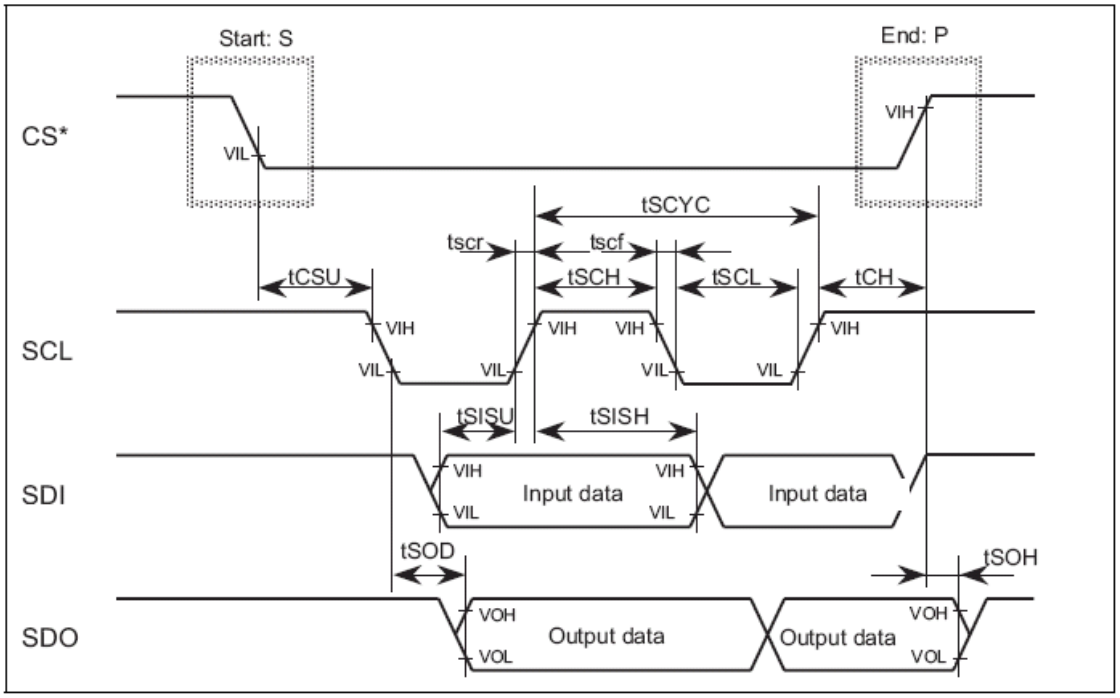


Figure 85

16.13 Reset operation

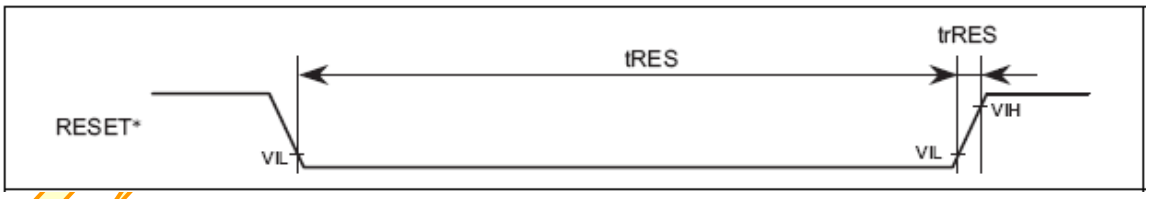


Figure 86

16.14 External display interface

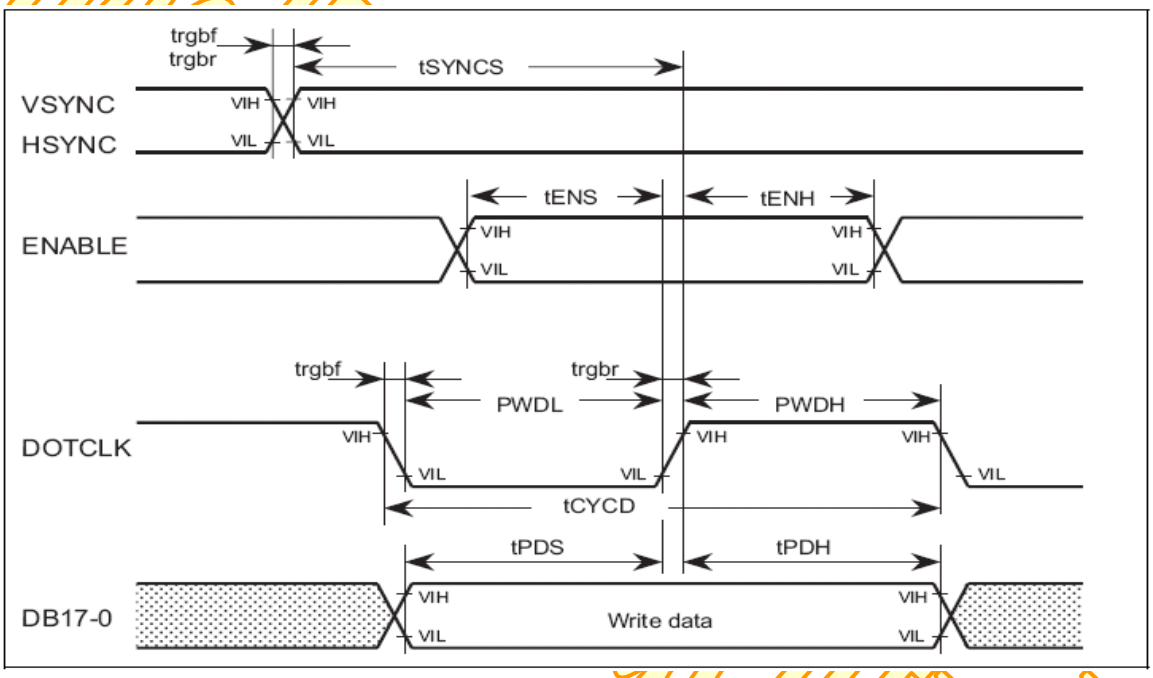


Figure 87

LCD driver outputs

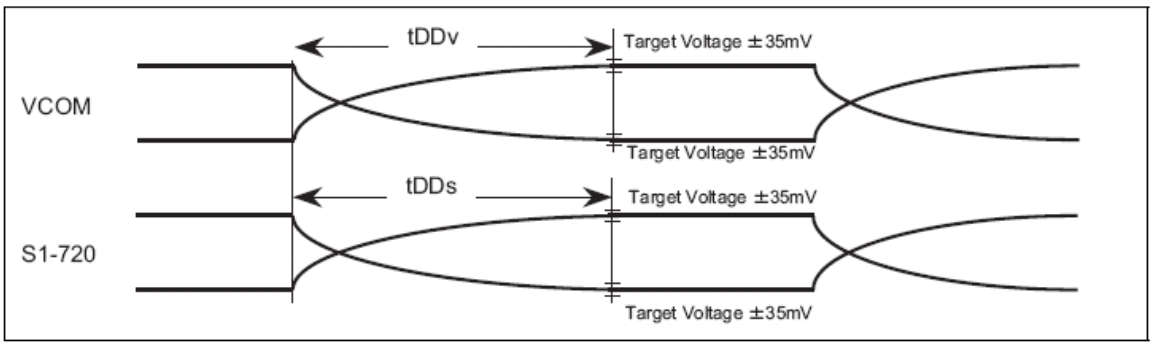


Figure 88

** May be revised without notice

REVISION TABLE

version	Revisions	Date
0.5	Page 48: Change Table 36 VDV[4:0]. Page 47: Change VRH[3..0] setting Page 45: Change Table 30 AP[2:0] The above is the difference comparing with FT1505C A version.	2008-08-01
1.0	Re-organize the table of content Add RGB interface on page 56~64 Add Resize function on page 110~113 Display interface Control 1 (R0Ch) on page 75 Correct description of R98 on page 95	2008-11-25
2.0	Correct Table 36 on page 82	2009-01-08

END OF DATABOOK