Product Datasheet

Version: 0.70
Date: 8-Oct-08

FT1509

a-Si TFT LCD Single Chip Driver
240RGBX432 Resolution and 262K Color

FocalTech Systems Co., Ltd
support@focaltech-systems.com

Index

Description

FT1509 is a single-chip 262k-color TFT LCD panel driver IC with built-in 233,280 bytes RAM, a 720-channel source driver, a 432-channel gate driver, and power supply circuit capable of supporting WQVGA (240RGBx432-dot) resolution display.

The dithering image processing is implemented in the FT1509 to provide 262K-color display quality and the Multi-domain Vertical Alignment (MVA) wide view angle display is also supported in the FT1509.

For efficient data transfer, the FT1509 supports 4 kinds of system interfaces which are i80-system MPU interface via 8-/9-/16-/18-bit bus, VSYNC interface (system interface + VSYNC, internal clock, DB17-DB0), serial data transfer interface (SPI), and RGB 6-/16-/18-bit interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-DB0).

In VSYNC interface modes, the combined use of widow address function enable displaying a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to display the refresh data only to minimize the amount of data transfer and the total power consumption.

FT1509 can operate at low voltage up to 1.65V I/O interface voltage, and an internal voltage follower circuit to generate voltage levels for driving LCD panel. The FT1509 also supports different power management functions (through software control) such as **CABC**—Content adaptive Backlight Control, 8-color display mode, sleep mode, standby mode, and deep standby mode to make the FT1509 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, PDA and PMP where long battery life is a major concern.

Features

- Single chip controller driver for 240RGB x 432-dot a-Si TFT LCD display supporting true 262K-color
- Dithering image processing improvement to support 16.7M-color display quality
- Supporting MVA (Multi-domain Vertical Alignment) wide view display
- **CABC: Content Adaptive Backlight Control**
- Sharpness enhancement mode
- No MDDI support, but the interface pins will be reserved for future use
- Display sharpness enhancement
- Incorporate 720-channel source driver and 432-channel gate driver
- Internal 233,280 bytes graphic RAM
- System interfaces
  - i80 system interface via 8-/ 9-/16-/18-bit bus
  - Serial Peripheral Interface (SPI)
  - Endian free interface, enabling switching endian by software
- Moving picture display interface
  - RGB interface (VSYNC, HSYNC,DOTCLK,ENABLE,DB17~0) via 6-,16-,18-bit bus
  - VSYNC interface (System interface + VSYNC)
  - FMARK interface (System interface + FMARK)
- High speed GRAM burst write function
- Internal oscillator and hardware reset
- Resizing function (×1/2, ×1/4)
- Reversible source/gate driver shift direction
- Window address function to specify a rectangular area for internal GRAM access
- Abundant color display and drawing functions
  - γ-correction function enabling display in 262,144 colors
  - 1 line-unit vertical scrolling function
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- N-line-inversion liquid crystal drive to invert polarity of liquid crystal at an interval of arbitrary number of line period (N=0~127)
- Internal NVM (OTP): User identification code (4 bits), Vcom level adjustment (12 bits)
- a-TFT LCD storage capacitor: Cst only
- Power saving functions
  - 8-color display mode: close source local buffer
  - Sleep mode: Oscillator and Regulator are on, other modules are off
  - Standby mode: Regulator is on, other modules are off.
  - Deep standby mode: All modules are off.
- Input power supply voltages:
  - Vcc = 2.5v ~ 3.3v (Logic regulator power supply)
  - IOVcc1=1.65v~3.3v (Interface I/O power supply)
  - Vci = 2.5v ~ 3.3v (Liquid crystal analog circuit power supply)
  - Vdd= 1.65v~1.75v (Digital circuit power supply)
- LCD driver output voltage:
  - Source/VCOM power supply voltage

- DDVDH - GND = 4.5v ~ 6.0v
- VCL – GND = -2.5v ~ -3.3v
- Vci – VCL ≦ 6.0v

■ Gate driver output voltage
- VGH - AGND = 10.0v ~ 20.0v
- VGL – AGND = -5.0v ~ -15.0v
- VGH – VGL ≦ 28.0v

■ VCOM driver (VCOM power supply)
- VcomH = 3.0v ~ (DDVDH-0.5)v (3v ~ 5v)
- VcomL = (VCL+0.5)v ~ 0v (-2.5v ~ 0v)
- VcomH – VcomL ≦ 6.0v

Table 1 FT1509 power supply main specifications

No.	Item		FT1509
1	TFT data lines		720 output
2	TFT gate lines		432 output
3	TFT display storage capacitor		Cst only (Common Vcom formula)
4	Liquid crystal drive output	S1~S720	V0 ~ V63 grayscales
		G1~G432	VGH-VGL
		Vcom	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML
5	Input voltage	IOVcc (interface power)	1.65v ~ 3.30v Power supply to IM0/ID, IM1-3, RESET, DB17-DB0, RDN, SDI, SDO, WR/SCL, RS, CSN, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK Connect to Vci on the FPC when IOVcc and Vci are at the same electrical potential.
		Vci (liquid crystal drive power)	2.40v ~ 3.30v Connect to IOVcc on the FPC when IOVcc and Vci are at the same electrical potential.
6	Regulated voltage	VDD	1.7v
7	Internal step-up circuits	DDVDH	Vci1 x 2
		VGH	Vci1 x 6, x 5, x 4
		VGL	Vci1 x -3, x -4, x -5
		VCL	Vci1 x -1

Block Diagram

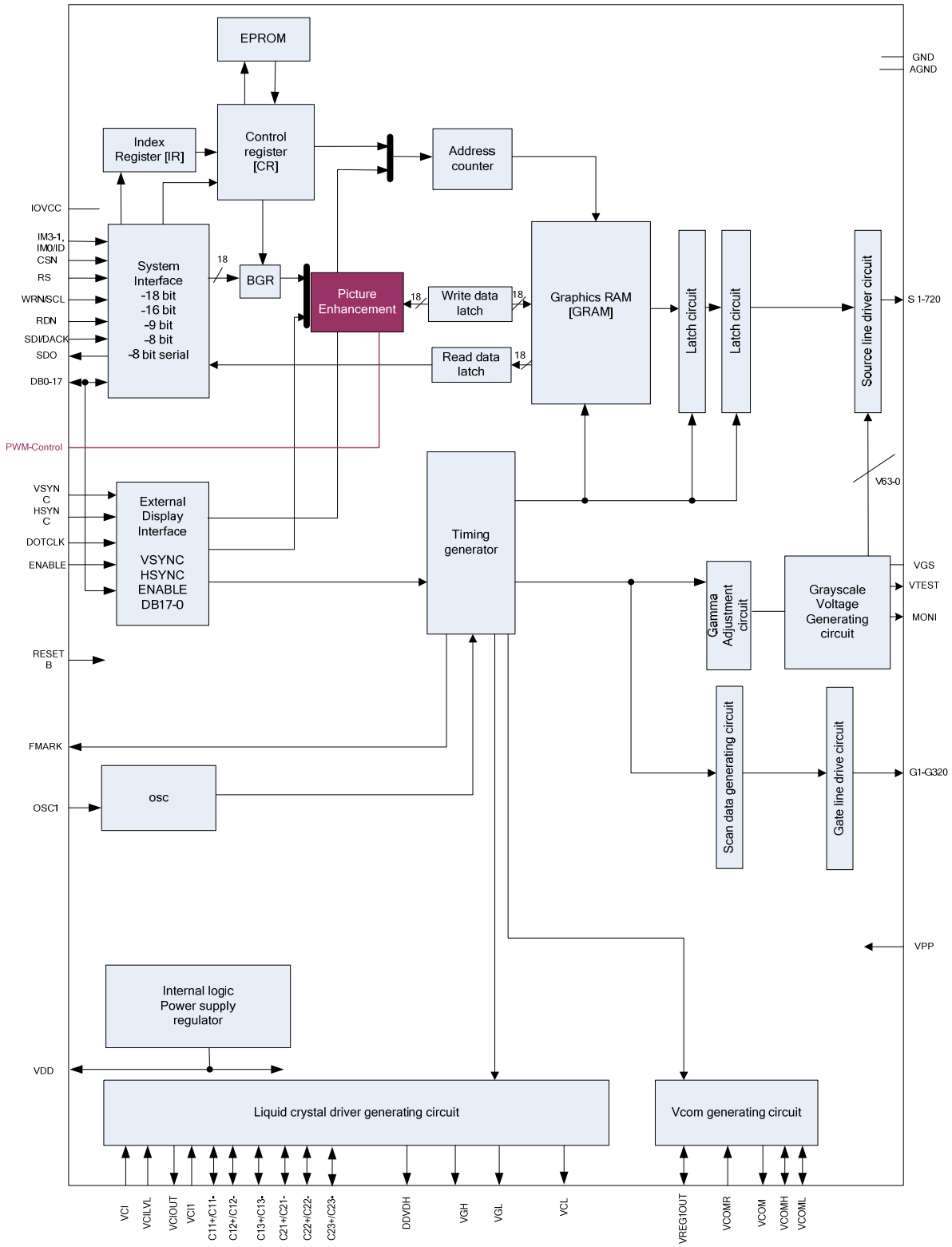


Figure 1

Pin Function

Table 2 Interface

<table>
<tr><th>Signal</th><th>NUM</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM2～ IM0/ID</td><td>4</td><td>I</td><td>GND or IOVcc</td><td>Selects MPU interface format. Amplitude: IOVcc-GND.
When selecting clock synchronous serial interface, IM0 pin is used to set the device code ID.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU interface format</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80system 18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80-system 9-bit interface.</td><td>DB17-DB9</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-DB10,DB[8:1]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Clock synchronous serial interface (SPI)</td><td>SDI/SDO</td></tr>
<tr><td>1</td><td>0</td><td>ID</td><td>Setting disabled</td><td>–</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>–</td></tr>
</table>
Note1: 65,536 colors in 1 transfer, 262,144 colors in 2 transfer
Note2: 65,536 colors in 2 transfer, 262,144 colors in 3 transfer</td><td>All pins can't be floating.</td></tr>
<tr><td>CSN</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVcc-GND
Low: the FT1509 is selected and accessible
High: the FT1509 is not selected and not accessible.</td><td>IOVcc</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVcc-GND
Low: select Index or status register
High: select control register</td><td>IOVcc</td></tr>
<tr><td>WRN/SCL</td><td>1</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WRN is low.
Synchronous clock signal (SCL) in serial interface operation.
Amplitude: IOVcc-GND</td><td>IOVcc</td></tr>
<tr><td>RDN</td><td>1</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RDN is low.
Amplitude: IOVcc-GND</td><td>IOVcc</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal.
Amplitude: IOVcc-GND</td><td>GND or IOVcc</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal.
Amplitude: IOVcc-GND</td><td>OPEN</td></tr>
</table>

Table 3 Interface (continued)

Signal	NUM	I/O	Connect to	Function	When not in use
DB0-DB17	18	I/O	MPU	Parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVcc-GND). Fix unused pins to either IOVcc or GND level. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. RGB interface: 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-DB1 are used. 18-bit I/F: DB17-DB0 are used.	GND or IOVcc
ENABLE	1	I	MPU	Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	GND or IOVcc
VSYNC	1	I	MPU	Frame synchronous signal . Low active. (Amplitude: IOVcc-GND).	GND or IOVcc
HSYNC	1	I	MPU	Line synchronous signal. Low active. (Amplitude: IOVcc-GND).	GND or IOVcc
DOTCLK	1	I	MPU	Dot clock signal. The data is inputted on the rising edge of DOTCLK. (Amplitude: IOVcc-GND).	GND or IOVcc
FMARK	1	O	MPU	Frame head pulse to synchronize RAM data writes operation with the frame head position. (Amplitude: IOVcc-GND).	Open
ledon	1	O	LED Driver	Control LED lighting or not	Open
ledpwm	1	O	LED Driver	Backlight control signal by PWM	Open

Table 4 Reset and oscillator

Signal	NUM	I/O	Connect to	Function	When not in use
RESETB	1	I	MPU or external RC circuit	Reset signal Initializes the FT1509 when RESET input is low. Make sure to execute a power-on reset when turning on the power supply. (Amplitude: IOVcc-GND).	-
OSC1	1	I	Oscillator	Allow external clock input	Open

Table 5 Power supply

Signal	NUM	I/O	Connect to	Function	When not in use
Vcc	1	-	Power supply	Power supply to internal logic regulator circuit: Vcc = 2.5V~3.3V. Vcc ≥ IOVcc	-
GND	1	-	Power supply	GND of Internal logic and GRAM. GND of interface pins: RESETB; CSN; WR; RDN; RS; DB17-DB0; VSYNC; HSYNC; DOTCLK; ENABLE. GND = 0v	-
VDD	1	O	Stabilizing capacitor	Internal regulator output used for logic and GRAM power supply. Connect a stabilizing capacitor.	-
IOVcc	1	-	Power supply	Power supply to interface pins: RESETB; CSN; WR; RDN; RS; DB17-DB0; VSYNC; HSYNC; DOTCLK; ENABLE. IOVcc = 1.65v ~ 3.3v.	-
VciLVL	1	I	Reference power supply	VciLVL and Vci must be at the same electrical potential. Connect VciLVL to an external power supply of 2.5V ~ 3.3V. In case of COG, connect to Vci on the FPC to prevent noise.	-
AGND	1	-	Power supply	Analog GND (for liquid crystal power supply circuit): AGND = 0v. In case of COG, connect to GND on the FPC to prevent noise.	-
Vci	1	I	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.4v ~ 3.3v.	-

Table 6 Step-up circuit

Signal	NUM	I/O	Connect to	Function	When not in use
Vci1	1	I/O	**Normal mode**: Stabilizing Capacitor **Fixed mode**: Directly connected Vci	**Normal mode:** Reference voltage for step-up circuit 1. Vci1 must be set for the output voltages DDVDH, VGH, VGL to be generated within the respective setting ranges. See Page 118 --**Strongly recommended mode.** **Fixed mode:** Directly connected Vci. In this case, the Vciout adjustment circuit is not available. (Please be careful register VC[2:0] setting to avoid conflict. –See Page 47 .It's potential negative factor for picture quality) but the efficiency of the step-up operation can be enhanced. More detail Circuit see page 119	-
VCL	1	O	Stabilizing capacitor	Power Supply for VCOML drive, internally generated	-
DDVDH	1	O	Stabilizing capacitor	Source driver unit liquid crystal drive voltage and Vcom drive power supply. DDVDH is generated from Vci1 in the step-up circuit 1. The step-up factor is set by instruction (BT). DDVDH = 4.5v ~ 6.0v	-
VGH	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2. The step-up factor is set by instruction (BT). VGH = max. 20.0v	-
VGL	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2. The step-up factor is set by instruction (BT). VGL = max. -15.0V	-
C11A, C11B C12A, C12B	5	I/O	Step-up capacitor	Capacitor connection pins of the step-up circuit 1.	-
C13A, C13B	4	I/O	Step-up capacitor	Capacitor connection pins of the step-up circuit 3.	-
C21A, C21B C22A, C22B	7	I/O	Step-up capacitor	Capacitor connection pins of the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.	-

Table 7 Liquid crystal drive

Signal	Number	I/O	Connect to	Function	When not in use
VREG1OUT	1	O	Stabilizing capacitor	VREG1OUT is generated from Vci, and the output level is set by instruction (VRH) and used for (1) source driver grayscale reference voltage, (2) VcomH level reference voltage, (3) Vcom amplitude reference voltage (4) liquid crystal drive electrical potential in 8-color display mode. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 2.4v ~ (DDVDH – 0.5)v	Open
Vcom	1	O	TFT common electrode	Power supply to TFT common electrode. Vcom voltage is defined by VcomH and VcomL. The alternating cycle can be changed by setting register. Also Vcom output can be controlled by instruction (COM).	Open
VcomH	1	O	Stabilizing capacitor	The high level of Vcom which can be changed by either internal electric volume or connecting variable resistor (VcomR)	Open
VcomL	1	O	Stabilizing capacitor	The low level of Vcom. Connect to a stabilizing capacitor	Open
VcomR	1	I	Variable resistor or open	Connect a variable resistor between VREG1OUT and GND when adjusting the VcomH level externally.	Open
VGS	1	I	GND or external resistor	Reference level of grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor	-
S1 ~ S720	720	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S720.	Open
G1 ~ G432	432	O	LCD	Gate output signal Gate select level: VGH Gate non-select level: VGL	Open

Table 8 test and dummy

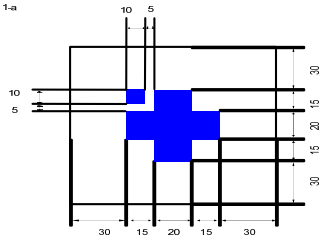
Signal	Number	I/O	Connect to	Function	When not in use
PTEST1 - 2	2	O	-	Test pin. Leave it open.	Open
TESTM1 - 3	3	I	GND	Test pin.	GND or Open
TS0-9	10	O	-	Test pin. Leave it open.	Open
OSC_TEST	1	-	-	Test pin. Leave them open.	Open
DUMMY14 - 15	2	-	-	Dummy pads. Available for measuring the COG contact	Open

				resistance. Dummy14 and Dummy15 are short-circuited within the chip.	
DUMMY1 - 13 DUMMY16 - 25	23	-	-	Dummy pads. Leave them open.	Open

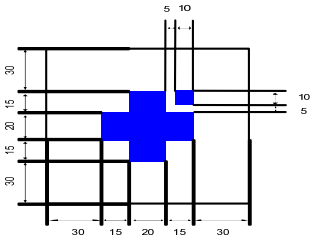
.Chip Size：21.544 mm X 0.91 mm
.Chip Thickness: 300um (typ.)
.Pad Coordinate: Pad Center
.Coordinate Origin: chip center
.Au BUMP size:
(1) 50 um * 80 um
Input / Output
(No.1 ~ No.299)
(2) 18 um * 110 um
Staggered LCD output side
(No. 300 ~ No. 1467)

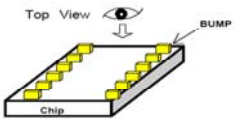
Alignment Mark:

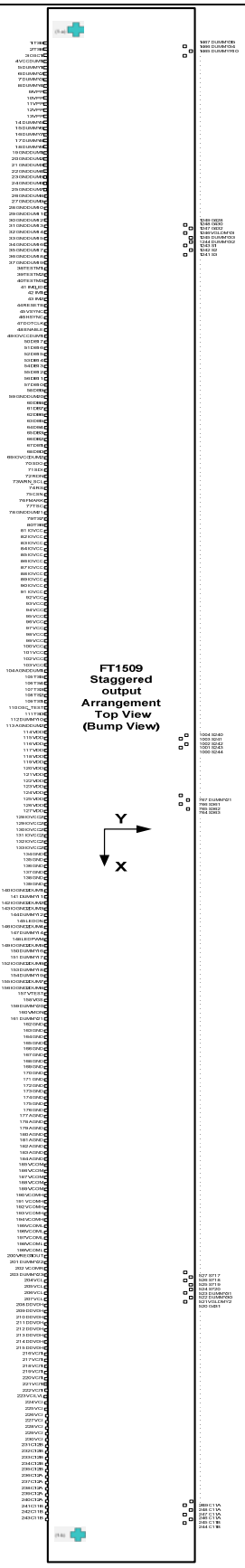
1-a



1-b







FT1509 PAD coordinates 1 (Unit: μm)

PAD NO.	PAD NAME	X	Y
1	TS9	-10430	-359
2	TS8	-10360	-359
3	OSC1	-10290	-359
4	VCCDUM1	-10220	-359
5	DUMMY1	-10150	-359
6	DUMMY2	-10080	-359
7	DUMMY3	-10010	-359
8	DUMMY4	-9940	-359
9	VPP	-9870	-359
10	VPP	-9800	-359
11	VPP	-9730	-359
12	VPP	-9660	-359
13	VPP	-9590	-359
14	DUMMY5	-9520	-359
15	DUMMY6	-9450	-359
16	DUMMY7	-9380	-359
17	DUMMY8	-9310	-359
18	DUMMY9	-9240	-359
19	GNDDUM1	-9170	-359
20	GNDDUM2	-9100	-359
21	GNDDUM3	-9030	-359
22	GNDDUM4	-8960	-359
23	GNDDUM5	-8890	-359
24	GNDDUM6	-8820	-359
25	GNDDUM7	-8750	-359
26	GNDDUM8	-8680	-359
27	GNDDUM9	-8610	-359
28	GNDDUM10	-8540	-359
29	GNDDUM11	-8470	-359
30	GNDDUM12	-8400	-359
31	GNDDUM13	-8330	-359
32	GNDDUM14	-8260	-359
33	GNDDUM15	-8190	-359
34	GNDDUM16	-8120	-359
35	GNDDUM17	-8050	-359
36	GNDDUM18	-7980	-359
37	GNDDUM19	-7910	-359
38	TESTM1	-7840	-359
39	TESTM2	-7770	-359
40	TESTM3	-7700	-359
41	IM0_ID	-7630	-359
42	IM1	-7560	-359
43	IM2	-7490	-359
44	RESETB	-7420	-359
45	VSYNC	-7350	-359
46	HSYNC	-7280	-359
47	DOTCLK	-7210	-359
48	ENABLE	-7140	-359
49	IOVCCDUM1	-7070	-359
50	DB17	-7000	-359

PAD NO.	PAD NAME	X	Y
51	DB16	-6930	-359
52	DB15	-6860	-359
53	DB14	-6790	-359
54	DB13	-6720	-359
55	DB12	-6650	-359
56	DB11	-6580	-359
57	DB10	-6510	-359
58	DB9	-6440	-359
59	GNDDUM20	-6370	-359
60	DB8	-6300	-359
61	DB7	-6230	-359
62	DB6	-6160	-359
63	DB5	-6090	-359
64	DB4	-6020	-359
65	DB3	-5950	-359
66	DB2	-5880	-359
67	DB1	-5810	-359
68	DB0	-5740	-359
69	IOVCCDUM2	-5670	-359
70	SDO	-5600	-359
71	SDI	-5530	-359
72	RDN	-5460	-359
73	WRN_SCL	-5390	-359
74	RS	-5320	-359
75	CSN	-5250	-359
76	FMARK	-5180	-359
77	TSC	-5110	-359
78	GNDDUM21	-5040	-359
79	TS7	-4970	-359
80	TS6	-4900	-359
81	IOVCC	-4830	-359
82	IOVCC	-4760	-359
83	IOVCC	-4690	-359
84	IOVCC	-4620	-359
85	IOVCC	-4550	-359
86	IOVCC	-4480	-359
87	IOVCC	-4410	-359
88	IOVCC	-4340	-359
89	IOVCC	-4270	-359
90	IOVCC	-4200	-359
91	IOVCC	-4130	-359
92	VCC	-4060	-359
93	VCC	-3990	-359
94	VCC	-3920	-359
95	VCC	-3850	-359
96	VCC	-3780	-359
97	VCC	-3710	-359
98	VCC	-3640	-359
99	VCC	-3570	-359
100	VCC	-3500	-359

FT1509 PAD coordinates 2 (Unit: μm)

PAD NO.	PAD NAME	X	Y
101	VCC	-3430	-359
102	VCC	-3360	-359
103	VCC	-3290	-359
104	AGNDDUM1	-3220	-359
105	TS5	-3150	-359
106	TS4	-3080	-359
107	TS3	-3010	-359
108	TS2	-2940	-359
109	TS1	-2870	-359
110	OSC_TEST	-2800	-359
111	TS0	-2730	-359
112	DUMMY10	-2660	-359
113	AGNDDUM2	-2590	-359
114	VDD	-2520	-359
115	VDD	-2450	-359
116	VDD	-2380	-359
117	VDD	-2310	-359
118	VDD	-2240	-359
119	VDD	-2170	-359
120	VDD	-2100	-359
121	VDD	-2030	-359
122	VDD	-1960	-359
123	VDD	-1890	-359
124	VDD	-1820	-359
125	VDD	-1750	-359
126	VDD	-1680	-359
127	VDD	-1610	-359
128	IOVCC2	-1540	-359
129	IOVCC2	-1470	-359
130	IOVCC2	-1400	-359
131	IOVCC2	-1330	-359
132	IOVCC2	-1260	-359
133	IOVCC2	-1190	-359
134	GND	-1120	-359
135	GND	-1050	-359
136	GND	-980	-359
137	GND	-910	-359
138	GND	-840	-359
139	GND	-770	-359
140	IOGND2DUM1	-700	-359
141	DUMMY11	-630	-359
142	IOGND2DUM2	-560	-359
143	IOGND2DUM3	-490	-359
144	DUMMY12	-420	-359
145	LEDON	-350	-359
146	IOGND2DUM4	-280	-359
147	DUMMY14	-210	-359
148	LEDPWM	-140	-359
149	IOGND2DUM5	-70	-359
150	DUMMY16	0	-359

PAD NO.	PAD NAME	X	Y
151	DUMMY17	70	-359
152	IOGND2DUM6	140	-359
153	DUMMY18	210	-359
154	DUMMY19	280	-359
155	IOGND2DUM7	350	-359
156	IOGND2DUM8	420	-359
157	VTEST	490	-359
158	VGS	560	-359
159	DUMMY20	630	-359
160	VMON	700	-359
161	DUMMY21	770	-359
162	GND	840	-359
163	GND	910	-359
164	GND	980	-359
165	GND	1050	-359
166	GND	1120	-359
167	GND	1190	-359
168	GND	1260	-359
169	GND	1330	-359
170	GND	1400	-359
171	GND	1470	-359
172	GND	1540	-359
173	GND	1610	-359
174	GND	1680	-359
175	GND	1750	-359
176	GND	1820	-359
177	AGND	1890	-359
178	AGND	1960	-359
179	AGND	2030	-359
180	AGND	2100	-359
181	AGND	2170	-359
182	AGND	2240	-359
183	AGND	2310	-359
184	AGND	2380	-359
185	VCOM	2450	-359
186	VCOM	2520	-359
187	VCOM	2590	-359
188	VCOM	2660	-359
189	VCOM	2730	-359
190	VCOMH	2800	-359
191	VCOMH	2870	-359
192	VCOMH	2940	-359
193	VCOMH	3010	-359
194	VCOMH	3080	-359
195	VCOML	3150	-359
196	VCOML	3220	-359
197	VCOML	3290	-359
198	VCOML	3360	-359
199	VCOML	3430	-359
200	VREG1OUT	3500	-359

FT1509 PAD coordinates 3 (Unit: μm)

PAD NO.	PAD NAME	X	Y
201	DUMMY22	3570	-359
202	VCOMR	3640	-359
203	DUMMY23	3710	-359
204	VCL	3780	-359
205	VCL	3850	-359
206	VCL	3920	-359
207	VCL	3990	-359
208	DDVDH	4060	-359
209	DDVDH	4130	-359
210	DDVDH	4200	-359
211	DDVDH	4270	-359
212	DDVDH	4340	-359
213	DDVDH	4410	-359
214	DDVDH	4480	-359
215	DDVDH	4550	-359
216	VCI1	4620	-359
217	VCI1	4690	-359
218	VCI1	4760	-359
219	VCI1	4830	-359
220	VCI1	4900	-359
221	VCI1	4970	-359
222	VCI1	5040	-359
223	VCILVL	5110	-359
224	VCI	5180	-359
225	VCI	5250	-359
226	VCI	5320	-359
227	VCI	5390	-359
228	VCI	5460	-359
229	VCI	5530	-359
230	VCI	5600	-359
231	C12B	5670	-359
232	C12B	5740	-359
233	C12B	5810	-359
234	C12B	5880	-359
235	C12B	5950	-359
236	C12A	6020	-359
237	C12A	6090	-359
238	C12A	6160	-359
239	C12A	6230	-359
240	C12A	6300	-359
241	C11B	6370	-359
242	C11B	6440	-359
243	C11B	6510	-359
244	C11B	6580	-359
245	C11B	6650	-359
246	C11A	6720	-359
247	C11A	6790	-359
248	C11A	6860	-359
249	C11A	6930	-359
250	C11A	7000	-359

PAD NO.	PAD NAME	X	Y
251	AGNDDUM3	7070	-359
252	VGL	7140	-359
253	VGL	7210	-359
254	VGL	7280	-359
255	VGL	7350	-359
256	VGL	7420	-359
257	VGL	7490	-359
258	VGL	7560	-359
259	VGL	7630	-359
260	VGL	7700	-359
261	VGL	7770	-359
262	AGNDDUM4	7840	-359
263	AGNDDUM5	7910	-359
264	VGH	7980	-359
265	VGH	8050	-359
266	VGH	8120	-359
267	VGH	8190	-359
268	VGH	8260	-359
269	VGH	8330	-359
270	DUMMY24	8400	-359
271	C13B	8470	-359
272	C13B	8540	-359
273	C13B	8610	-359
274	DUMMY25	8680	-359
275	C13A	8750	-359
276	C13A	8820	-359
277	C13A	8890	-359
278	DUMMY26	8960	-359
279	C21B	9030	-359
280	C21B	9100	-359
281	C21B	9170	-359
282	C21A	9240	-359
283	C21A	9310	-359
284	C21A	9380	-359
285	C22B	9450	-359
286	C22B	9520	-359
287	C22B	9590	-359
288	C22A	9660	-359
289	C22A	9730	-359
290	C22A	9800	-359
291	C23B	9870	-359
292	C23B	9940	-359
293	C23B	10010	-359
294	C23A	10080	-359
295	C23A	10150	-359
296	C23A	10220	-359
297	DUMMY27	10290	-359
298	DUMMYR5	10360	-359
299	DUMMYR6	10430	-359
300	DUMMY28	10647	340

FT1509 PAD coordinates 4 (Unit: μm)

PAD NO.	PAD NAME	X	Y
301	DUMMY29	10629	205
302	DUMMYR7	10611	340
303	DUMMYR8	10593	205
304	VGLDMY1	10575	340
305	G1	10557	205
306	G3	10539	340
307	G5	10521	205
308	G7	10503	340
309	G9	10485	205
310	G11	10467	340
311	G13	10449	205
312	G15	10431	340
313	G17	10413	205
314	G19	10395	340
315	G21	10377	205
316	G23	10359	340
317	G25	10341	205
318	G27	10323	340
319	G29	10305	205
320	G31	10287	340
321	G33	10269	205
322	G35	10251	340
323	G37	10233	205
324	G39	10215	340
325	G41	10197	205
326	G43	10179	340
327	G45	10161	205
328	G47	10143	340
329	G49	10125	205
330	G51	10107	340
331	G53	10089	205
332	G55	10071	340
333	G57	10053	205
334	G59	10035	340
335	G61	10017	205
336	G63	9999	340
337	G65	9981	205
338	G67	9963	340
339	G69	9945	205
340	G71	9927	340
341	G73	9909	205
342	G75	9891	340
343	G77	9873	205
344	G79	9855	340
345	G81	9837	205
346	G83	9819	340
347	G85	9801	205
348	G87	9783	340
349	G89	9765	205
350	G91	9747	340

PAD NO.	PAD NAME	X	Y
351	G93	9729	205
352	G95	9711	340
353	G97	9693	205
354	G99	9675	340
355	G101	9657	205
356	G103	9639	340
357	G105	9621	205
358	G107	9603	340
359	G109	9585	205
360	G111	9567	340
361	G113	9549	205
362	G115	9531	340
363	G117	9513	205
364	G119	9495	340
365	G121	9477	205
366	G123	9459	340
367	G125	9441	205
368	G127	9423	340
369	G129	9405	205
370	G131	9387	340
371	G133	9369	205
372	G135	9351	340
373	G137	9333	205
374	G139	9315	340
375	G141	9297	205
376	G143	9279	340
377	G145	9261	205
378	G147	9243	340
379	G149	9225	205
380	G151	9207	340
381	G153	9189	205
382	G155	9171	340
383	G157	9153	205
384	G159	9135	340
385	G161	9117	205
386	G163	9099	340
387	G165	9081	205
388	G167	9063	340
389	G169	9045	205
390	G171	9027	340
391	G173	9009	205
392	G175	8991	340
393	G177	8973	205
394	G179	8955	340
395	G181	8937	205
396	G183	8919	340
397	G185	8901	205
398	G187	8883	340
399	G189	8865	205
400	G191	8847	340

FT1509 PAD coordinates 5 (Unit: μm)

PAD NO.	PAD NAME	X	Y
401	G193	8829	205
402	G195	8811	340
403	G197	8793	205
404	G199	8775	340
405	G201	8757	205
406	G203	8739	340
407	G205	8721	205
408	G207	8703	340
409	G209	8685	205
410	G211	8667	340
411	G213	8649	205
412	G215	8631	340
413	G217	8613	205
414	G219	8595	340
415	G221	8577	205
416	G223	8559	340
417	G225	8541	205
418	G227	8523	340
419	G229	8505	205
420	G231	8487	340
421	G233	8469	205
422	G235	8451	340
423	G237	8433	205
424	G239	8415	340
425	G241	8397	205
426	G243	8379	340
427	G245	8361	205
428	G247	8343	340
429	G249	8325	205
430	G251	8307	340
431	G253	8289	205
432	G255	8271	340
433	G257	8253	205
434	G259	8235	340
435	G261	8217	205
436	G263	8199	340
437	G265	8181	205
438	G267	8163	340
439	G269	8145	205
440	G271	8127	340
441	G273	8109	205
442	G275	8091	340
443	G277	8073	205
444	G279	8055	340
445	G281	8037	205
446	G283	8019	340
447	G285	8001	205
448	G287	7983	340
449	G289	7965	205
450	G291	7947	340

PAD NO.	PAD NAME	X	Y
451	G293	7929	205
452	G295	7911	340
453	G297	7893	205
454	G299	7875	340
455	G301	7857	205
456	G303	7839	340
457	G305	7821	205
458	G307	7803	340
459	G309	7785	205
460	G311	7767	340
461	G313	7749	205
462	G315	7731	340
463	G317	7713	205
464	G319	7695	340
465	G321	7677	205
466	G323	7659	340
467	G325	7641	205
468	G327	7623	340
469	G329	7605	205
470	G331	7587	340
471	G333	7569	205
472	G335	7551	340
473	G337	7533	205
474	G339	7515	340
475	G341	7497	205
476	G343	7479	340
477	G345	7461	205
478	G347	7443	340
479	G349	7425	205
480	G351	7407	340
481	G353	7389	205
482	G355	7371	340
483	G357	7353	205
484	G359	7335	340
485	G361	7317	205
486	G363	7299	340
487	G365	7281	205
488	G367	7263	340
489	G369	7245	205
490	G371	7227	340
491	G373	7209	205
492	G375	7191	340
493	G377	7173	205
494	G379	7155	340
495	G381	7137	205
496	G383	7119	340
497	G385	7101	205
498	G387	7083	340
499	G389	7065	205
500	G391	7047	340

FT1509 PAD coordinates 6 (Unit: μm)

PAD NO.	PAD NAME	X	Y
501	G393	7029	205
502	G395	7011	340
503	G397	6993	205
504	G399	6975	340
505	G401	6957	205
506	G403	6939	340
507	G405	6921	205
508	G407	6903	340
509	G409	6885	205
510	G411	6867	340
511	G413	6849	205
512	G415	6831	340
513	G417	6813	205
514	G419	6795	340
515	G421	6777	205
516	G423	6759	340
517	G425	6741	205
518	G427	6723	340
519	G429	6705	205
520	G431	6687	340
521	VGLDMY2	6669	205
522	DUMMY30	6651	340
523	DUMMY31	6417	340
524	S720	6399	205
525	S719	6381	340
526	S718	6363	205
527	S717	6345	340
528	S716	6327	205
529	S715	6309	340
530	S714	6291	205
531	S713	6273	340
532	S712	6255	205
533	S711	6237	340
534	S710	6219	205
535	S709	6201	340
536	S708	6183	205
537	S707	6165	340
538	S706	6147	205
539	S705	6129	340
540	S704	6111	205
541	S703	6093	340
542	S702	6075	205
543	S701	6057	340
544	S700	6039	205
545	S699	6021	340
546	S698	6003	205
547	S697	5985	340
548	S696	5967	205
549	S695	5949	340
550	S694	5931	205

PAD NO.	PAD NAME	X	Y
551	S693	5913	340
552	S692	5895	205
553	S691	5877	340
554	S690	5859	205
555	S689	5841	340
556	S688	5823	205
557	S687	5805	340
558	S686	5787	205
559	S685	5769	340
560	S684	5751	205
561	S683	5733	340
562	S682	5715	205
563	S681	5697	340
564	S680	5679	205
565	S679	5661	340
566	S678	5643	205
567	S677	5625	340
568	S676	5607	205
569	S675	5589	340
570	S674	5571	205
571	S673	5553	340
572	S672	5535	205
573	S671	5517	340
574	S670	5499	205
575	S669	5481	340
576	S668	5463	205
577	S667	5445	340
578	S666	5427	205
579	S665	5409	340
580	S664	5391	205
581	S663	5373	340
582	S662	5355	205
583	S661	5337	340
584	S660	5319	205
585	S659	5301	340
586	S658	5283	205
587	S657	5265	340
588	S656	5247	205
589	S655	5229	340
590	S654	5211	205
591	S653	5193	340
592	S652	5175	205
593	S651	5157	340
594	S650	5139	205
595	S649	5121	340
596	S648	5103	205
597	S647	5085	340
598	S646	5067	205
599	S645	5049	340
600	S644	5031	205

FT1509 PAD coordinates 7 (Unit: μm)

PAD NO.	PAD NAME	X	Y
601	S643	5013	340
602	S642	4995	205
603	S641	4977	340
604	S640	4959	205
605	S639	4941	340
606	S638	4923	205
607	S637	4905	340
608	S636	4887	205
609	S635	4869	340
610	S634	4851	205
611	S633	4833	340
612	S632	4815	205
613	S631	4797	340
614	S630	4779	205
615	S629	4761	340
616	S628	4743	205
617	S627	4725	340
618	S626	4707	205
619	S625	4689	340
620	S624	4671	205
621	S623	4653	340
622	S622	4635	205
623	S621	4617	340
624	S620	4599	205
625	S619	4581	340
626	S618	4563	205
627	S617	4545	340
628	S616	4527	205
629	S615	4509	340
630	S614	4491	205
631	S613	4473	340
632	S612	4455	205
633	S611	4437	340
634	S610	4419	205
635	S609	4401	340
636	S608	4383	205
637	S607	4365	340
638	S606	4347	205
639	S605	4329	340
640	S604	4311	205
641	S603	4293	340
642	S602	4275	205
643	S601	4257	340
644	S600	4239	205
645	S599	4221	340
646	S598	4203	205
647	S597	4185	340
648	S596	4167	205
649	S595	4149	340
650	S594	4131	205

PAD NO.	PAD NAME	X	Y
651	S593	4113	340
652	S592	4095	205
653	S591	4077	340
654	S590	4059	205
655	S589	4041	340
656	S588	4023	205
657	S587	4005	340
658	S586	3987	205
659	S585	3969	340
660	S584	3951	205
661	S583	3933	340
662	S582	3915	205
663	S581	3897	340
664	S580	3879	205
665	S579	3861	340
666	S578	3843	205
667	S577	3825	340
668	S576	3807	205
669	S575	3789	340
670	S574	3771	205
671	S573	3753	340
672	S572	3735	205
673	S571	3717	340
674	S570	3699	205
675	S569	3681	340
676	S568	3663	205
677	S567	3645	340
678	S566	3627	205
679	S565	3609	340
680	S564	3591	205
681	S563	3573	340
682	S562	3555	205
683	S561	3537	340
684	S560	3519	205
685	S559	3501	340
686	S558	3483	205
687	S557	3465	340
688	S556	3447	205
689	S555	3429	340
690	S554	3411	205
691	S553	3393	340
692	S552	3375	205
693	S551	3357	340
694	S550	3339	205
695	S549	3321	340
696	S548	3303	205
697	S547	3285	340
698	S546	3267	205
699	S545	3249	340
700	S544	3231	205

FT1509 PAD coordinates 8 (Unit: μm)

PAD NO.	PAD NAME	X	Y
701	S543	3213	340
702	S542	3195	205
703	S541	3177	340
704	S540	3159	205
705	S539	3141	340
706	S538	3123	205
707	S537	3105	340
708	S536	3087	205
709	S535	3069	340
710	S534	3051	205
711	S533	3033	340
712	S532	3015	205
713	S531	2997	340
714	S530	2979	205
715	S529	2961	340
716	S528	2943	205
717	S527	2925	340
718	S526	2907	205
719	S525	2889	340
720	S524	2871	205
721	S523	2853	340
722	S522	2835	205
723	S521	2817	340
724	S520	2799	205
725	S519	2781	340
726	S518	2763	205
727	S517	2745	340
728	S516	2727	205
729	S515	2709	340
730	S514	2691	205
731	S513	2673	340
732	S512	2655	205
733	S511	2637	340
734	S510	2619	205
735	S509	2601	340
736	S508	2583	205
737	S507	2565	340
738	S506	2547	205
739	S505	2529	340
740	S504	2511	205
741	S503	2493	340
742	S502	2475	205
743	S501	2457	340
744	S500	2439	205
745	S499	2421	340
746	S498	2403	205
747	S497	2385	340
748	S496	2367	205
749	S495	2349	340
750	S494	2331	205

PAD NO.	PAD NAME	X	Y
751	S493	2313	340
752	S492	2295	205
753	S491	2277	340
754	S490	2259	205
755	S489	2241	340
756	S488	2223	205
757	S487	2205	340
758	S486	2187	205
759	S485	2169	340
760	S484	2151	205
761	S483	2133	340
762	S482	2115	205
763	S481	2097	340
764	S480	2079	205
765	S479	2061	340
766	S478	2043	205
767	S477	2025	340
768	S476	2007	205
769	S475	1989	340
770	S474	1971	205
771	S473	1953	340
772	S472	1935	205
773	S471	1917	340
774	S470	1899	205
775	S469	1881	340
776	S468	1863	205
777	S467	1845	340
778	S466	1827	205
779	S465	1809	340
780	S464	1791	205
781	S463	1773	340
782	S462	1755	205
783	S461	1737	340
784	S460	1719	205
785	S459	1701	340
786	S458	1683	205
787	S457	1665	340
788	S456	1647	205
789	S455	1629	340
790	S454	1611	205
791	S453	1593	340
792	S452	1575	205
793	S451	1557	340
794	S450	1539	205
795	S449	1521	340
796	S448	1503	205
797	S447	1485	340
798	S446	1467	205
799	S445	1449	340
800	S444	1431	205

FT1509 PAD coordinates 9 (Unit: μm)

PAD NO.	PAD NAME	X	Y
801	S443	1413	340
802	S442	1395	205
803	S441	1377	340
804	S440	1359	205
805	S439	1341	340
806	S438	1323	205
807	S437	1305	340
808	S436	1287	205
809	S435	1269	340
810	S434	1251	205
811	S433	1233	340
812	S432	1215	205
813	S431	1197	340
814	S430	1179	205
815	S429	1161	340
816	S428	1143	205
817	S427	1125	340
818	S426	1107	205
819	S425	1089	340
820	S424	1071	205
821	S423	1053	340
822	S422	1035	205
823	S421	1017	340
824	S420	999	205
825	S419	981	340
826	S418	963	205
827	S417	945	340
828	S416	927	205
829	S415	909	340
830	S414	891	205
831	S413	873	340
832	S412	855	205
833	S411	837	340
834	S410	819	205
835	S409	801	340
836	S408	783	205
837	S407	765	340
838	S406	747	205
839	S405	729	340
840	S404	711	205
841	S403	693	340
842	S402	675	205
843	S401	657	340
844	S400	639	205
845	S399	621	340
846	S398	603	205
847	S397	585	340
848	S396	567	205
849	S395	549	340
850	S394	531	205

PAD NO.	PAD NAME	X	Y
851	S393	513	340
852	S392	495	205
853	S391	477	340
854	S390	459	205
855	S389	441	340
856	S388	423	205
857	S387	405	340
858	S386	387	205
859	S385	369	340
860	S384	351	205
861	S383	333	340
862	S382	315	205
863	S381	297	340
864	S380	279	205
865	S379	261	340
866	S378	243	205
867	S377	225	340
868	S376	207	205
869	S375	189	340
870	S374	171	205
871	S373	153	340
872	S372	135	205
873	S371	117	340
874	S370	99	205
875	S369	81	340
876	S368	63	205
877	S367	45	340
878	S366	27	205
879	S365	9	340
880	S364	-9	205
881	S363	-27	340
882	S362	-45	205
883	S361	-63	340
884	S360	-81	205
885	S359	-99	340
886	S358	-117	205
887	S357	-135	340
888	S356	-153	205
889	S355	-171	340
890	S354	-189	205
891	S353	-207	340
892	S352	-225	205
893	S351	-243	340
894	S350	-261	205
895	S349	-279	340
896	S348	-297	205
897	S347	-315	340
898	S346	-333	205
899	S345	-351	340
900	S344	-369	205

FT1509 PAD coordinates 10 (Unit: μm)

PAD NO.	PAD NAME	X	Y
901	S343	-387	340
902	S342	-405	205
903	S341	-423	340
904	S340	-441	205
905	S339	-459	340
906	S338	-477	205
907	S337	-495	340
908	S336	-513	205
909	S335	-531	340
910	S334	-549	205
911	S333	-567	340
912	S332	-585	205
913	S331	-603	340
914	S330	-621	205
915	S329	-639	340
916	S328	-657	205
917	S327	-675	340
918	S326	-693	205
919	S325	-711	340
920	S324	-729	205
921	S323	-747	340
922	S322	-765	205
923	S321	-783	340
924	S320	-801	205
925	S319	-819	340
926	S318	-837	205
927	S317	-855	340
928	S316	-873	205
929	S315	-891	340
930	S314	-909	205
931	S313	-927	340
932	S312	-945	205
933	S311	-963	340
934	S310	-981	205
935	S309	-999	340
936	S308	-1017	205
937	S307	-1035	340
938	S306	-1053	205
939	S305	-1071	340
940	S304	-1089	205
941	S303	-1107	340
942	S302	-1125	205
943	S301	-1143	340
944	S300	-1161	205
945	S299	-1179	340
946	S298	-1197	205
947	S297	-1215	340
948	S296	-1233	205
949	S295	-1251	340
950	S294	-1269	205

PAD NO.	PAD NAME	X	Y
951	S293	-1287	340
952	S292	-1305	205
953	S291	-1323	340
954	S290	-1341	205
955	S289	-1359	340
956	S288	-1377	205
957	S287	-1395	340
958	S286	-1413	205
959	S285	-1431	340
960	S284	-1449	205
961	S283	-1467	340
962	S282	-1485	205
963	S281	-1503	340
964	S280	-1521	205
965	S279	-1539	340
966	S278	-1557	205
967	S277	-1575	340
968	S276	-1593	205
969	S275	-1611	340
970	S274	-1629	205
971	S273	-1647	340
972	S272	-1665	205
973	S271	-1683	340
974	S270	-1701	205
975	S269	-1719	340
976	S268	-1737	205
977	S267	-1755	340
978	S266	-1773	205
979	S265	-1791	340
980	S264	-1809	205
981	S263	-1827	340
982	S262	-1845	205
983	S261	-1863	340
984	S260	-1881	205
985	S259	-1899	340
986	S258	-1917	205
987	S257	-1935	340
988	S256	-1953	205
989	S255	-1971	340
990	S254	-1989	205
991	S253	-2007	340
992	S252	-2025	205
993	S251	-2043	340
994	S250	-2061	205
995	S249	-2079	340
996	S248	-2097	205
997	S247	-2115	340
998	S246	-2133	205
999	S245	-2151	340
1000	S244	-2169	205

FT1509 PAD coordinates 11 (Unit: μm)

PAD NO.	PAD NAME	X	Y
1001	S243	-2187	340
1002	S242	-2205	205
1003	S241	-2223	340
1004	S240	-2241	205
1005	S239	-2259	340
1006	S238	-2277	205
1007	S237	-2295	340
1008	S236	-2313	205
1009	S235	-2331	340
1010	S234	-2349	205
1011	S233	-2367	340
1012	S232	-2385	205
1013	S231	-2403	340
1014	S230	-2421	205
1015	S229	-2439	340
1016	S228	-2457	205
1017	S227	-2475	340
1018	S226	-2493	205
1019	S225	-2511	340
1020	S224	-2529	205
1021	S223	-2547	340
1022	S222	-2565	205
1023	S221	-2583	340
1024	S220	-2601	205
1025	S219	-2619	340
1026	S218	-2637	205
1027	S217	-2655	340
1028	S216	-2673	205
1029	S215	-2691	340
1030	S214	-2709	205
1031	S213	-2727	340
1032	S212	-2745	205
1033	S211	-2763	340
1034	S210	-2781	205
1035	S209	-2799	340
1036	S208	-2817	205
1037	S207	-2835	340
1038	S206	-2853	205
1039	S205	-2871	340
1040	S204	-2889	205
1041	S203	-2907	340
1042	S202	-2925	205
1043	S201	-2943	340
1044	S200	-2961	205
1045	S199	-2979	340
1046	S198	-2997	205
1047	S197	-3015	340
1048	S196	-3033	205
1049	S195	-3051	340
1050	S194	-3069	205

PAD NO.	PAD NAME	X	Y
1051	S193	-3087	340
1052	S192	-3105	205
1053	S191	-3123	340
1054	S190	-3141	205
1055	S189	-3159	340
1056	S188	-3177	205
1057	S187	-3195	340
1058	S186	-3213	205
1059	S185	-3231	340
1060	S184	-3249	205
1061	S183	-3267	340
1062	S182	-3285	205
1063	S181	-3303	340
1064	S180	-3321	205
1065	S179	-3339	340
1066	S178	-3357	205
1067	S177	-3375	340
1068	S176	-3393	205
1069	S175	-3411	340
1070	S174	-3429	205
1071	S173	-3447	340
1072	S172	-3465	205
1073	S171	-3483	340
1074	S170	-3501	205
1075	S169	-3519	340
1076	S168	-3537	205
1077	S167	-3555	340
1078	S166	-3573	205
1079	S165	-3591	340
1080	S164	-3609	205
1081	S163	-3627	340
1082	S162	-3645	205
1083	S161	-3663	340
1084	S160	-3681	205
1085	S159	-3699	340
1086	S158	-3717	205
1087	S157	-3735	340
1088	S156	-3753	205
1089	S155	-3771	340
1090	S154	-3789	205
1091	S153	-3807	340
1092	S152	-3825	205
1093	S151	-3843	340
1094	S150	-3861	205
1095	S149	-3879	340
1096	S148	-3897	205
1097	S147	-3915	340
1098	S146	-3933	205
1099	S145	-3951	340
1100	S144	-3969	205

FT1509 PAD coordinates 12 (Unit: μm)

PAD NO.	PAD NAME	X	Y
1101	S143	-3987	340
1102	S142	-4005	205
1103	S141	-4023	340
1104	S140	-4041	205
1105	S139	-4059	340
1106	S138	-4077	205
1107	S137	-4095	340
1108	S136	-4113	205
1109	S135	-4131	340
1110	S134	-4149	205
1111	S133	-4167	340
1112	S132	-4185	205
1113	S131	-4203	340
1114	S130	-4221	205
1115	S129	-4239	340
1116	S128	-4257	205
1117	S127	-4275	340
1118	S126	-4293	205
1119	S125	-4311	340
1120	S124	-4329	205
1121	S123	-4347	340
1122	S122	-4365	205
1123	S121	-4383	340
1124	S120	-4401	205
1125	S119	-4419	340
1126	S118	-4437	205
1127	S117	-4455	340
1128	S116	-4473	205
1129	S115	-4491	340
1130	S114	-4509	205
1131	S113	-4527	340
1132	S112	-4545	205
1133	S111	-4563	340
1134	S110	-4581	205
1135	S109	-4599	340
1136	S108	-4617	205
1137	S107	-4635	340
1138	S106	-4653	205
1139	S105	-4671	340
1140	S104	-4689	205
1141	S103	-4707	340
1142	S102	-4725	205
1143	S101	-4743	340
1144	S100	-4761	205
1145	S99	-4779	340
1146	S98	-4797	205
1147	S97	-4815	340
1148	S96	-4833	205
1149	S95	-4851	340
1150	S94	-4869	205

PAD NO.	PAD NAME	X	Y
1151	S93	-4887	340
1152	S92	-4905	205
1153	S91	-4923	340
1154	S90	-4941	205
1155	S89	-4959	340
1156	S88	-4977	205
1157	S87	-4995	340
1158	S86	-5013	205
1159	S85	-5031	340
1160	S84	-5049	205
1161	S83	-5067	340
1162	S82	-5085	205
1163	S81	-5103	340
1164	S80	-5121	205
1165	S79	-5139	340
1166	S78	-5157	205
1167	S77	-5175	340
1168	S76	-5193	205
1169	S75	-5211	340
1170	S74	-5229	205
1171	S73	-5247	340
1172	S72	-5265	205
1173	S71	-5283	340
1174	S70	-5301	205
1175	S69	-5319	340
1176	S68	-5337	205
1177	S67	-5355	340
1178	S66	-5373	205
1179	S65	-5391	340
1180	S64	-5409	205
1181	S63	-5427	340
1182	S62	-5445	205
1183	S61	-5463	340
1184	S60	-5481	205
1185	S59	-5499	340
1186	S58	-5517	205
1187	S57	-5535	340
1188	S56	-5553	205
1189	S55	-5571	340
1190	S54	-5589	205
1191	S53	-5607	340
1192	S52	-5625	205
1193	S51	-5643	340
1194	S50	-5661	205
1195	S49	-5679	340
1196	S48	-5697	205
1197	S47	-5715	340
1198	S46	-5733	205
1199	S45	-5751	340
1200	S44	-5769	205

FT1509 PAD coordinates 13 (Unit: μm)

PAD NO.	PAD NAME	X	Y
1201	S43	-5787	340
1202	S42	-5805	205
1203	S41	-5823	340
1204	S40	-5841	205
1205	S39	-5859	340
1206	S38	-5877	205
1207	S37	-5895	340
1208	S36	-5913	205
1209	S35	-5931	340
1210	S34	-5949	205
1211	S33	-5967	340
1212	S32	-5985	205
1213	S31	-6003	340
1214	S30	-6021	205
1215	S29	-6039	340
1216	S28	-6057	205
1217	S27	-6075	340
1218	S26	-6093	205
1219	S25	-6111	340
1220	S24	-6129	205
1221	S23	-6147	340
1222	S22	-6165	205
1223	S21	-6183	340
1224	S20	-6201	205
1225	S19	-6219	340
1226	S18	-6237	205
1227	S17	-6255	340
1228	S16	-6273	205
1229	S15	-6291	340
1230	S14	-6309	205
1231	S13	-6327	340
1232	S12	-6345	205
1233	S11	-6363	340
1234	S10	-6381	205
1235	S9	-6399	340
1236	S8	-6417	205
1237	S7	-6435	340
1238	S6	-6453	205
1239	S5	-6471	340
1240	S4	-6489	205
1241	S3	-6507	340
1242	S2	-6525	205
1243	S1	-6543	340
1244	DUMMY32	-6561	205
1245	DUMMY33	-6651	340
1246	VGLDMY3	-6669	205
1247	G432	-6687	340
1248	G430	-6705	205
1249	G428	-6723	340
1250	G426	-6741	205

PAD NO.	PAD NAME	X	Y
1251	G424	-6759	340
1252	G422	-6777	205
1253	G420	-6795	340
1254	G418	-6813	205
1255	G416	-6831	340
1256	G414	-6849	205
1257	G412	-6867	340
1258	G410	-6885	205
1259	G408	-6903	340
1260	G406	-6921	205
1261	G404	-6939	340
1262	G402	-6957	205
1263	G400	-6975	340
1264	G398	-6993	205
1265	G396	-7011	340
1266	G394	-7029	205
1267	G392	-7047	340
1268	G390	-7065	205
1269	G388	-7083	340
1270	G386	-7101	205
1271	G384	-7119	340
1272	G382	-7137	205
1273	G380	-7155	340
1274	G378	-7173	205
1275	G376	-7191	340
1276	G374	-7209	205
1277	G372	-7227	340
1278	G370	-7245	205
1279	G368	-7263	340
1280	G366	-7281	205
1281	G364	-7299	340
1282	G362	-7317	205
1283	G360	-7335	340
1284	G358	-7353	205
1285	G356	-7371	340
1286	G354	-7389	205
1287	G352	-7407	340
1288	G350	-7425	205
1289	G348	-7443	340
1290	G346	-7461	205
1291	G344	-7479	340
1292	G342	-7497	205
1293	G340	-7515	340
1294	G338	-7533	205
1295	G336	-7551	340
1296	G334	-7569	205
1297	G332	-7587	340
1298	G330	-7605	205
1299	G328	-7623	340
1300	G326	-7641	205

FT1509 PAD coordinates 14 (Unit: μm)

PAD NO.	PAD NAME	X	Y
1301	G324	-7659	340
1302	G322	-7677	205
1303	G320	-7695	340
1304	G318	-7713	205
1305	G316	-7731	340
1306	G314	-7749	205
1307	G312	-7767	340
1308	G310	-7785	205
1309	G308	-7803	340
1310	G306	-7821	205
1311	G304	-7839	340
1312	G302	-7857	205
1313	G300	-7875	340
1314	G298	-7893	205
1315	G296	-7911	340
1316	G294	-7929	205
1317	G292	-7947	340
1318	G290	-7965	205
1319	G288	-7983	340
1320	G286	-8001	205
1321	G284	-8019	340
1322	G282	-8037	205
1323	G280	-8055	340
1324	G278	-8073	205
1325	G276	-8091	340
1326	G274	-8109	205
1327	G272	-8127	340
1328	G270	-8145	205
1329	G268	-8163	340
1330	G266	-8181	205
1331	G264	-8199	340
1332	G262	-8217	205
1333	G260	-8235	340
1334	G258	-8253	205
1335	G256	-8271	340
1336	G254	-8289	205
1337	G252	-8307	340
1338	G250	-8325	205
1339	G248	-8343	340
1340	G246	-8361	205
1341	G244	-8379	340
1342	G242	-8397	205
1343	G240	-8415	340
1344	G238	-8433	205
1345	G236	-8451	340
1346	G234	-8469	205
1347	G232	-8487	340
1348	G230	-8505	205
1349	G228	-8523	340
1350	G226	-8541	205

PAD NO.	PAD NAME	X	Y
1351	G224	-8559	340
1352	G222	-8577	205
1353	G220	-8595	340
1354	G218	-8613	205
1355	G216	-8631	340
1356	G214	-8649	205
1357	G212	-8667	340
1358	G210	-8685	205
1359	G208	-8703	340
1360	G206	-8721	205
1361	G204	-8739	340
1362	G202	-8757	205
1363	G200	-8775	340
1364	G198	-8793	205
1365	G196	-8811	340
1366	G194	-8829	205
1367	G192	-8847	340
1368	G190	-8865	205
1369	G188	-8883	340
1370	G186	-8901	205
1371	G184	-8919	340
1372	G182	-8937	205
1373	G180	-8955	340
1374	G178	-8973	205
1375	G176	-8991	340
1376	G174	-9009	205
1377	G172	-9027	340
1378	G170	-9045	205
1379	G168	-9063	340
1380	G166	-9081	205
1381	G164	-9099	340
1382	G162	-9117	205
1383	G160	-9135	340
1384	G158	-9153	205
1385	G156	-9171	340
1386	G154	-9189	205
1387	G152	-9207	340
1388	G150	-9225	205
1389	G148	-9243	340
1390	G146	-9261	205
1391	G144	-9279	340
1392	G142	-9297	205
1393	G140	-9315	340
1394	G138	-9333	205
1395	G136	-9351	340
1396	G134	-9369	205
1397	G132	-9387	340
1398	G130	-9405	205
1399	G128	-9423	340
1400	G126	-9441	205

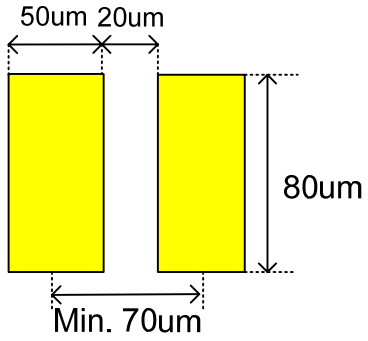
FT1509 PAD coordinates 15 (Unit: μm)

PAD NO.	PAD NAME	X	Y
1401	G124	-9459	340
1402	G122	-9477	205
1403	G120	-9495	340
1404	G118	-9513	205
1405	G116	-9531	340
1406	G114	-9549	205
1407	G112	-9567	340
1408	G110	-9585	205
1409	G108	-9603	340
1410	G106	-9621	205
1411	G104	-9639	340
1412	G102	-9657	205
1413	G100	-9675	340
1414	G98	-9693	205
1415	G96	-9711	340
1416	G94	-9729	205
1417	G92	-9747	340
1418	G90	-9765	205
1419	G88	-9783	340
1420	G86	-9801	205
1421	G84	-9819	340
1422	G82	-9837	205
1423	G80	-9855	340
1424	G78	-9873	205
1425	G76	-9891	340
1426	G74	-9909	205
1427	G72	-9927	340
1428	G70	-9945	205
1429	G68	-9963	340
1430	G66	-9981	205
1431	G64	-9999	340
1432	G62	-10017	205
1433	G60	-10035	340
1434	G58	-10053	205
1435	G56	-10071	340
1436	G54	-10089	205
1437	G52	-10107	340
1438	G50	-10125	205
1439	G48	-10143	340
1440	G46	-10161	205
1441	G44	-10179	340
1442	G42	-10197	205
1443	G40	-10215	340
1444	G38	-10233	205
1445	G36	-10251	340
1446	G34	-10269	205
1447	G32	-10287	340
1448	G30	-10305	205
1449	G28	-10323	340
1450	G26	-10341	205

PAD NO.	PAD NAME	X	Y
1451	G24	-10359	340
1452	G22	-10377	205
1453	G20	-10395	340
1454	G18	-10413	205
1455	G16	-10431	340
1456	G14	-10449	205
1457	G12	-10467	340
1458	G10	-10485	205
1459	G8	-10503	340
1460	G6	-10521	205
1461	G4	-10539	340
1462	G2	-10557	205
1463	VGLDMY4	-10575	340
1464	DUMMYR9	-10593	205
1465	DUMMYR10	-10611	340
1466	DUMMY34	-10629	205
1467	DUMMY35	-10647	340
Alignment Marks			
1-a	Left	-10655	-333
1-b	Right	10655	-333

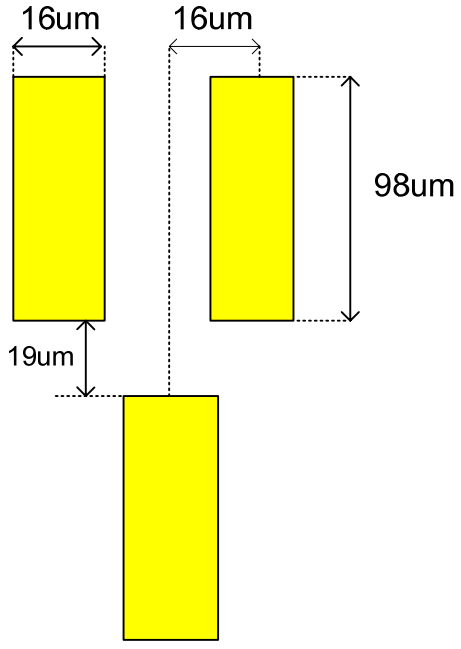
Bump Arrangement

(1) I/O pin (No. 1 ~ No. 243)



BUMP area:4000um^2

S1 ~ S720
G1 ~ G320
DUMMY
DUMMYR
(No. 244 ~ No. 1291)



BUMP area:1568 um^2

Figure 3

Block Function

1. System Interface

The FT1509 supports the following system interfaces: 80-system high-speed interface via 8-, 9-, 16-, 18-bit bus and clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The FT1509 has 16-bit index register (IR), 18-bit write-data register (WDR), and 18-bit read-data register (RDR). The IR is the register to store index information from control register and the internal GRAM. The WDR is the register to temporarily store the data to be written to the internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via the RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the FT1509 performs the first read operation from the internal GRAM. Valid data is read out when the FT1509 performs the second and subsequent read operations.

The instruction execution time except starting oscillation takes 0 clock cycle and instructions can be written consecutively.

Table 9 Register Selection (80-system 8/9/16/18-bit bus Interface)

WRN	RDN	RS	Function
0	1	0	Write index to IR
1	0	0	Read internal status
0	1	1	Write to control register/internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 10 Register Selection (clock synchronous serial interface - SPI)

Start byte

R/W	RS	Function
0	0	Write index to IR
1	0	Read internal status
0	1	Write to control register/internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

2. External Display Interface (VSYNC interfaces)

The FT1509 supports VSYNC interface as the moving picture display interface (external display interface). In VSYNC interface operation, the display operation is synchronized with the internal clock and VSYNC signal, which is used for frame synchronization. The display data is written to the internal GRAM via system interface but there are restrictions in setting the speed and the method to write data to the internal RAM. For details, see the “External Display Interface” section.

The FT1509 allows switching between the external display interface operation and the system interface operation by instruction so that the optimal interface is selected for the kind of picture on the panel (still and/or moving picture). The FT1509 writes the display data to the internal GRAM to enable transferring data only when the frame data is updated, which contributes to the reduction of data to be transferred from the system and power consumption required for moving picture display.

3. Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the address setting instruction is written in the IR, the address information is sent from the IR to the AC. When the data is written to the internal GRAM, the AC is automatically incremented (plus one) or decremented (minus

one). The window address function enables writing data only within the rectangular area specified in GRAM by setting.

4. Graphics RAM (GRAM)

GRAM is graphics RAM, which is used to store graphic pattern data.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltages according to the grayscale data in the γ-correction registers to enable a maximum 262k-color display.

6. Timing Generator

The timing generator generates timing signals to operate internal circuits such as GRAM. The FT1509 generates timing signals for display operation such as the RAM read operation and for internal operation such as RAM access from MPU and outputs them separately to avoid mutual interference. Also FMARK is generated internally and output from the timing generator.

7. Oscillator (OSC)

The FT1509 generates the RC oscillation clock signal by internal RC oscillator. No external resistor is needed. Adjust the frame frequency by command setting. In deep standby mode, RC oscillation is halted to reduce power consumption. For details, see “Oscillator”.

8. Liquid crystal driver Circuit

The liquid crystal driver circuit of the FT1509 consists of a 720-channel source driver (S1 ~ S720) and a 432-output gate driver (G1 ~ G432). The display pattern data is latched when 720 bits of data are input. The latched data control the source driver and generates liquid crystal drive waveform. The shift direction of 720-bit source output from the source driver is determined by instruction (SS bit). The shift direction of gate output from the gate driver can be changed by setting the GS bit. The gate pin assignment can be changed by setting the SM bit. Set SM and GS bits to select the optimal scan mode for the module.

9. Internal logic power supply regulator

The internal logic power supply regulator generates internal power supply for RAM: VDD.

10. Liquid crystal drive power supply circuit

The liquid crystal drive power supply circuit generates the voltage levels to drive liquid crystal: VREG1OUT, DDVDH, VGL, VGH, Vcom.

GRAM Address MAP

Instruction

The FT1509 adopts 18-bit bus architecture to interface to high-performance microcomputer. The FT1509 starts internal processing when the control information sent via 18-, 16-, 9-, 8-bit ports is stored in the instruction register (IR) and the data register (DR). Since the internal operation of the FT1509 is controlled by the signals sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signals (IB15 to IB0) are called instruction. The FT1509 accesses the internal GRAM in units of 18 bits. The instructions of the FT1509 are categorized into the following 8 groups.

1. Index specification
2. Status Read
3. Display control
4. Power management control
5. GRAM address setting
6. Transfer data to/from the internal GRAM
7. γ-correction
8. EPROM control

Normally, the instruction to write data in the GRAM is used the most often. In order to minimize the data transfer and lessen the programming load on the microcomputer, the FT1509 rewrites data only within the window address area and updates internal GRAM address in the address counter automatically as it writes data in the internal GRAM. The FT1509 writes instruction consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycle).

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

Instruction data format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface as shown below.

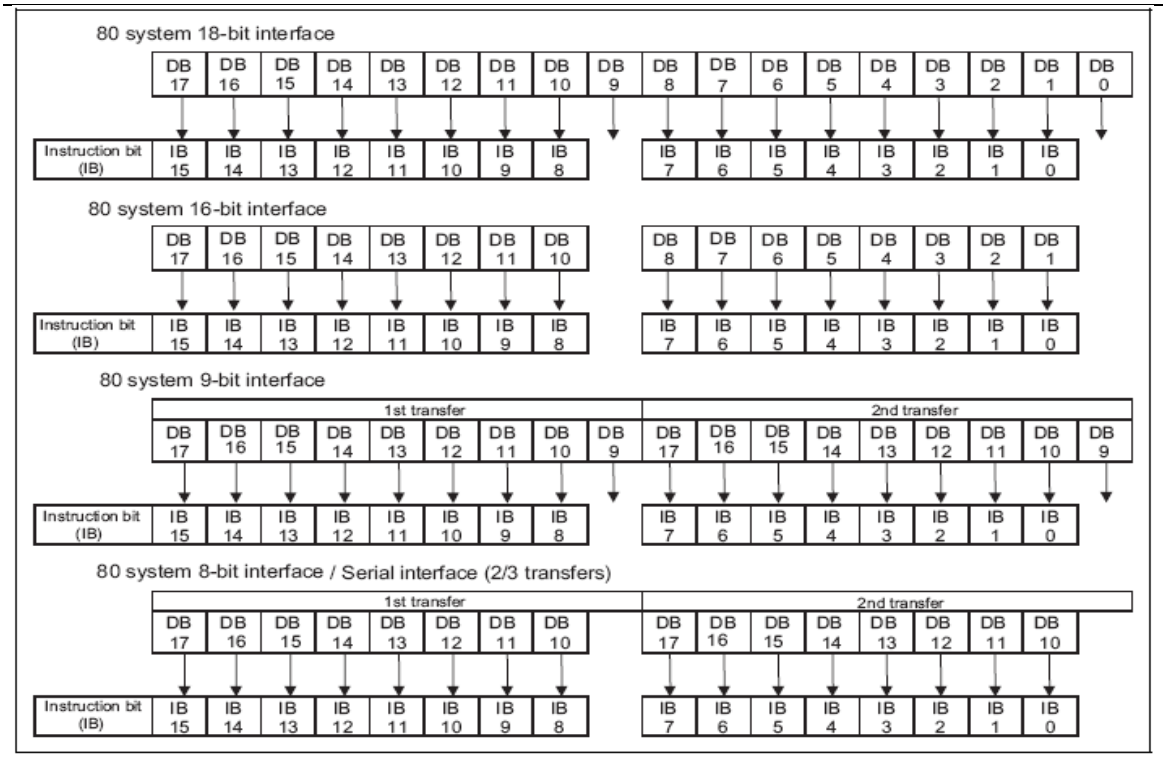


Figure 4: Instruction format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface (see Figure 10 Instruction format).

Index specification/Status read/Display control instructions

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register represents the index of the control register to be accessed (R00h ~ RFFh) and for RAM control using binary numbers from “0000_0000” to “1111_1111”. The access to a register and instruction bits in it is prohibited unless the index is specified in the index register.

Status read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The internal status of the FT1509 can be read out from the SR register.

L[7:0]: represents the line where the FT1509 drives liquid crystal.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The start oscillation instruction starts the oscillator from a halt in standby mode. After executing this

instruction, wait at least 10 ms to stabilize the oscillator before issuing next instruction.

*The device code “0001”H is read out when reading out this register.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.
When SS = “0”, the source driver output shift from S1 to S720.
When SS = “1”, the source driver output shift from S720 to S1.
The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S720.
When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S720 to S1.

When changing the SS and BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module. See “Scan mode setting”.

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

EOR: By setting EOR = “1”, the polarity of C pattern waveform (n-line inversion waveform) is inverted according to the result of EOR (exclusive OR) between the odd/even-number frame select signal and the n-line inversion signal. Set EOR = 1 when the number of lines to drive liquid crystal is not compatible with n-line inversion waveform. For details, see “n-line inversion AC drive”.

B/C: When B/C = “0”, the liquid crystal drive signal becomes frame-inversion waveform and inverts the polarity of liquid crystal in every frame cycle. When B/C = “1”, liquid crystal drive signal becomes n-line inversion waveform and inverts the polarity of liquid crystal in every (n+1)-line cycle. For details, see “n-line inversion AC drive”.

Internal Source output Control (R91h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W								Eqi1	Eqi0						Sdti2	Sdti1	Sdti0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EQI: Define internal source equalize cycles, EQI=0 that is no equalize cycle, otherwise EQI cycles.

SDTI: define internal source output delay based on the gate falling edge, SDTI=0:one cycle, otherwise SDTI+1 cycles.

Internal Source output Control (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W								LS11	LS10			VCOM_SK1	VCOM_SK0			LS01	LS00
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LS0: Define the source OP work cycle. LS0=0 is one “dfosc” cycle, otherwise LS0+1 cycles.

LS1: Define source overshoot work cycle. LS1=0 is one “dfosc” cycle, otherwise LS1+1 cycles.

VCOM_SK: define VCOM overshoot work cycle. VCOM_SK is a half dfosc cycle, otherwise VCOM_SK/2 cycles.

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	EP F1	EP F0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the FT1509 writes data in the internal GRAM.

AM= “0”, sets the horizontal direction.

AM = “1”, sets the vertical direction.

When a window address area is specified in GRAM, the FT1509 writes data within the window address area in the direction determined by the I/D1-0, AM settings.

I/D[1:0]: The RAM address is automatically incremented (+1) when I/D = “1” and decremented (-1) when I/D = “0” as the FT1509 writes data in the GRAM. The I/D[0] bit sets either increment or decrement of RAM address (AD[7:0]) in horizontal direction. The I/D[1] bit sets either increment or decrement of RAM address (AD[15:8]) in vertical direction. (**Recommended value: I/D[1]=”1”**)The AM bit sets either horizontal or vertical direction in updating RAM address automatically when writing data in the internal RAM.

BGR: Reverses the order of assigning 18-bit RGB data to the data bus (DB17-0) from RGB to BGR

DFM: In combination with the TRI setting, sets the interface format to transfer 18-bit data via 80-system 16-/8-bit bus interface. Make sure to set DFM = “0”, when not using 16-/8-bit interface.

EPF: Set data format when 16bpp (R,G and B) to 18 bpp (r,g,b) is stored in internal RAM. EFP settings are effective when:

1. 80-system 16-bit interface, TRI=0
2. 80-systems 8-bit interface, TRI=0
3. MDDI, DFM=1

EPF	Expand 16bpp (R,G,B) to 18bpp(r,g,b)
2'h0	Same value as MSB is inputted to LSB of R and B r[5:0] = {R[4:0],R[4]} g[5:0]={G[5:0]} b[5:0]={B[4:0],B[4]}
2'h1	"0" is inputted to LSB of r and b r[5:0]= {R[4:0],1'h0} g[5:0]={G[5:0]} b[5:0]={B[4:0],1'h0} Except, R[4:0], B[4:0]=5'h1F → r, b[5:0]=6'h3F G[5:0]=6'h3F → g[5:0]=6'h3F
2'h2	"1" is inputted to LSB of r and b r[5:0]={R[4:0], 1'h1} g[5:0]={G[5:0]} b[5:0]={B[4:0], 1'h1} Except, R[4:0], B[4:0]=5'h0 → r,b[5:0]=6'h00 G[5:0]=6'h0 → g[5:0]=6'h00
2'h3	Setting disabled.

TRI: Sets the interface format when transferring 18-bit data via 80-system 16-/8-bit interface in combination with DFM bit.

In 8-bit interface operation, TRI =0: 16-bit RAM data is transferred in two transfers via 8-bit interface.

TRI =1: 18-bit RAM data is transferred in three transfers via 8-bit interface.

In 16-bit interface operation, TRI =0: 16-bit RAM data is transferred in one-transfer via 16-bit interface.
TRI =1: 18-bit RAM data is transferred in two transfers via 16-bit interface.

Make sure to set TRI = "0", when not using 16-/8-bit interface. Also, set TRI = "0" in read operation.

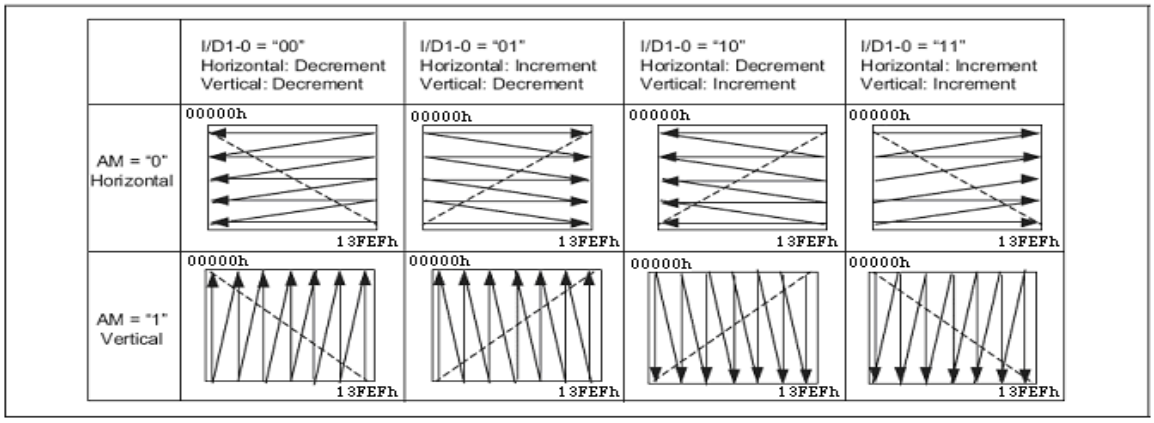


Figure 5: Automatic address transition direction setting (AM, I/D[1:0])

Note: When a window address area is specified in the GRAM, the data is written within the window address area.

Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSZ[1:0]: Sets the resizing factor. When the RSZ bits are set for resizing, the FT1509 writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions, which are contracted according to the factor respectively. See “Resizing function”.

Table 13 Resizing factor (RSZ)

RSZ [1:0]	Resizing Scale	RSZ [1:0]	Resizing Scale
2’h0	No resizing (x1)	2’h2	Setting prohibited
2’h1	x 1/2	2’h3	x 1/4

RCH[1:0]: Sets the number of remainder pixels in horizontal direction when resizing a picture. By specifying the number of remainder pixels by RCH bits, the data can be transferred without taking the remainder pixels into consideration. Make sure that RCH = 2’h0 when not using the resizing function (RSZ = 2’h0) or there are no remainder pixels.

Table 14 Remainder Pixels in Horizontal Direction (RCH) Note: 1 pixel = 1RGB

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
2’h0	0 pixel
2’h1	1 pixel
2’h2	2 pixels
2’h3	3 pixels

RCV[1:0]: Sets the number of remainder pixels in vertical direction when resizing a picture. By specifying the number of remainder pixels by RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2’h0 when not using the resizing function (RSZ = 2’h0) or there are no remainder pixels.

Table 15 Remainder Pixels in Vertical Direction (RCV) Note: 1 pixel = 1RGB

RCV[1:0]	Number of remainder Pixels in Vertical Direction
2’h0	0 pixels
2’h1	1 pixels
2’h2	2 pixels
2’h3	3 pixels

I80-i/F Endian Control (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCREV[1]	TCREV[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TCREV[1:0]: SControls the endian setting (big/little endian: the order of receiving data) when transferring one-pixel data via i80 interface in multiple times. When setting a new value to TCREV[1:0], the order is changed from when the next instruction is executed.

Big/little Endian Control (TCREV)

TCREV [1:0]	2 Transfers/Pixel	3 transfers/Pixel
2’h0	Upper to lower (1^{st} to 2^{nd})	Upper to lower (1^{st},2^{nd},3^{rd})
2’h1	Setting disabled	Setting disabled
2’h2	Setting disabled	Setting disabled
2’h3	Lower to upper (2^{nd} to 1^{st})	Lower to upper (3^{rd},2^{nd},1^{st})

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on the panel when writing D[1] = "1", and is turned off when writing D[1] = "0". When writing D[1] = "0", the graphics display data is retained in the internal GRAM and the FT1509 displays the data when writing D[1] = "1". When D[1] = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D[1-0] = 2'b01, the FT1509 continues internal display operation. When the display is turned off by setting D[1-0] = 2'b00, the FT1509's internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF. For details, see "Instruction Setting".

Table 16

D[1:0]	BASEE	Source output (S1 ~S720)	FMARK signal	Internal operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-lit display level	Operation	Operation
2'h3	0	Non-lit display level	Operation	Operation
	1	Base image display	Operation	Operation

Notes: 1. The data write operation from the microcomputer to the internal RAM is performed irrespective of the setting of the D[1:0] bits.
2. The internal state of the FT1509 in standby mode become the same as when D[1:0] = 2'b00. This does not mean the D[1:0] setting is changed when setting the standby mode.
3. The D[1:0] setting is valid on both 1st and 2nd displays.
4. The non-lit display level from the source output pins is determined by instruction (PTS).

CL: When CL = "1", the FT1509 enters the 8-color mode. Follow the 8-color mode setting sequence when setting the 8-color mode. In 8-color mode, the grayscale amplifiers other than those for the V0 and V63 level are halted. If used in combination with frame-inversion liquid crystal drive, the power consumption will be further reduced.

Table 17 DTE, GON: Controls the output of liquid crystal panel output signal.

GON	DTE	G1 ~ G320
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

BASEE: Base image display enable bit. When BASEE = "0", no base image is displayed. The FT1509 drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed, and the partial display is inactive. The base image indicates the whole display screen. The D[1:0] setting has precedence over the BASEE setting.

PTDE0: Partial image 1 enable bit
PTDE1: Partial image 2 enable bit
PTDE0/1 = 0: turns off partial image. Only base image is displayed.
PTDE0/1 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default		0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

FP [3:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [3:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Note on Setting BP and FP Set the BP and FP bits as follows in respective operation modes.

Table 18 BP and FP Settings

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Table 19 Front and Back Porch period (Line periods)

FP[3:0] or BP[3:0]	Front or Back Porch period (Line periods)	FP[3:0] or BP[3:0]	Front or Back Porch period (Line periods)
4'h0	2 lines	4'h8	8 lines
4'h1	2 lines	4'h9	9 lines
4'h2	2 lines	4'hA	10 lines
4'h3	3 lines	4'hB	11 lines
4'h4	4 lines	4'hC	12 lines
4'h5	5 lines	4'hD	13 lines
4'h6	6 lines	4'hE	14 lines
4'h7	7 lines	4'hF	14 lines

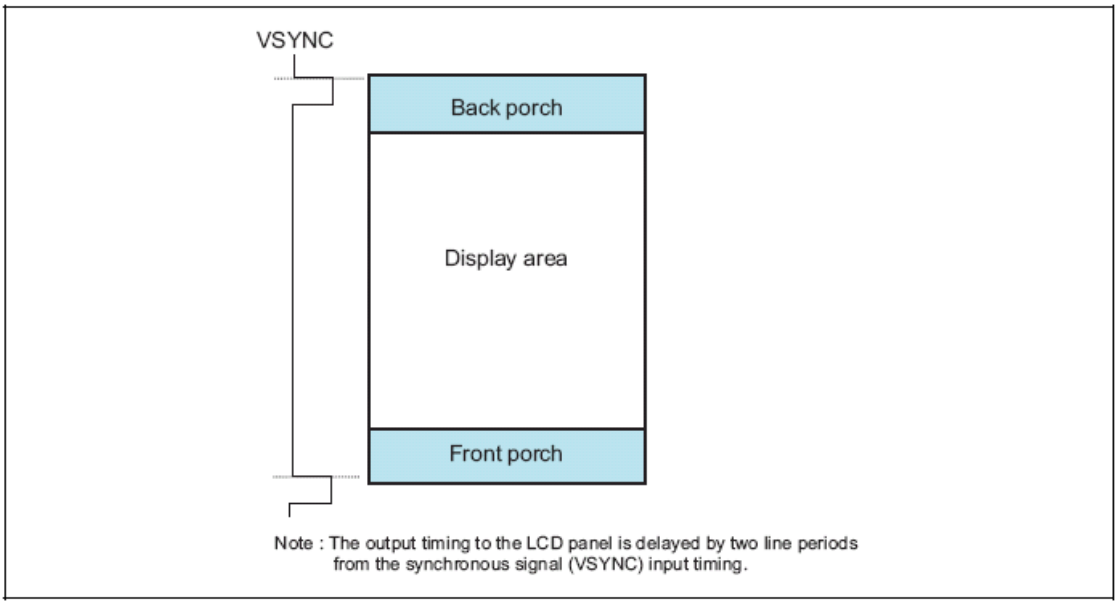


Figure 6: Front, Back Porch periods

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC[3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 20

ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz	ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz
4'h0	0 frame	-	4'h8	17 frames	284ms
4'h1	3 frames	50ms	4'h9	19 frames	317ms
4'h2	5 frames	84ms	4'hA	21 frames	351ms
4'h3	7 frames	117ms	4'hB	23 frames	384ms
4'h4	9 frames	150ms	4'hC	25 frames	418ms
4'h5	11 frames	184ms	4'hD	27 frames	451ms
4'h6	13 frames	217ms	4'hE	29 frames	484ms
4'h7	15 frames	251ms	4'hF	31 frames	518ms

Table 21 PTG[1:0]: Sets the scan mode in non-display area.

PTG[1]	PTG[0]	Scan mode in non-display area	Source output level in non-display area	Vcom output
0	**0**	Normal scan	PTS[2:0] setting	alternating output
0	**1**	VGL (fixed)	PTS[2:0] setting	alternating output
1	**0**	Interval scan	PTS[2:0] setting	alternating output
1	**1**	Interval scan	PTS[2:0] setting	alternating output

PTS[2:0]: Sets the source output level in non-display area drive period (front/back porch period and blank area between partial displays). When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 22 Source output level and voltage generating operation in non-display drive period

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3'h0	V63	V0	V0 to V63	Register setting (DC0, DC1)
3'h1	V63	V0	V0 to V63	Register setting (DC0, DC1)
3'h2	GND	GND	V0 to V63	Register setting (DC0, DC1)
3'h3	Hi-Z	Hi-Z	V0 to V63	Register setting (DC0, DC1)
3'h4	V63	V0	V0 and V63	1/2 the frequency set by DC0, DC1
3'h5	V63	V0	V0 and V63	1/2 the frequency set by DC0, DC1
3'h6	GND	GND	V0 and V63	1/2 the frequency set by DC0, DC1
3'h7	Hi-Z	Hi-Z	V0 and V63	1/2 the frequency set by DC0, DC1

Notes: 1. The power efficiency improvement from halting grayscale amplifiers and slowing down the step-up clock frequency can be obtained in non-display drive period.

2. The gate output level in non-display area drive period is determined by PTG[1:0].

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the FT1509 starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits. See “FMARK” for details.

Table 23

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

Display interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

Table 25 Display Interface

DM[1:0]	Display Interface
2’h0	Internal clock operations
2’h2	VSYNC interface
2’h3	VSYNC interface

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. When RM = 0, it is possible to write data via system interface.

Table 26 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface

The FT1509 selects the optimum interface according to the displayed image by setting instruction as follows.

Table 27

The state of display	Operation Mode	RAM Access (RM)	Display Operation Mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 2’h0)
Rewrite still picture area while displaying moving pictures.	System interface	System interface (RM = 0)	Interanl clock operation (DM1-0 = 2’h1)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 2’h2)

Notes: 1. Instructions are set only via system interface.
2. The VSYNC interfaces cannot be used simultaneously.
3. See the “External Display Interface” section for the sequences when switching from one mode to another.

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator’s clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the FT1509 to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the “VSYNC Interface” section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the FT1509 according to the instruction settings for these periods.

Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9’h00, a high-active pulse FMARK is outputted at the start of back porch period for 1H period (IOVcc-GND amplitude signal). FMARK can be used as the trigger signal for frame synchronous write operation. See “FMARK” for details.

Make sure the setting restriction 9’h000 ≤ FMP ≤ BP+NL+FP.

Table 29

FMP[8:0]	FMARK output position
9’h000	0th line
9’h001	1st line
9’h002	2nd line
….	….
9’h14E	334th line
9’h14F	335th line
9’h150~1FF	Setting disabled

Power control

Power control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STB: When STB = 1, the FT1509 enters the standby mode. In standby mode, the FT1509 halts RC oscillation and receiving external clock signal to halt the display operation completely. In setting the standby mode, follow the standby mode setting sequence. The instruction register setting is retained in standby mode. The FT1509 accepts only the following instructions in standby mode:

1. Exit standby mode (STB = 0)
2. Start oscillation

SLP: When SLP = 1, the FT1509 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change to the GRAM data and instruction setting is accepted and the GRAM data and the instruction setting are maintained in sleep mode.

DSTB: When DSTB = 1, the FT1509 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the FT1509 enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = 3'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Table 30 constant current in operational amplifiers

AP[2:0]	Gamma driver amplifiers
3'h0	Halt
3'h1	Disable
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	Disable

Note: The values in the table represent the ratios of currents in respective settings to the current.

APE: Liquid crystal power supply enable bit. Set APE = "1" when starting the generation of liquid crystal power supply according to the liquid crystal power supply startup sequence. After starting up the power supply circuit, set APE = "1".

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

Table 31 Step-up factor for step-up circuits

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Vci1 +Vci	-Vci	3xDDVDH	-(Vci+2 x DDVDH
3'h1	Vci1 +Vci	-Vci		-(2xDDVDH)
3'h2				-(Vci+DDVDH)

3'h3	Vci1+Vci	-Vci	Vci+2xDDVDH	-(Vci+2xDDVDH)
3'h4				-2xDDVDH
3'h5				-(Vci+DDVDH)
3'h6	Vci1 +Vci	-Vci	2xDDVDH	-2xDDVDH
3'h7				-(Vci+DDVDH)

Notes:
1. Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.
2. Set the following voltages within the respective ranges:
   DDVDH = 6.0V (max.) VGH = 15.0V (max.)
   VGL = -12.5V (max.) VCL = -3.0V (max.)

SAP: Source driver output control
SAP = 0, Source driver is disabled.
SAP = 1, Source driver is enabled.
When starting the charge-pump of LCD in the Power ON stage, make sure that SAP = 0, and set the SAP = 1, after starting up the LCD power supply circuit.

Power control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VC[2:0]: Sets the factor of Vci to generate the reference voltages VciOUT, Vci1.

Table 32 Reference voltage setting (Vci1)

VC[2:0]	VciOUT (reference voltage) Vci1 voltage
3'h0	0.90 x Vci
3'h1	0.80 x Vci
3'h2	0.70 x Vci
3'h3	0.60 x Vci
3'h4	0.50 x Vci
3'h5	0.40 x Vci
3'h6	Vci
3'h7	Vci

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current/power consumption. Adjust the frequency taking the trade-off between the display quality and the current/power consumption into account.

Table 33 operating frequencies of step-up circuits 1/2

DC0[2:0]	Step-up circuit 1 Operating frequency (f_{DCDC1})	DC1[2:0]	Step-up circuit 2 Operating frequency (f_{DCDC2})
3'h0	fosc	3'h0	fosc/4
3'h1	fosc/2	3'h1	fosc/8

3'h2	fosc/4	3'h2	fosc/16
3'h3	fosc/8	3'h3	fosc/32
3'h4	fosc/16	3'h4	fosc/64
3'h5	fosc/32	3'h5	fosc/128
3'h6	fosc/64	3'h6	fosc/256
3'h7	Halt set-up circuit 1	3'h7	Halt set-up circuit 2

Note: Make sure $f_{DCDC1} \geq f_{DCDC2}$. when setting the operating frequencies of DC0[2:0] and DC1[2:0]

Power control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VRH[3:0]: Sets the amplifying rate (1.6 ~ 1.9) of Vci to generate the output of VREG1OUT, which is a reference level of VCOM and grayscale voltage.

VRH[3:0]	VREG1OUT
4'h0	Halt(Hi-Z)
4'h1	Vci x1.4
4'h2	Vci x1.45
4'h3	Vci x1.5
4'h4	Vci x1.55
4'h5	Vci x1.6
4'h6	Vci x1.65
4'h7	Vci x1.7
4'h8	Vci x1.75
4'h9	Vci x1.8
4'h10	Vci x1.85
4'h11	Disable
4'h12	Disable
4'h13	Disable
4'h14	Disable
4'h15	Disable

PON: Controls ON/OFF of VGH/VGL. When setting the PON bit, follow the power supply startup sequence.

PON = "0": Stop the step-up operation to generate VGH/VGL.

PON = "1": Start the step-up operation to generate VGH/VGL.

VCMR: Selects either external resistor (VcomR) or internal electric volume (VCM) to set the electrical potential of VcomH.

Table 35

VCMR	VCOMH1 electrical potential
0	VCOMR (variable resistor)
1	Internal electronic volume

Power control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0

W	1	0	0	0	VDV6	VDV5	VDV4	VDV3	VDV2	0	0	0	0	0	0	VDV1	VDV0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[6:0]: Sets the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.685 to 1.32 x VREG1OUT.

Table 36 VDV: Vcom amplitude

VDV[6:0]	Vcom amplitude	VDV[6:0]	Vcom amplitude
7'h00	VREG1OUT x 0.685	7'h40	VREG1OUT x 1.005
7'h01	VREG1OUT x 0.690	7'h41	VREG1OUT x 1.010
7'h02	VREG1OUT x 0.695	7'h42	VREG1OUT x 1.015
7'h03	VREG1OUT x 0.700	7'h43	VREG1OUT x 1.020
7'h04	VREG1OUT x 0.705	7'h44	VREG1OUT x 1.025
7'h05	VREG1OUT x 0.710	7'h45	VREG1OUT x 1.030
7'h06	VREG1OUT x 0.715	7'h46	VREG1OUT x 1.035
7'h07	VREG1OUT x 0.720	7'h47	VREG1OUT x 1.040
7'h08	VREG1OUT x 0.725	7'h48	VREG1OUT x 1.045
7'h09	VREG1OUT x 0.730	7'h49	VREG1OUT x 1.050
7'h0A	VREG1OUT x 0.735	7'h4A	VREG1OUT x 1.055
7'h0B	VREG1OUT x 0.740	7'h4B	VREG1OUT x 1.060
7'h0C	VREG1OUT x 0.745	7'h4C	VREG1OUT x 1.065
7'h0D	VREG1OUT x 0.750	7'h4D	VREG1OUT x 1.070
7'h0E	VREG1OUT x 0.755	7'h4E	VREG1OUT x 1.075
7'h0F	VREG1OUT x 0.760	7'h4F	VREG1OUT x 1.080
7'h10	VREG1OUT x 0.765	7'h50	VREG1OUT x 1.085
7'h11	VREG1OUT x 0.770	7'h51	VREG1OUT x 1.090
7'h12	VREG1OUT x 0.775	7'h52	VREG1OUT x 1.095
7'h13	VREG1OUT x 0.780	7'h53	VREG1OUT x 1.100
7'h14	VREG1OUT x 0.785	7'h54	VREG1OUT x 1.105
7'h15	VREG1OUT x 0.790	7'h55	VREG1OUT x 1.110
7'h16	VREG1OUT x 0.795	7'h56	VREG1OUT x 1.115
7'h17	VREG1OUT x 0.800	7'h57	VREG1OUT x 1.120
7'h18	VREG1OUT x 0.805	7'h58	VREG1OUT x 1.125
7'h19	VREG1OUT x 0.810	7'h59	VREG1OUT x 1.130
7'h1A	VREG1OUT x 0.815	7'h5A	VREG1OUT x 1.135
7'h1B	VREG1OUT x 0.820	7'h5B	VREG1OUT x 1.140
7'h1C	VREG1OUT x 0.825	7'h5C	VREG1OUT x 1.145
7'h1D	VREG1OUT x 0.830	7'h5D	VREG1OUT x 1.150
7'h1E	VREG1OUT x 0.835	7'h5E	VREG1OUT x 1.155
7'h1F	VREG1OUT x 0.840	7'h5F	VREG1OUT x 1.160
7'h20	VREG1OUT x 0.845	7'h60	VREG1OUT x 1.165
7'h21	VREG1OUT x 0.850	7'h61	VREG1OUT x 1.170
7'h22	VREG1OUT x 0.855	7'h62	VREG1OUT x 1.175
7'h23	VREG1OUT x 0.860	7'h63	VREG1OUT x 1.180
7'h24	VREG1OUT x 0.865	7'h64	VREG1OUT x 1.185
7'h25	VREG1OUT x 0.870	7'h65	VREG1OUT x 1.190
7'h26	VREG1OUT x 0.875	7'h66	VREG1OUT x 1.195
7'h27	VREG1OUT x 0.880	7'h67	VREG1OUT x 1.200
7'h28	VREG1OUT x 0.885	7'h68	VREG1OUT x 1.205
7'h29	VREG1OUT x 0.890	7'h69	VREG1OUT x 1.210
7'h2A	VREG1OUT x 0.895	7'h6A	VREG1OUT x 1.215
7'h2B	VREG1OUT x 0.900	7'h6B	VREG1OUT x 1.220
7'h2C	VREG1OUT x 0.905	7'h6C	VREG1OUT x 1.225

7'h2D	VREG1OUT x 0.910	7'h6D	VREG1OUT x 1.230
7'h2E	VREG1OUT x 0.915	7'h6E	VREG1OUT x 1.235
7'h2F	VREG1OUT x 0.920	7'h6F	VREG1OUT x 1.240
7'h30	VREG1OUT x 0.925	7'h70	VREG1OUT x 1.245
7'h31	VREG1OUT x 0.930	7'h71	VREG1OUT x 1.250
7'h32	VREG1OUT x 0.935	7'h72	VREG1OUT x 1.255
7'h33	VREG1OUT x 0.940	7'h73	VREG1OUT x 1.260
7'h34	VREG1OUT x 0.945	7'h74	VREG1OUT x 1.265
7'h35	VREG1OUT x 0.950	7'h75	VREG1OUT x 1.270
7'h36	VREG1OUT x 0.955	7'h76	VREG1OUT x 1.275
7'h37	VREG1OUT x 0.960	7'h77	VREG1OUT x 1.280
7'h38	VREG1OUT x 0.965	7'h78	VREG1OUT x 1.285
7'h39	VREG1OUT x 0.970	7'h79	VREG1OUT x 1.290
7'h3A	VREG1OUT x 0.975	7'h7A	VREG1OUT x 1.295
7'h3B	VREG1OUT x 0.980	7'h7B	VREG1OUT x 1.300
7'h3C	VREG1OUT x 0.985	7'h7C	VREG1OUT x 1.305
7'h3D	VREG1OUT x 0.990	7'h7D	VREG1OUT x 1.310
7'h3E	VREG1OUT x 0.995	7'h7E	VREG1OUT x 1.315
7'h3F	VREG1OUT x 1.000	7'h7F	VREG1OUT x 1.320

Note: Set the Vcom amplitude from 2.5V to (DDVDH-0.5)V.

RAM access instruction

RAM Address set horizontal address (R20h), RAM Address set vertical address (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Top: R20h, Bottom: R21h

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the AM, I/D[1:0] settings as the FT1509 writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note : In internal clock operation and VSYNC interface operation (RM = "0"), the address AD16-0 is set when executing the instruction.

Table 37 GRAM address range

AD[16:0]	GRAM Setting
17'h00000 ~ 17'h000EF	Bitmap data on the first line
17'h00100 ~ 17'h001EF	Bitmap data on the second line
17'h00200 ~ 17'h002EF	Bitmap data on the third line
17'h00300 ~ 17'h003EF	Bitmap data on the fourth line

:	:
17'h13C00 ~ 17'h13CEF	Bitmap data on the 317th line
17'h13D00 ~ 17'h13DEF	Bitmap data on the 318th line
17'h13E00 ~ 17'h13EEF	Bitmap data on the 319th line
17'h13F00 ~ 17'h13FEF	Bitmap data on the 320th line

Write/Read RAM data

Write Data to GRAM (R22h)

R/W	RS	IB15 IB14 IB13 IB12 IB11 IB10 IB9 IB8 IB7 IB6 IB5 IB4 IB3 IB2 IB1 IB0
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation

WD[17:0]: The FT1509 expands data into 18 bits internally in write operation. The format to expand data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The FT1509 automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. In deep standby mode, GRAM access is disabled. In 8-/16-bit interface operation, the MSBs of R and B dot are written as the LSBs of respective dot to expand data into 18 bits. In this case, 65,536 colors are available.

Table 38 GRAM data and LCD output level (REV = "0")

GRAM data (RGB)	Selected grayscale		GRAM data (RGB)	Selected grayscale	
	Negative	Positive		Negative	Positive
000000	V0	V63	100000	V32	V31
000001	V1	V62	100001	V33	V30
000010	V2	V61	100010	V34	V29
000011	V3	V60	100011	V35	V28
000100	V4	V59	100100	V36	V27
000101	V5	V58	100101	V37	V26
000110	V6	V57	100110	V38	V25
000111	V7	V6	100111	V39	V24
001000	V8	V55	101000	V40	V23
001001	V9	V54	101001	V41	V22
001010	V10	V53	101010	V42	V21
001011	V11	V52	101011	V43	V20
001100	V12	V51	101100	V44	V19
001101	V13	V50	101101	V45	V18
001110	V14	V49	101110	V46	V17
001111	V15	V48	101111	V47	V16
010000	V16	V47	110000	V48	V15
010001	V17	V46	110001	V49	V14
010010	V18	V45	110010	V50	V13

010011	V19	V44	110011	V51	V12
010100	V20	V43	110100	V52	V11
010101	V21	V42	110101	V53	V10
010110	V22	V41	110110	V54	V9
010111	V23	V40	110111	V55	V8
011000	V24	V39	111000	V56	V7
011001	V25	V38	111001	V57	V6
011010	V26	V37	111010	V58	V5
011011	V27	V36	111011	V59	V4
011100	V28	V35	111100	V60	V3
011101	V29	V34	111101	V61	V2
011110	V30	V33	111110	V62	V1
011111	V31	V32	111111	V63	V0

RAM Access via System interface

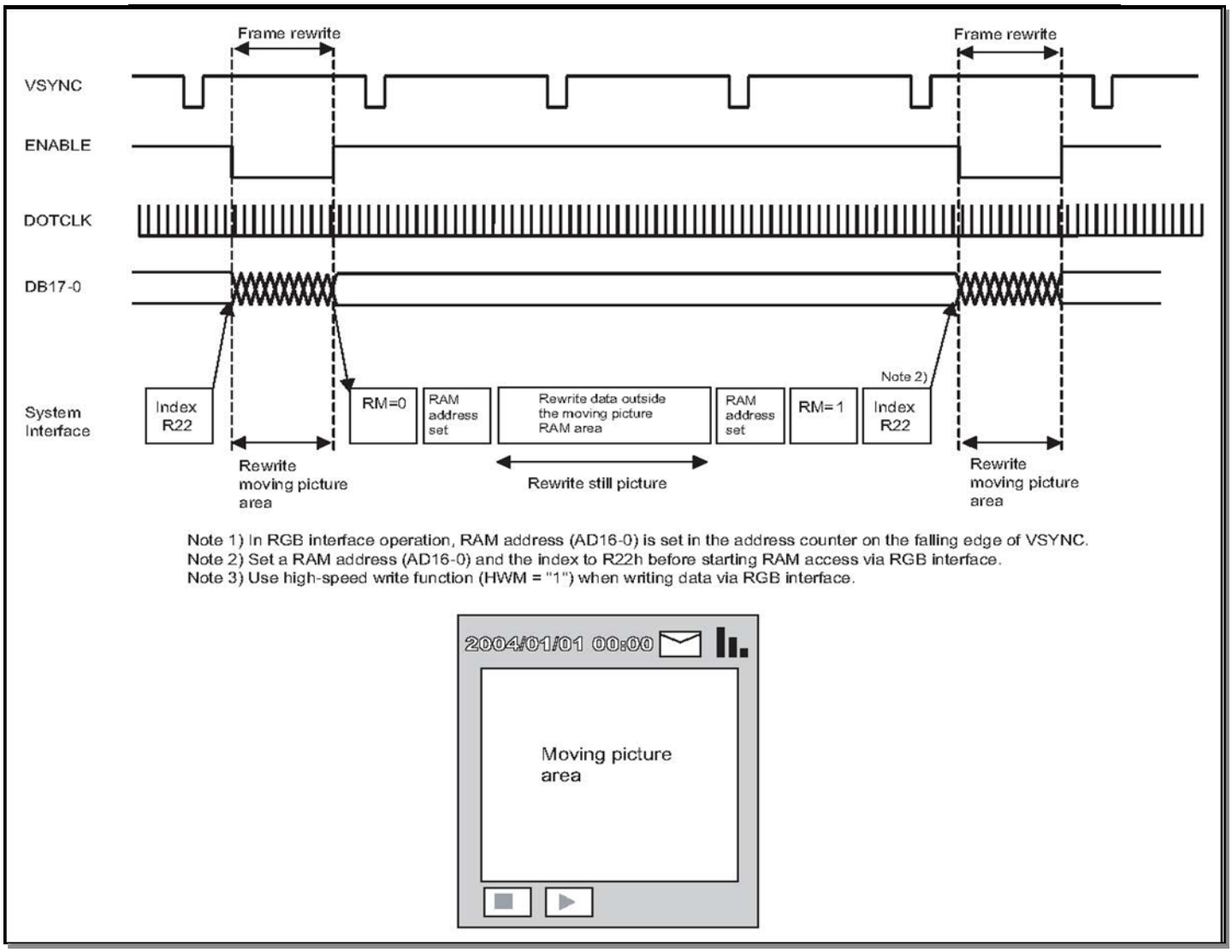


Figure 7

Read Data from GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.															

RD[17:0]: 18-bit data read from the GRAM. RAM read data RD[17:0] is transferred via different data bus in different interface operation.

When the FT1509 reads data from the GRAM to the microcomputer, the first word, which is read immediately after the RAM address set instruction is executed, is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the FT1509 reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

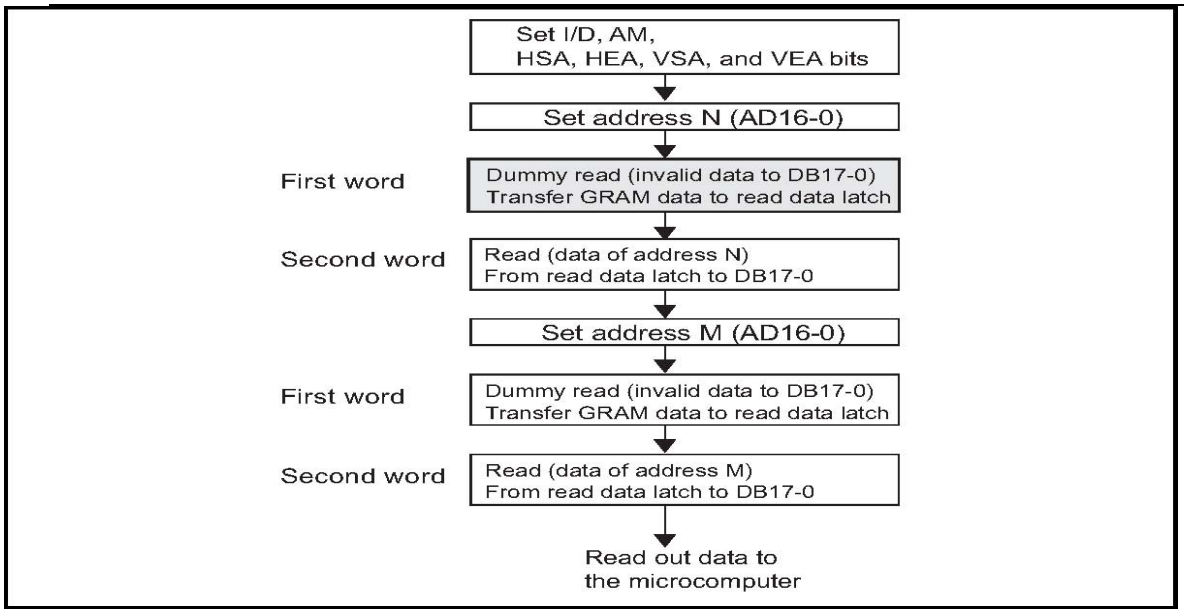


Figure 8: GRAM read sequence

Power control 7 (R29h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM[5:0]: Selects the internal electronic volume applied to VREG1OUT to set the VcomH electrical potential.

Table 39 VCM: internal electronic volume adjustment

VCM[5:0]	VcomH	VCM[5:0]	VcomH
6'h00	VREG1OUT x 0.685	6'h20	VREG1OUT x 0.845
6'h01	VREG1OUT x 0.690	6'h21	VREG1OUT x 0.850
6'h02	VREG1OUT x 0.695	6'h22	VREG1OUT x 0.855
6'h03	VREG1OUT x 0.700	6'h23	VREG1OUT x 0.860
6'h04	VREG1OUT x 0.705	6'h24	VREG1OUT x 0.865
6'h05	VREG1OUT x 0.710	6'h25	VREG1OUT x 0.870
6'h06	VREG1OUT x 0.715	6'h26	VREG1OUT x 0.875
6'h07	VREG1OUT x 0.720	6'h27	VREG1OUT x 0.880
6'h08	VREG1OUT x 0.725	6'h28	VREG1OUT x 0.885
6'h09	VREG1OUT x 0.730	6'h29	VREG1OUT x 0.890
6'h0A	VREG1OUT x 0.735	6'h2A	VREG1OUT x 0.895
6'h0B	VREG1OUT x 0.740	6'h2B	VREG1OUT x 0.900
6'h0C	VREG1OUT x 0.745	6'h2C	VREG1OUT x 0.905
6'h0D	VREG1OUT x 0.750	6'h2D	VREG1OUT x 0.910
6'h0E	VREG1OUT x 0.755	6'h2E	VREG1OUT x 0.915
6'h0F	VREG1OUT x 0.760	6'h2F	VREG1OUT x 0.920
6'h10	VREG1OUT x 0.765	6'h30	VREG1OUT x 0.925
6'h11	VREG1OUT x 0.770	6'h31	VREG1OUT x 0.930
6'h12	VREG1OUT x 0.775	6'h32	VREG1OUT x 0.935
6'h13	VREG1OUT x 0.780	6'h33	VREG1OUT x 0.940

6'h14	VREG1OUT x 0.785	6'h34	VREG1OUT x 0.945
6'h15	VREG1OUT x 0.790	6'h35	VREG1OUT x 0.950
6'h16	VREG1OUT x 0.795	6'h36	VREG1OUT x 0.955
6'h17	VREG1OUT x 0.800	6'h37	VREG1OUT x 0.960
6'h18	VREG1OUT x 0.805	6'h38	VREG1OUT x 0.965
6'h19	VREG1OUT x 0.810	6'h39	VREG1OUT x 0.970
6'h1A	VREG1OUT x 0.815	6'h3A	VREG1OUT x 0.975
6'h1B	VREG1OUT x 0.820	6'h3B	VREG1OUT x 0.980
6'h1C	VREG1OUT x 0.825	6'h3C	VREG1OUT x 0.985
6'h1D	VREG1OUT x 0.830	6'h3D	VREG1OUT x 0.990
6'h1E	VREG1OUT x 0.835	6'h3E	VREG1OUT x 0.995
6'h1F	VREG1OUT x 0.840	6'h3F	VREG1OUT

Notes: Set VcomH from 2.5V to (DDVDH-0.5)V.

Frame Rate and Color Control (R2Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	16M_EN	Dither	0	0	0	0	0	0	0	0	0	0	0	RC2	RC1	RC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RC[2:0]: Set the internal oscillator frequency.

Table 40 RC: OSC frequency

RC2	RC1	RC0	(fosc) OSC frequency (kHz)
0	0	0	452
0	0	1	536
0	1	0	652
0	1	1	821
1	0	0	400
1	0	1	336
1	1	0	284
1	1	1	External Clock

16M_EN: Select the color depth. 16M_EN=0 (262K color, default), 16M_EN=1 (16.7M color dither)

Dither: Dithering function control. When the dithering function is enabled, the 24-bit input data will be dithered into 18-bit and the display quality is closed to 16.7M color. Dither=0 (Disable, default), Dither=1 (Enable). The dithering input data transfer format is as below (16M_EN=1, Dither=1).

- 18-bit interface: 2 transfer mode
  - 1st transfer: DB17 ~ DB10, DB8 ~ DB1
  - 2nd transfer: DB17 ~ DB10
- 16-bit interface: 2 transfer mode (TRIREG=1, DFM=0)
  - 1st transfer: DB17 ~ DB10, DB8 ~ DB1
  - 2nd transfer: DB17 ~ DB10
- 8-bit interface: 3 transfer mode (TRIREG=1, DFM=1)
  - 1st transfer: DB17 ~ DB10
  - 2nd transfer: DB17 ~ DB10
  - 3rd transfer: DB17 ~ DB10

γ Control Instruction

γ Control (1) ~ (10) (R30h ~ R3Dh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP1 [2]	PKP1 [1]	PKP1 [0]	0	0	0	0	0	PKP0 [2]	PKP0 [1]	PKP0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31	W	1	0	0	0	0	0	PKP3 [2]	PKP3 [1]	PKP3 [0]	0	0	0	0	0	PKP2 [2]	PKP2 [1]	PKP2 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R32	W	1	0	0	0	0	0	PKP5 [2]	PKP5 [1]	PKP5 [0]	0	0	0	0	0	PKP4 [2]	PKP4 [1]	PKP4 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R35	W	1	0	0	0	0	0	PRP1 [2]	PRP1 [1]	PRP1 [0]	0	0	0	0	0	PRP0 [2]	PRP0 [1]	PRP0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R36	W	1	0	0	0	VRP1 [4]	VRP1 [3]	VRP1 [2]	VRP1 [1]	VRP1 [0]	0	0	0	VRP0 [4]	VRP0 [3]	VRP0 [2]	VRP0 [1]	VRP0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R37	W	1	0	0	0	0	0	PKN1 [2]	PKN1 [1]	PKN1 [0]	0	0	0	0	0	PKN0 [2]	PKN0 [1]	PKN0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38	W	1	0	0	0	0	0	PKN3 [2]	PKN3 [1]	PKN3 [0]	0	0	0	0	0	PKN2 [2]	PKN2 [1]	PKN2 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R39	W	1	0	0	0	0	0	PKN5 [2]	PKN5 [1]	PKN5 [0]	0	0	0	0	0	PKN4 [2]	PKN4 [1]	PKN4 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3C	W	1	0	0	0	0	0	PRN1 [2]	PRN1 [1]	PRN1 [0]	0	0	0	0	0	PRN0 [2]	PRN0 [1]	PRN0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R3D	W	1	0	0	0	VRN1 [4]	VRN1 [3]	VRN1 [2]	VRN1 [1]	VRN1 [0]	0	0	0	VRN0 [4]	VRN0 [3]	VRN0 [2]	VRN0 [1]	VRN0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KP5-0[2:0] γ fine adjustment register for positive polarity
RP1-0[2:0] gradient adjustment register for positive polarity
KN5-0[2:0] γ fine adjustment register for negative polarity
RN1-0[2:0] gradient adjustment register for negative polarity
VRP0[4:0] amplitude adjustment register for positive polarity
VRP1[4:0] amplitude adjustment register for positive polarity
VRN0[4:0] amplitude adjustment register for negative polarity
VRN1[4:0] amplitude adjustment register for negative polarity
See “γCorrection function” for details.

Window address control instruction

Window horizontal RAM start address (R50h), Window horizontal RAM end address (R51h)
Window vertical RAM start address (R52h), Window vertical RAM end address (R53h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R50	W/R	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	W/R	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	Default		0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1
R52	W/R	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53	W/R	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	Default		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

HSA[7:0]/HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that “00”h ≤ HSA[7:0] < HEA[7:0] ≤ “EF”h and “04”h ≤ HEA - HSA

VSA[8:0]/VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that “000”h ≤ VSA[8:0] < VEA[8:0] ≤ “13F”h.

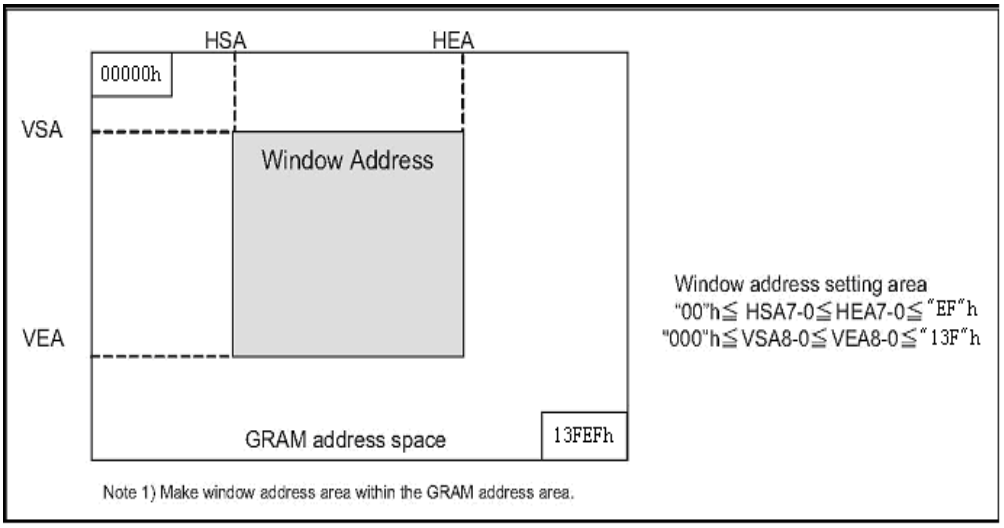


Figure 9: GRAM address map and window address area

Base image display control instruction

Driver output control (R60h), Base image display control (R61h), Vertical scroll control (R6Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R60	W/R	1	GS	0	NL 5	NL 4	NL 3	NL 2	NL 1	NL0	0	0	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R61	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6A	W/R	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the FT1509 to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 42 GRAM Data-grayscale level inversion

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

GS: Sets the direction of scan by the gate driver in the range determined by SCN[5:0] and NL[5:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G320.

When GS = 1, the scan direction is from G320 to G1

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 43

NL[5:0]	LCD drive line	NL[5:0]	LCD drive line	NL[5:0]	LCD drive line	NL[5:0]	LCD drive line
6'h00	0 line	6'h0D	112 lines	6'h1A	216 lines	6'h27	320 lines
6'h01	16 lines	6'h0E	120 lines	6'h1B	224 lines	6'h28—6'h3F	320 lines
6'h02	24 lines	6'h0F	128 lines	6'h1C	232 lines		
6'h03	32 lines	6'h10	136 lines	6'h1D	240 lines		
6'h04	40 lines	6'h11	144 lines	6'h1E	248 lines		
6'h05	48 lines	6'h12	152 lines	6'h1F	256 lines		
6'h06	56 lines	6'h13	160 lines	6'h20	264 lines		
6'h07	64 lines	6'h14	168 lines	6'h21	272 lines		
6'h08	72 lines	6'h15	176 lines	6'h22	280 lines		
6'h09	80 lines	6'h16	184 lines	6'h23	288 lines		
6'h0A	88 lines	6'h17	192 lines	6'h24	296 lines		
6'h0B	96 lines	6'h18	200 lines	6'h25	304 lines		
6'h0C	104 lines	6'h19	208 lines	6'h26	312 lines		

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

Table 44

SCN [5:0]	Scan start position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28-6'h3F	Disabled	Disabled	Disabled	Disabled

VLE: When VLE1 = 1, a vertical scroll is performed in the base image from the line (of the physical display) determined by VL[8:0] bit. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE=0.

VLE	base image
0	Fixed display
1	Scrolling

NDL: Set the source driver output level in the non-display area.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE=0.

NDL	Non-display area	
	Positive Polarity	Negative Polarity
0	V63	V0
1	V0	V63

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0] in this case. Make sure that VL[8:0] ≤ **160**.

Partial control instruction

Partial image 1 display position (R80h)

Partial image 1 RAM start address (R81h), Partial image 1 RAM end address (R82h)

Partial image 2 display position (R83h)

Partial image 2 RAM start address (R84h), Partial image 2 RAM end address (R85h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R80	W	1	0	0	0	0	0	0	0	PTD P0[8]	PTD P0[7]	PTD P0[6]	PTD P0[5]	PTD P0[4]	PTD P0[3]	PTD P0[2]	PTD P0[1]	PTD P0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R81	W		0	0	0	0	0	0	0	PTS A0[8]	PTS A0[7]	PTS A0[6]	PTS A0[5]	PTS A0[4]	PTS A0[3]	PTS A0[2]	PTS A0[1]	PTS A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82	W		0	0	0	0	0	0	0	PTE A0[8]	PTE A0[7]	PTE A0[6]	PTE A0[5]	PTE A0[4]	PTE A0[3]	PTE A0[2]	PTE A0[1]	PTE A0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R83	W	1	0	0	0	0	0	0	0	PTD P1[8]	PTD P1[7]	PTD P1[6]	PTD P1[5]	PTD P1[4]	PTD P1[3]	PTD P1[2]	PTD P1[1]	PTD P1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R84	W	1	0	0	0	0	0	0	0	PTS A1[8]	PTS A1[7]	PTS A1[6]	PTS A1[5]	PTS A1[4]	PTS A1[3]	PTS A1[2]	PTS A1[1]	PTS A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R85	W	1	0	0	0	0	0	0	0	PTE A1[8]	PTE A1[7]	PTE A1[6]	PTE A1[5]	PTE A1[4]	PTE A1[3]	PTE A1[2]	PTE A1[1]	PTE A1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display position of partial image 1.
PTDP1[8:0]: Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting, make sure

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display area: (PTDP0, PTDP0+(PTEA0 – PTSA0))
Coordinates of partial image 2 display area: (PTDP1, PTDP1+(PTEA1 – PTSA1))

If PTDP0 is set to “9’h000”, the partial image 1 is displayed from the 1st line of the panel on the base image.

PTSA0[8:0] PTEA0[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[8:0] ≤ PTEA0[8:0]. **Make sure PTSA0[8:0]**

≤PTDP0[8:0].

PTSA1[8:0] PTEA1[8:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure PTSA1[8:0] ≤ PTEA1[8:0]. **Make sure PTSA1[8:0] ≤PTDP1[8:0]**.

Panel interface control instruction

Panel interface control 1 (R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the FT1509's display operation is synchronized with internal clock signal.

Table 45 Clocks per Line

RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line
5'h00—5'h0F	Disabled	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clock	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

Note: internal clock operation: the frequency of which is determined by instruction (DIVI), from the reference point.

DIVI[1:0]: Sets the division ratio of internal clock frequency. The FT1509's internal operation is synchronized with the frequency-divided internal clock, the frequency of which is divided by the division ratio set by DIVI[1:0]. When changing the DIVI[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed.

Table 46 Division ratio of the internal operation clock

DIVI[1:0]	Division Ratio	Internal Operation Clock Frequency
2'h0	1/1	fosc / 1
2'h1	1/2	fosc / 2
2'h2	1/4	fosc / 4
2'h3	1/8	fosc / 8

Note: fosc: RC oscillation frequency

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, the frame frequency must be adjusted. See "Frame-Frequency Adjustment Function" for details.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clocks per line x division ratio x (line} + \text{BP} + \text{FP)}} \quad [\text{Hz}]$$

fosc : RC oscillation frequency

Line: Number of lines to drive the LCD (NL bits)

Division ratio: DIVI

Clocks per line: RTNI

Panel interface control 2 (R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOI2	NOI1	NOI0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOI[2:0]: Sets the non-overlap period of gate output when the FT1509's display operation is synchronized with internal clock signal.

Table 47

NOI[2:0]	Gate non-overlap period	NOI[2:0]	Gate non-overlap period
3'h0	0 clocks	3'h4	4 clocks
3'h1	1 clocks	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

EPROM control

EPROM access control 1 (RA0h), EPROM access control 2 (RA1h), Calibration control (RA4h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RA0	W	1	0	0	0	0	0	0	0	0	TE	0	EOP [1]	EOP [0]	0	0	EAD [1]	EAD [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA1	W		0	0	0	0	0	0	0	0	ED [7]	ED [6]	ED [5]	ED [4]	ED [3]	ED [2]	ED [1]	ED [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TE: Enable internal EPROM control bit (EOP). Follow the PROM control sequence when setting TE. When resetting register (loading EOP = 2'h2) and executing calibration, TE is set automatically according to the internal automatic sequence and it does not have to be set.

EOP[1:0]: Internal EPROM control bit. Follow the PROM control sequence when setting EOP[1:0].

Table 51

EOP[1:0]	EPROM control
2'h0	Halt

2'h1	Write
2'h2	Reset register (load)

EAD[1:0]: Internal EPROM address. Set EAD[1:0] = 00 ~ 10 when writing to the internal EPROM. The EAD[1:0] setting determines the register (R28h, R29h, R2Ah) to write the data ED[7:0] (see Table 59).

ED[7:0]: Internal EPROM write data.

Table 52

EAD[1:0]	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
2'h0	0	0	0	0	0	0	0	0
2'h1	EVCME0*	0	0	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
2'h2	EVCME1*	0	0	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

Note*: Make sure to write "1" to EVCME0, EVCME1.

CALB: When CALB = 1, the FT1509 executes calibration to the internal operation. Set CALB = 1 after power-on reset. The CALB setting is automatically returned to "0".

FT1509 Instruction list

Main category		Sub category		Upper code								Lower code							
Upper index		index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
IR	index			*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status read			L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
0*	Display control(1)	00h	Start oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
			Device code read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		00h	Start oscillation	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
		01h	Driver output control (1)	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
		02h	LCD driving control	0	0	0	0	0	0	B/C	EOR	0							
		03h	Entry mode	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	AM	0	EPF1	EPF0
		04h	Resize control	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
		05h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCREV1	TCREV0
		06h	Edge Enhance	egmode	Avst2	Avst1	Avst0		Adst2	Adst1	Adst0	Dthu1	Dthu0	Dthl1	Dthl0		Dth2	Dht1	Dth0
		07h	Display control (1)	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
		08h	Display control (2)	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
		09h	Display control (3)	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
		0Ah	Display control (4)	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
		0Bh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Ch	RGB display interface control (1)	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
		0Dh	Frame Mark Position	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
		0Eh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		OFh														VSPL	HSPL	EPL	DPL
1*	Power	10h	Power control (1)				SAP		BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	STB

	control	11h	Power control (2)	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
		12h	Power control (3)	0	0	0	VON	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
		13h	Power control (4)	0	0	VDV7	VDV6	VDV35	VDV4	VDV3	VDV2	0	0	0	0	0	0	VDV1	VDV0
		14h-1Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		17h												DCM1	DCM0	DCT3	DCT2	DCT1	DCT0
2*	RAM access	20h	RAM address set (horizontal direction)	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		21h	RAM address set (vertical direction)	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		22h	RAM data write/read	RAM write data(WD17-0)/Read data(RD17-0) bits are transferred via different data bus in different interface operation															
		23h-28h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		29h	Power control (7)	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
		2Ah	EPROM read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		2Bh	Frame rate and color control	16M_EN	Dither	0	0	0	0	0	0	0	0	0	0	0	RC2	RC1	RC0
		2Ch-2Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3*	Gamma control	30h	Gamma control (1)	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
		31h	Gamma control (2)	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
		32h	Gamma control (3)	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
		33h-34h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		35h	Gamma control (4)	PLP13	PLP12	PLP11	PLP10	0	PRP12	PRP11	PRP10	PHP03	PHP02	PHP01	PHP00	0	PRP02	PRP01	PRP00
		36h	Gamma control (5)	0	0	0	VRP14	VRP13	VRP 12	VRP11	VRP10	0	0	0	VRP04	VRP03	VRP02	VRP01	VRP00
		37h	Gamma control (6)	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
		38h	Gamma control (7)	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
		39h	Gamma control (8)	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
		3Ah-3Bh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		3Ch	Gamma control (9)	PLN13	PLN12	PLN11	PLN10	0	PRN12	PRN11	PRN10	PHN03	PHN02	PHN01	PHN00	0	PRN02	PRN01	PRN00
		3Dh	Gamma control (10)	0	0	0	VRN14	VRN13	VRN 12	VRN11	VRN10	0	0	0	VRN04	VRN03	VRN02	VRN01	VRN00
		3Eh-3Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Instruction list (continued)

Main category		Sub category		Upper code								Lower code							
Upper index		index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4*		40h-4Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5*	Window address control	50h	Horizontal RAM address start position	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
		51h	Horizontal RAM address end position	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
		52h	Vertical RAM address start position	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
		53h	Vertical RAM address end position	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
		54h-5Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6*	Display control(2) & Base image display control	60h	Driver output control (2)	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
		61h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
		62h-69h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		6Ah	Vertical scroll control	0	0	0	0	0	0	0	VL8	VI7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
		6Bh-6Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7*		70h-7Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8*	Partial image control	80h	Partial image 1 display position	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
		81h	Partial image 1 RAM area start line	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
		82h	Partial image 1 RAM end line	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00

		83h	Partial image 2 display position	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
		84h	partial image 2 RAM area start line	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
		85h	Partial image 2 RAM end line	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
		86h-8Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9*	Panel interface control	90h	Panel interface control (1)	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
		91h	Setting disabled	0	0	0	0	0	EQI2	EQI1	EQI0	0	0	0	0	0	SDTI2	SDTI1	SDTI0
		92h	Panel interface control (2)	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
		93h-94h	Setting disabled	0	0	0	0	0											
		95h	Panel interface control (4)	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
		96h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		97h	Setting disabled	0	0	0	0	NOE3	NOE2	NOE1	NOE0	0	0	0	0	0	0	0	0
		98-9Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A*	EPROM control	A0h	EPROM control (1)	0	0	0	0	0	0	0	0	TE	0	EOP1	EOP0	0	0	EAD1	EAD0
		A1h	EPROM control (2)	0	0	0	0	0	0	0	0	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
		A2h	VCN_En	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Vcn_En
		A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
		AE	EPROM read	EVCM4	EVCM3	EVCM2	EVCM1	EVCM0	EVCM14	EVCM13	EVCM1	EVCM11	EVCM10	EVCME0	EVCME1	UID3	UID2	UID1	UID0
		A3h,A5-AFh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		2Ah	EPROM read	0	0	0	0	0	0	0	0	EVCME1	0	EVCM11[5]	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]
C*	CABC control register	C0h		0	0	0	PWMWM	0	0	DBLS1	DBLS0	0	0	0	LEDONR	0	0	0	DBLENABLE
		C1h		0	0	0	0	0s	Per_Iss2	Per_Iss1	Per_Is0	0	0	NUM_TH5	NUM_TH4	NUM_H 3	NUM_TH2	NUM_TH1	NUM_TH0
		C2h		0	0	0	V_MODE	0	TAV2	TAV1	TAV0	TAV_ADAPT7	TAV_ADAPT6	TAV_ADAPT5	TAV_ADAPT4	TAV_ADAPT3	TAV_ADAPT2	TAV_ADAPT1	TAV_ADAPT0
		C3h		0	0	K_5	K_4	K_3	K_2	K_1	K_0	0	0	TH_LOW5	TH_LOW4	TH_LOW3	TH_LOW2	TH_LOW1	TH_LOW0
		C4h		PWD_REG27	PWD_REG26	PWD_REG25	PWD_REG24	PWD_REG23	PWD_REG22	PWD_REG21	WD_RE20	PWD_REG17	PWD_REG16	PWD_REG15	PWD_REG14	PWD_EG13	PWD_REG12	PWD_REG11	PWD_REG10
		C5h		PWD_REG47	PWD_REG46	PWD_REG45	PWD_REG44	PWD_REG43	PWD_REG42	PWD_REG41	WD_RE40	PWD_REG37	PWD_REG36	PWD_REG35	PWD_REG34	PWD_EG33	PWD_REG32	PWD_REG31	PWD_REG30
		C6h		PWD_REG67	PWD_REG66	PWD_REG65	PWD_REG64	PWD_REG63	PWD_REG62	PWD_REG61	WD_RE60	PWD_REG57	PWD_REG56	PWD_REG55	PWD_REG54	PWD_EG53	PWD_REG52	PWD_REG51	PWD_REG50
		C7h		0	0	0	0	0	0	0	0	PWD_REG77	PWD_REG76	PWD_REG75	PWD_REG74	PWD_EG73	PWD_REG72	PWD_REG71	PWD_REG70
		C8h		0	0	0	0	0	0	0	0	DBCV7	DBCV6	DBCV5	DBCV4	DBCV3	DBCV2	DBCV1	DBCV0
		C9h		MBSD7	MBSD6	MBSD5	MBSD4	MBSD3	MBSD2	MBSD1	MBSD0	LABC7	LABC6	LABC5	LABC4	LABC3	LABC2	LABC1	LABC0
		CAh		0	0	0	0	0	0	0	0	PWMDIV7	PWMDIV6	PWMDIV5	PWMDIV4	PWMDIV3	PWMDIV2	PWMDIV1	PWMDIV0
		CBh		0	0	0	0	0	0	OUTSEL1	OUTSEL	0	0	0	0	0	0	0	LEDPWMPOL

Reset Function

The FT1509 is initialized by the RESET input. During reset period, the FT1509 is in a busy state and instruction from the MPU and GRAM access are not accepted. The FT1509's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 10 ms). During this period, GRAM access and initial instruction setting are prohibited.

1. Initial state of instruction bits (default)

See the instruction tables. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (D1-0 = “00”).

3. Output pin initial state (see note)

1. LCD driver S1~S720	: GND
G1~G320	: VGL (= GND)
2. Vcom	: GND
3. VcomH	: Vci
4. VcomL	: GND
5. VREG1OUT	: VGS
6. VciOUT	: Hi-z
7. DDVDH	: Vci
8. VGH	: DDVDH (= Vci)
9. VGL	: GND
10. VCL	: GND
11. FMARK	: Halt (GND output)
12. Oscillator	: Oscillate
13. SDO	: High-level (IOVcc) when IM[3:1]=010(serial interface),
	: Hi-z when IM[3:1]<>010(other than serial interface).

4. Initial state of input/output pins* see Note

1. C11A	: Hi-z
2. C11B	: Hi-z
3. C12A	: Hi-z
4. C12B	: Hi-z
5. C13A	: Vci1 (= Hi-z)
6. C13B	: GND
7. C21A	: DDVDH (= Vci)
8. C21B	: GND
9. C22A	: DDVDH (= Vci)
10. C22B	: GND
11. VDD	: 1.7v

Note: The initial states of output and input pins become the state mentioned above when the FT1509’s power supply circuit is connected as exemplified in “Connection example”.

5. Note on Reset function

- When a RESET input is entered into the FT1509 while it is in deep standby mode, the FT1509 starts up the internal logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable. For this reason, do not enter a RESET input in deep standby mode.
- When transferring instruction and data in either two or three transfers via 8-/9-/16-bit interface, make sure to execute data transfer synchronization after reset operation.

Interface and data format

The FT1509 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The FT1509 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the FT1509 supports VSYNC interface, which enables data rewrite operation without flickering the moving picture on display.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The FT1509 operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register. When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 53

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still picture)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes: 1. Instructions are set only via system interface.

2. The VSYNC interfaces cannot be used simultaneously.
3. See “External Display Interface” section for sequences switching from one mode to another.

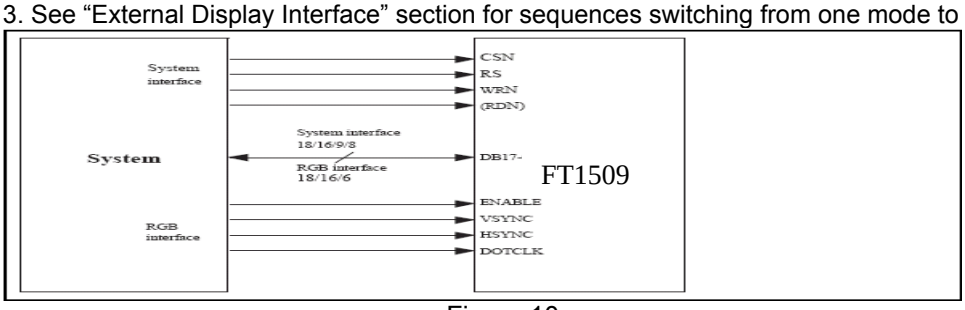


Figure 10

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator’s clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the FT1509 to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the “VSYNC Interface” section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display periods (NL) are automatically calculated from the frame synchronous signal (VSYNC) in FT1509 according to the instruction setting for these periods.

System Interface

The following kinds of system interface are available with the FT1509 and the interface is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 54 IM bits settings and system interface

IM2	IM1	IM0	Interface operation	DB Pins
0	0	0	80-system 18-bit interface	DB17-DB0-
0	0	1	80-system 9-bit interface	-

0	1	0	80-system 16-bit interface	DB17-10, DB8-1
0	1	1	80-system 8-bit interface	DB17-10
0	1	1	Clock synchronous serial interface	SDI/SDO
1	0	ID	Setting disabled	-
1	1	1	Setting disabled	-

Note 1: 65,536 colors in 1 transfer, 262,144 colors in 2 transfers
Note 2: 65,536 colors in 2 transfers, 262,144 colors in 3 transfers
Note 3: 'Setting disabled' option is operating under 80-system 18-bit interface.

80-system 18-bit interface

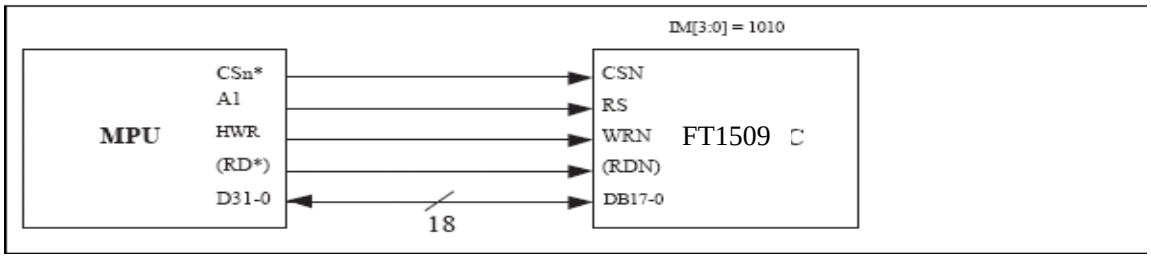


Figure 11

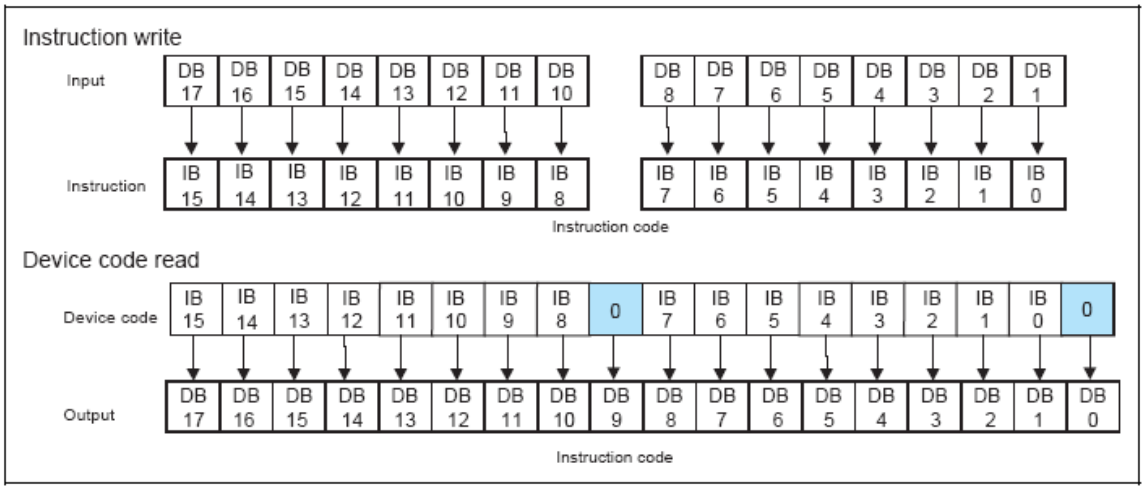


Figure 12: Instruction/Device code read (18-bit interface)

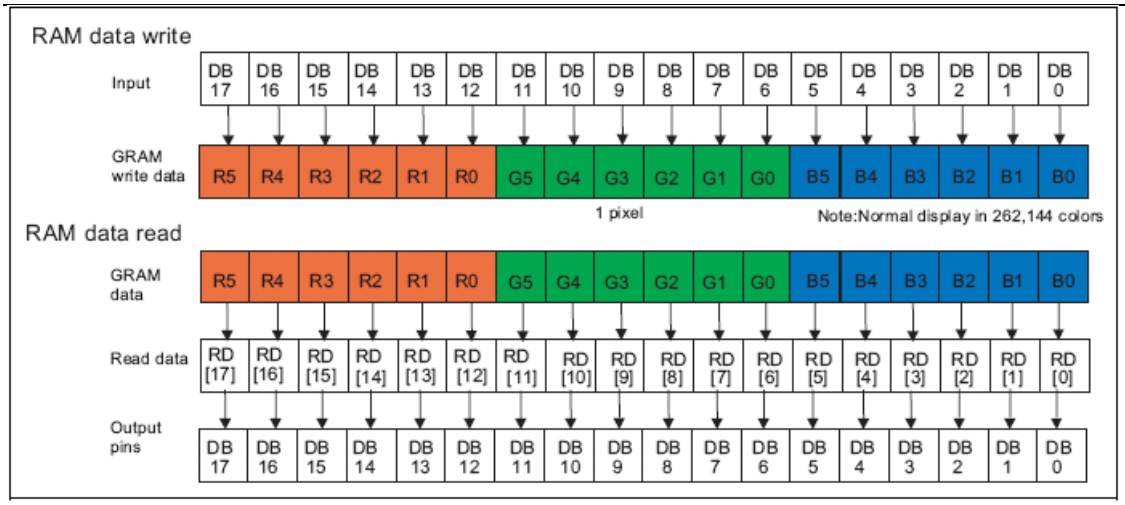


Figure 13: RAM data write/read (18-bit interface)

80-system 16-bit interface

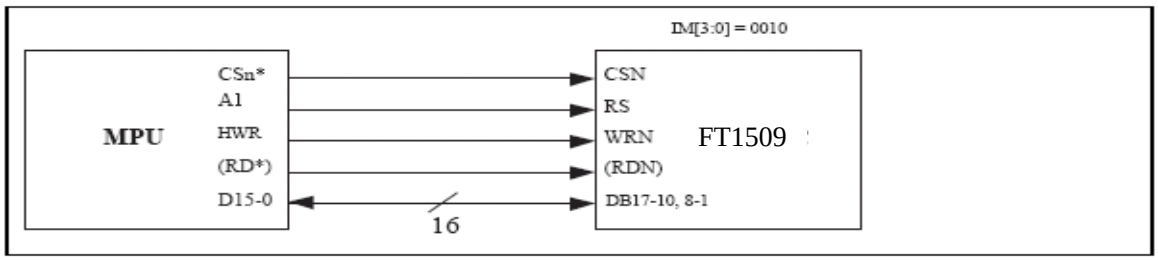


Figure 14

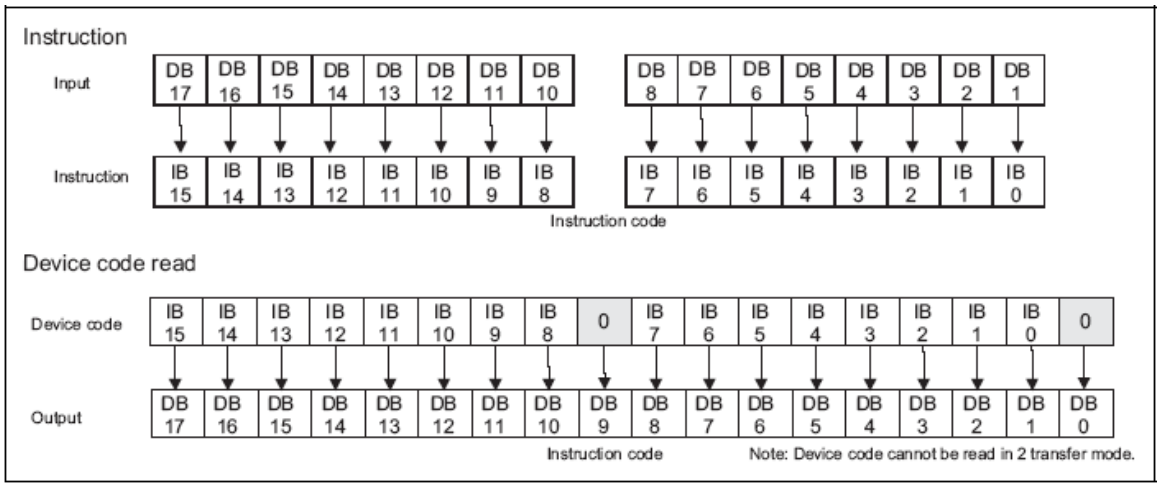


Figure 15: Instruction/Device code read (16-bit interface)

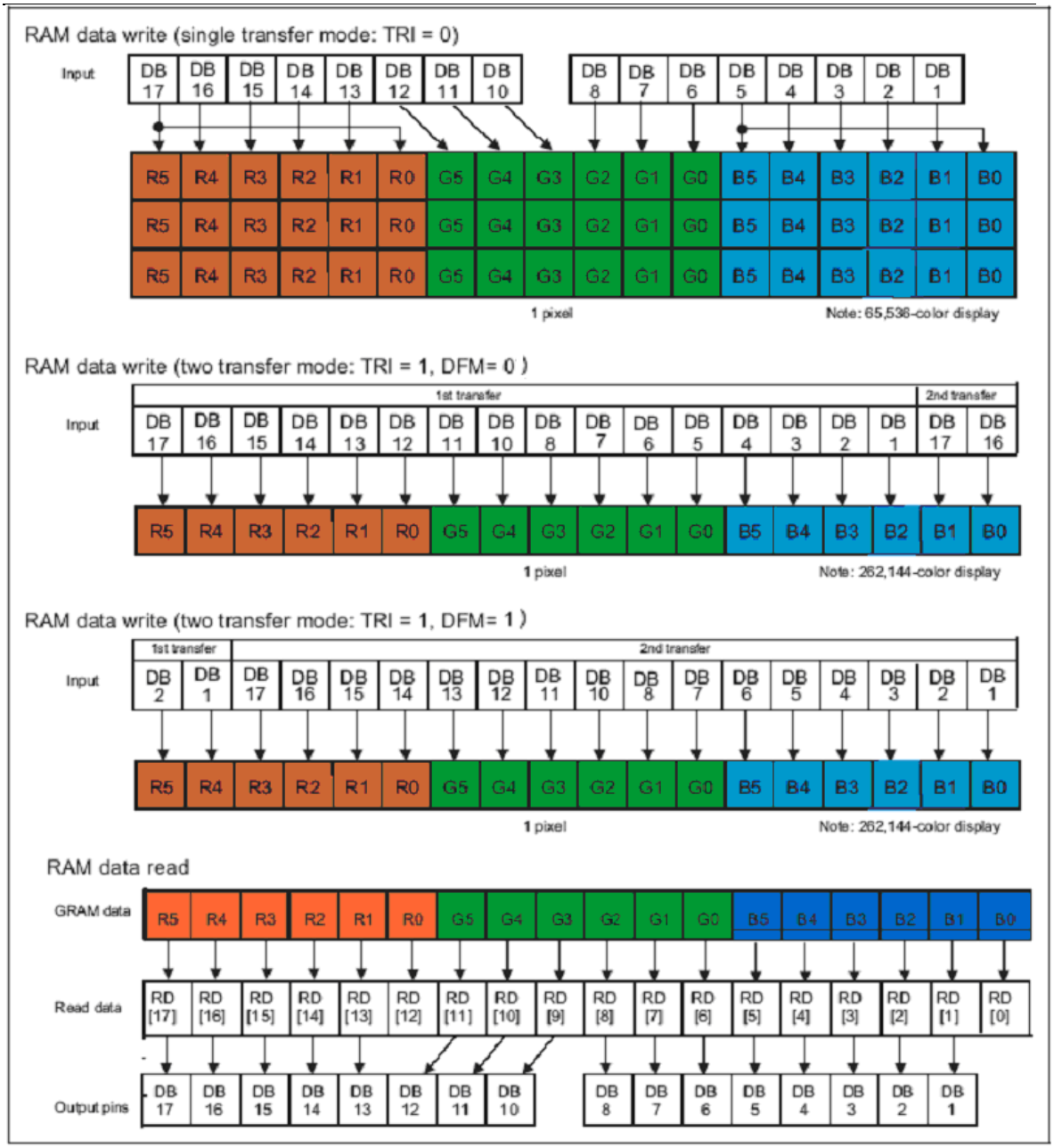


Figure 16: RAM data write/read (16-bit interface)

80-system 9-bit interface

When transferring 16-bit instruction via 9-bit interface (DB17~DB9), it is divided into upper and lower 8 bits (DB9 is not used) and the upper 8 bits are transferred first. The RAM write data are divided into upper and lower 9 bits and the upper 9 bits are transferred first. The unused DB8-0 pins must be fixed at either IOVcc or GND level. When writing in the index register, make sure to write the upper byte (8 bits).

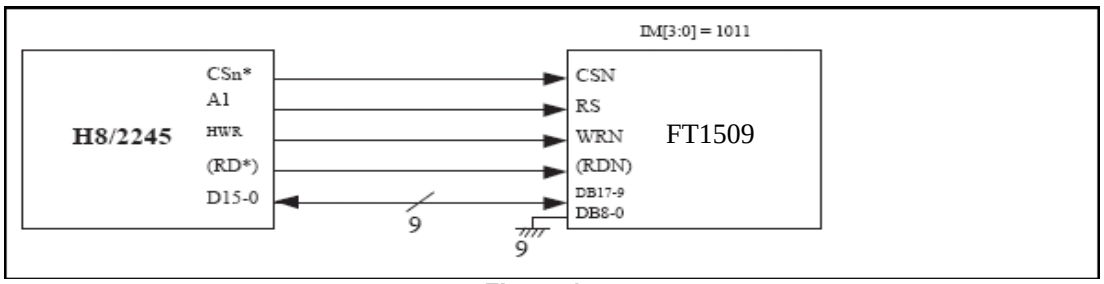


Figure 17

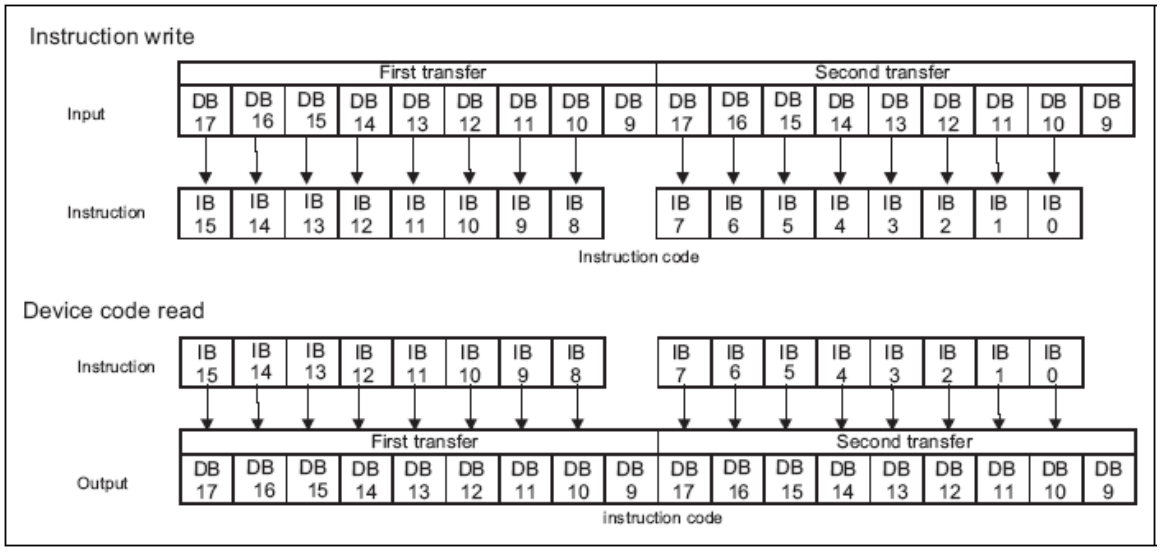


Figure 18: Instruction/Device code read (9-bit interface)

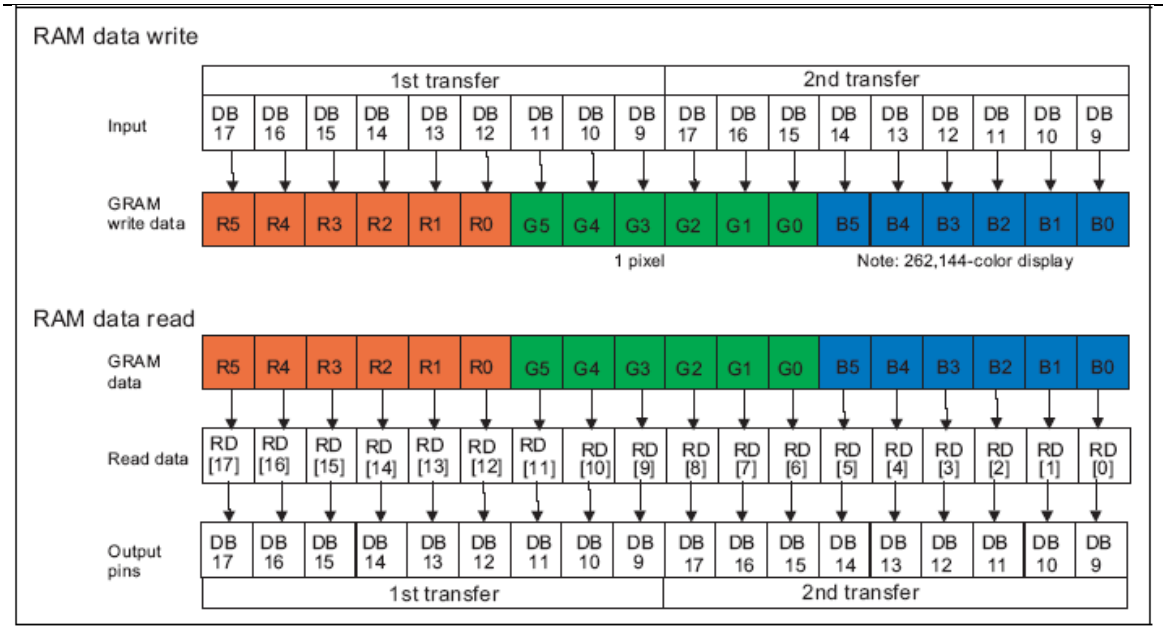


Figure 19: RAM data write/read (9-bit interface)

The FT1509 supports data transfer synchronization function to reset the counters, which count the number of upper and lower 9 bits when transferring data via 9-bit bus interface. If a mismatch occurs in transferring upper and lower 9 bits due to noise and so on, “00”H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 9 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

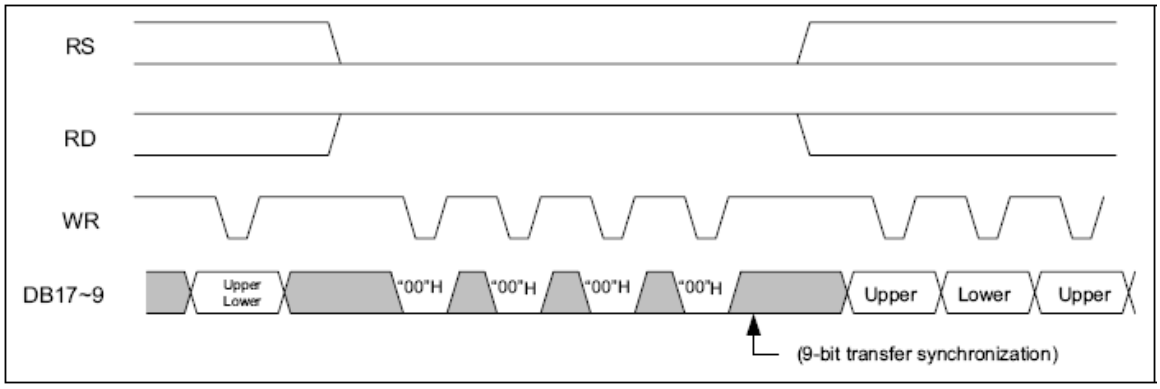


Figure 20: Data transfer synchronization (9-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

80-system 8-bit interface

When transferring 16-bit instruction via 8-bit interface (DB17~DB10), it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The RAM write data are divided into upper and lower 8 bits and the upper 8 bits are transferred first. The unused DB9-0 pins must be fixed at either IOVcc or GND level. When writing in the index register, make sure to write the upper byte (8 bits).

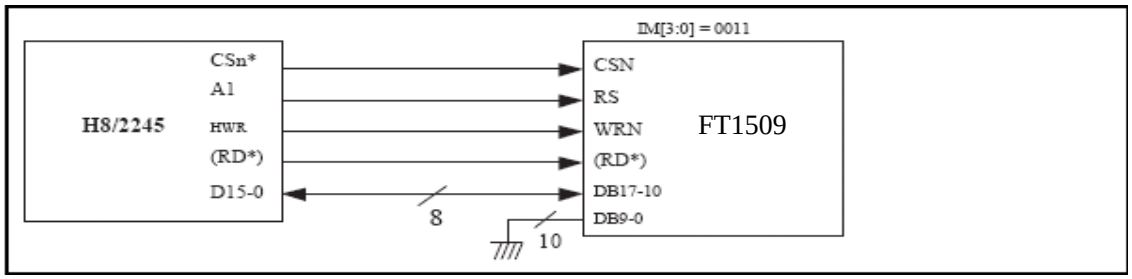
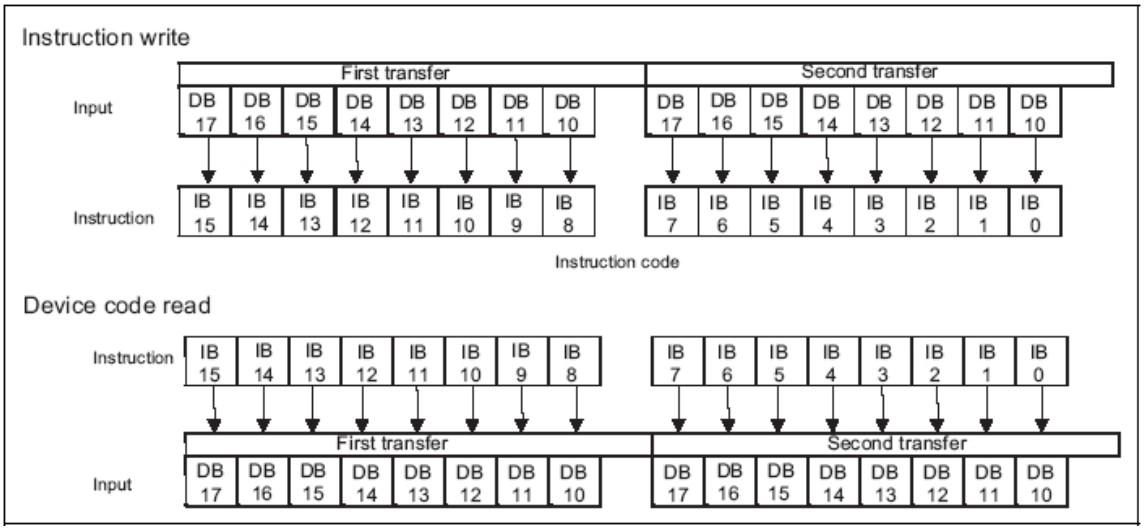
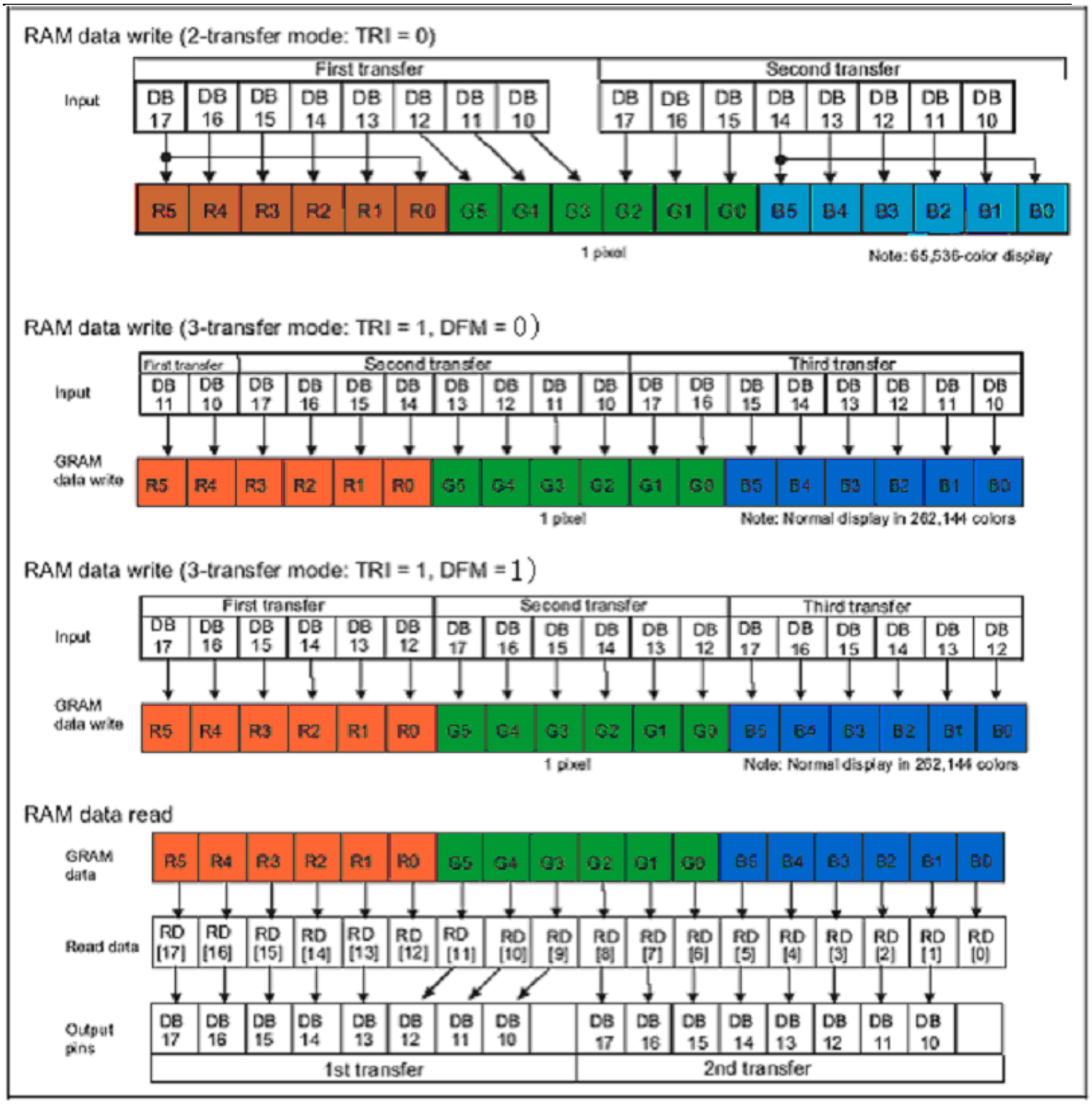


Figure 21



Note: Data cannot be read in 3-transfer mode.

Figure 22: Instruction/Device code read (8-bit interface)



Note: Data cannot be read in 3-transfer mode.

Figure 23: RAM data write/read (8-bit interface)

The FT1509 supports data transfer synchronization function to reset the counters, which count the number of upper and lower 8 bits when transferring data via 8-bit bus interface. If a mismatch occurs in transferring upper and lower 8 bits due to noise and so on, “00”H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 8 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

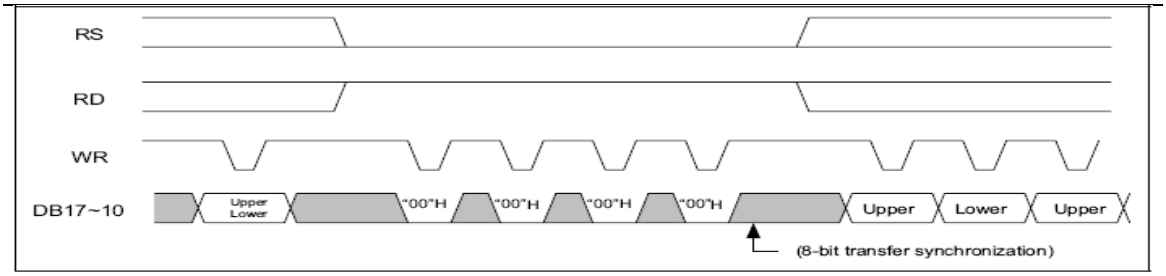


Figure 24: Data transfer synchronization (8-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

Serial interface

The serial interface is selected by setting the IM3/2/1 pins to GND/IOVcc/GND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The FT1509 recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The FT1509 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the FT1509 are compared and both 6-bit data match. Then, the FT1509 starts taking in subsequent data. The least significant bit of the device identification code is determined by setting the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the FT1509 because the seventh bit of the start byte is register select bit (RS). When RS = 0, either index register write or status read operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The FT1509 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The FT1509 writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the FT1509 starts transferring or receiving data in units of bytes. The FT1509 transfers data from the MSB. The FT1509's instruction consists of 16 bits and it is executed inside the FT1509 after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The FT1509 expands RAM write data into 18 bits when writing them to the internal GRAM. The first byte received by the FT1509 following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the GRAM, valid data is not transferred to the data bus until first five bytes of data are read from the GRAM following the start byte. The FT1509 sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 55 Start Byte Format

Transferred bits	**S**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1		1	1	0	ID	

Note: The ID bit is selected by setting the IM0/ID pin.

Table 56

RS	R/W	Function
0	0	Set index register
0	1	Read status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

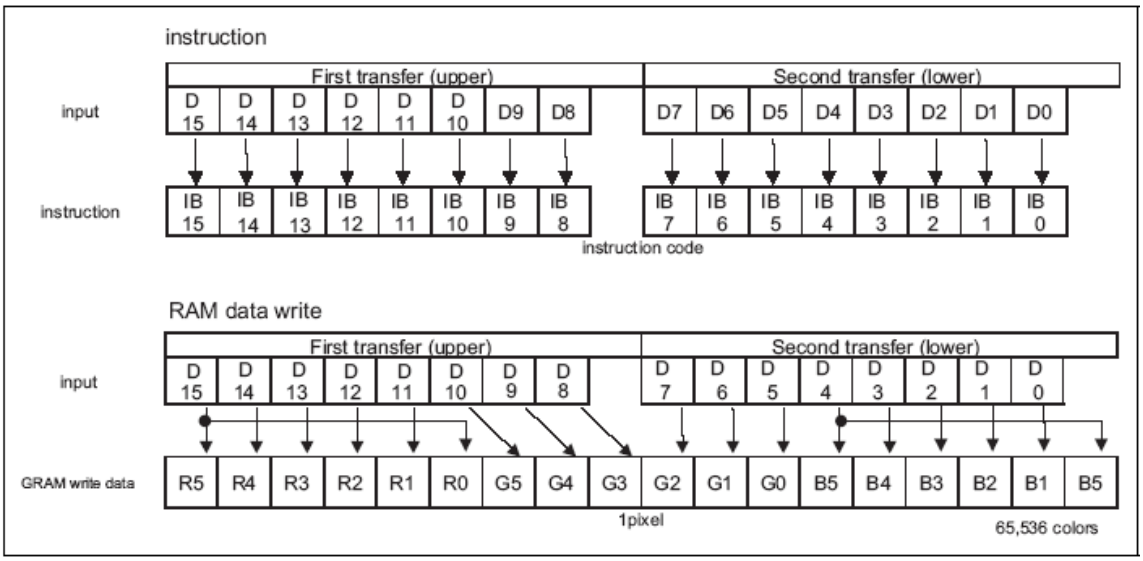


Figure 25

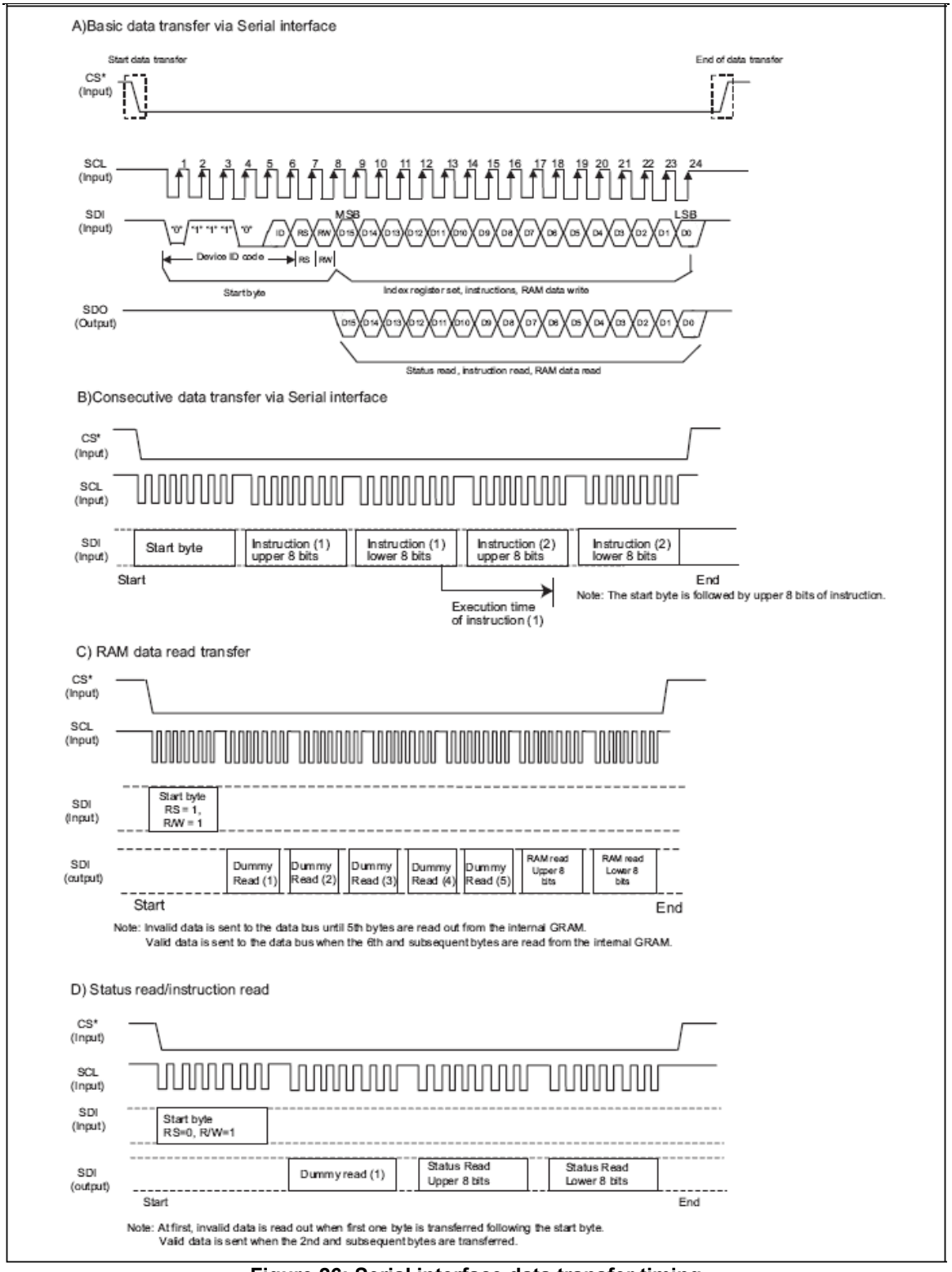


Figure 26: Serial interface data transfer timing

VSYNC Interface

The FT1509 supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

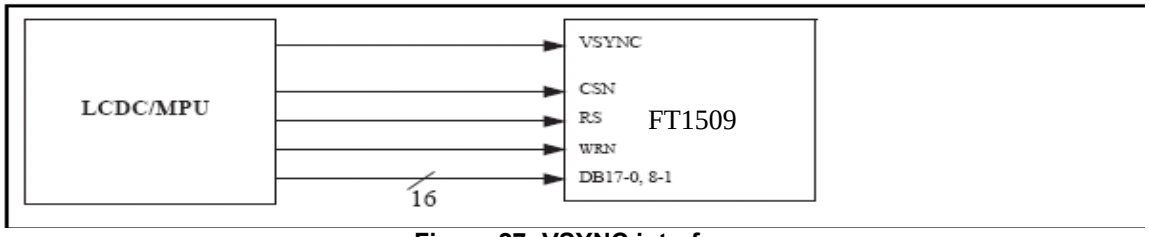


Figure 27: VSYNC interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the FT1509 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

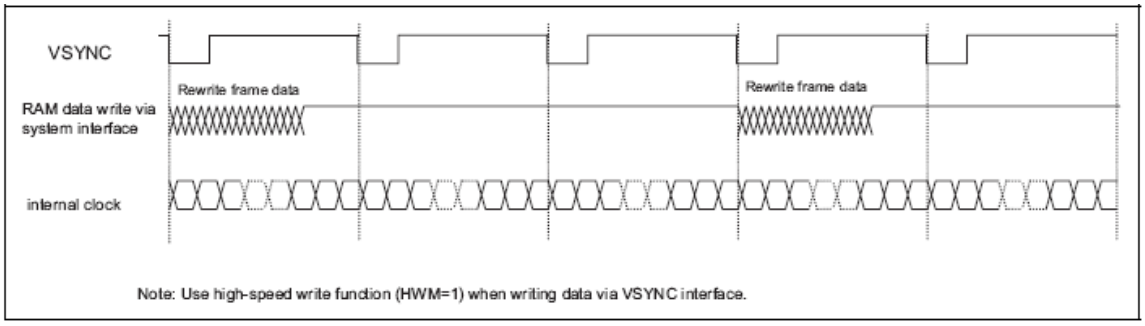


Figure 28: Moving picture data write via VSYNC

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$Internal\ clock\ frequency\ (fosc)\ [Hz]$$
$$= FrameFrequency \times (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) \times 16(clocks) \times variance$$

$$RAMWriteSpeed(\min.)[Hz] > \frac{240 \times DisplayLines(NL)}{(BackPorch(BP) + DisplayLines(NL) - margins) \times 16(clocks) \times \frac{1}{fosc}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface

operation is as follows.

Notes: 1. When setting the internal clock/oscillator frequency (through register RC[2:0]), possible causes of fluctuation must also be taken into consideration. In this example, the internal clock/oscillator frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz] > 240 × 320 / {((14 + 320 - 2) lines × 16 clock) /394 kHz} = 5.7 MHz

Notes: 1. In this example, it is assumed that the FT1509 starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the FT1509 has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 5.7MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the FT1509 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

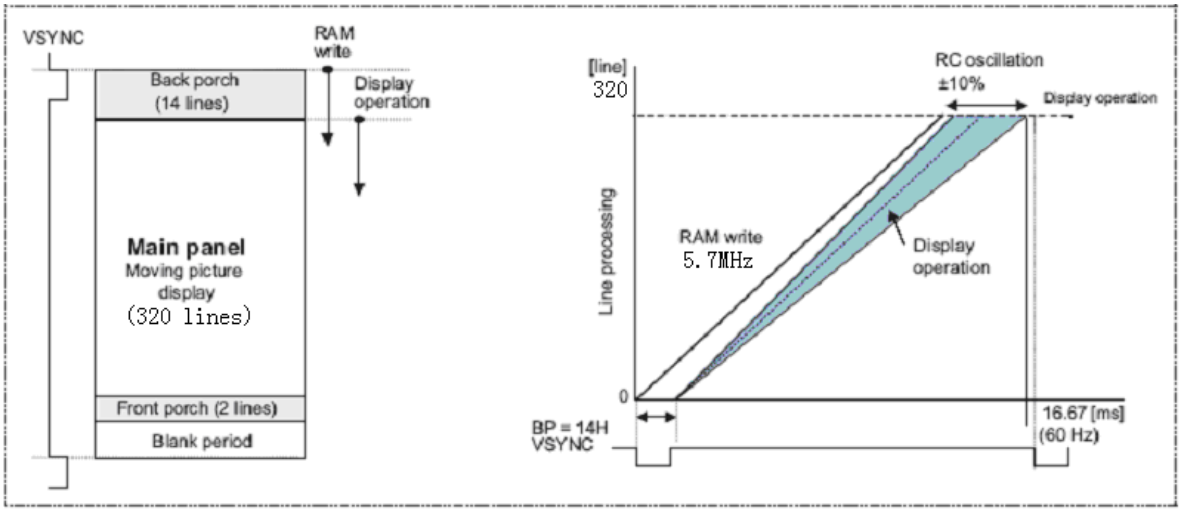


Figure 29: Write/display operation timing via VSYNC interface

Notes to VSYNC Interface operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margins in setting RAM write speed for VSYNC interface operation.
2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

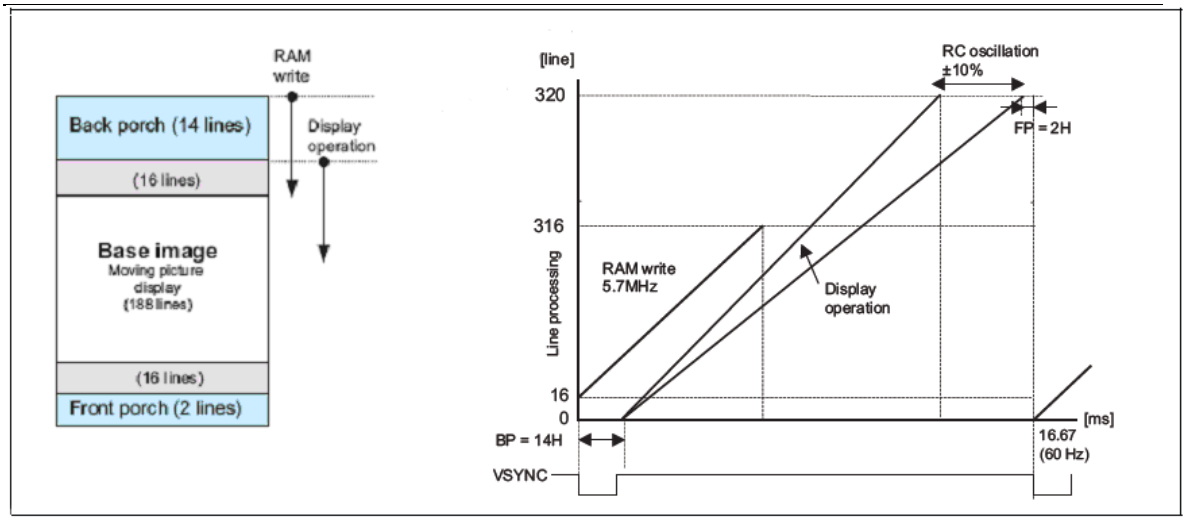


Figure 30: RAM write speed margin

3. The front porch period continues from the end of one frame period to the next VSYNC input.
4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.
5. The partial display and vertical scroll functions and interlaced scan are not available in VSYNC interface operation.
6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.

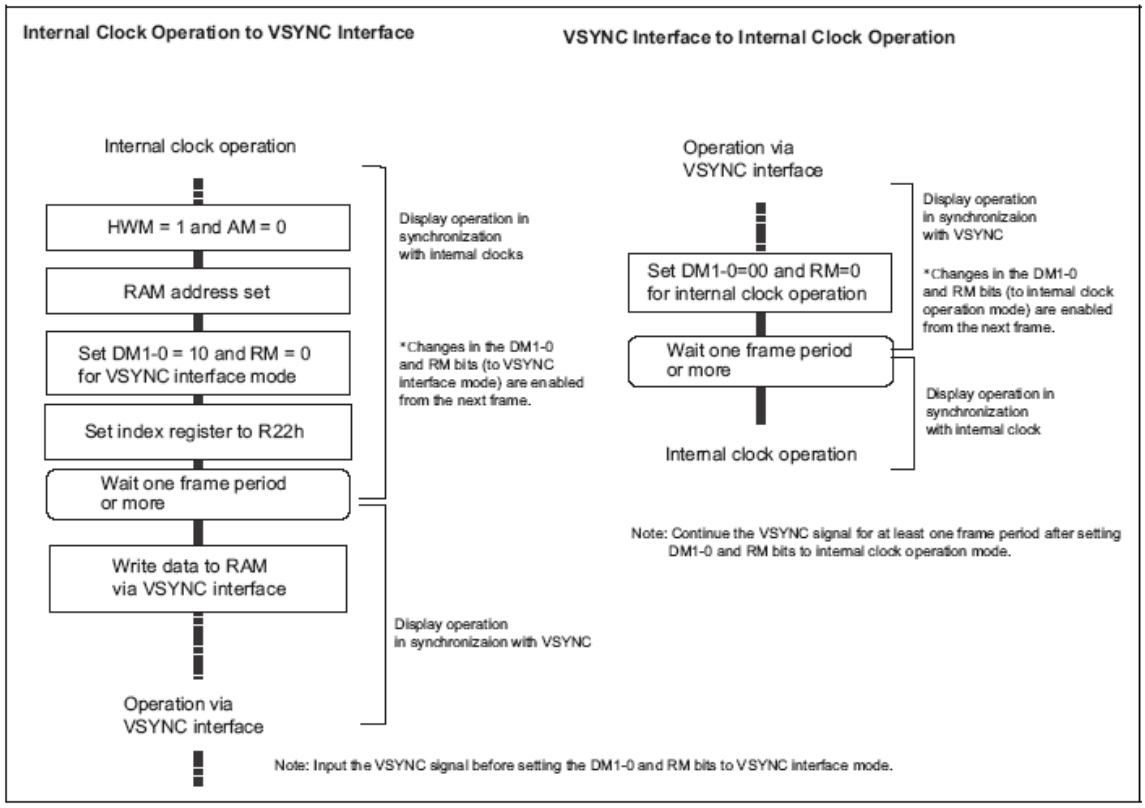


Figure 31: Sequence to switch between VSYNC and Internal clock operation modes

ENABLE signal function

The following table shows the relationship between the ENABLE, EPL setting and RAM access operation. Whenever the FT1509 performs write operation, ENABLE must be “Low” to allow write operation but this is not the determinant of enabling automatic address update in RAM write operation. EPL controls the active polarity of ENABLE signal.

Table 58

EPL	ENABLE	RAM write	RAM address
0	0	Enable	Update
0	1	Disable	Retain
1	0	Disable	Retain
1	1	Enable	Update

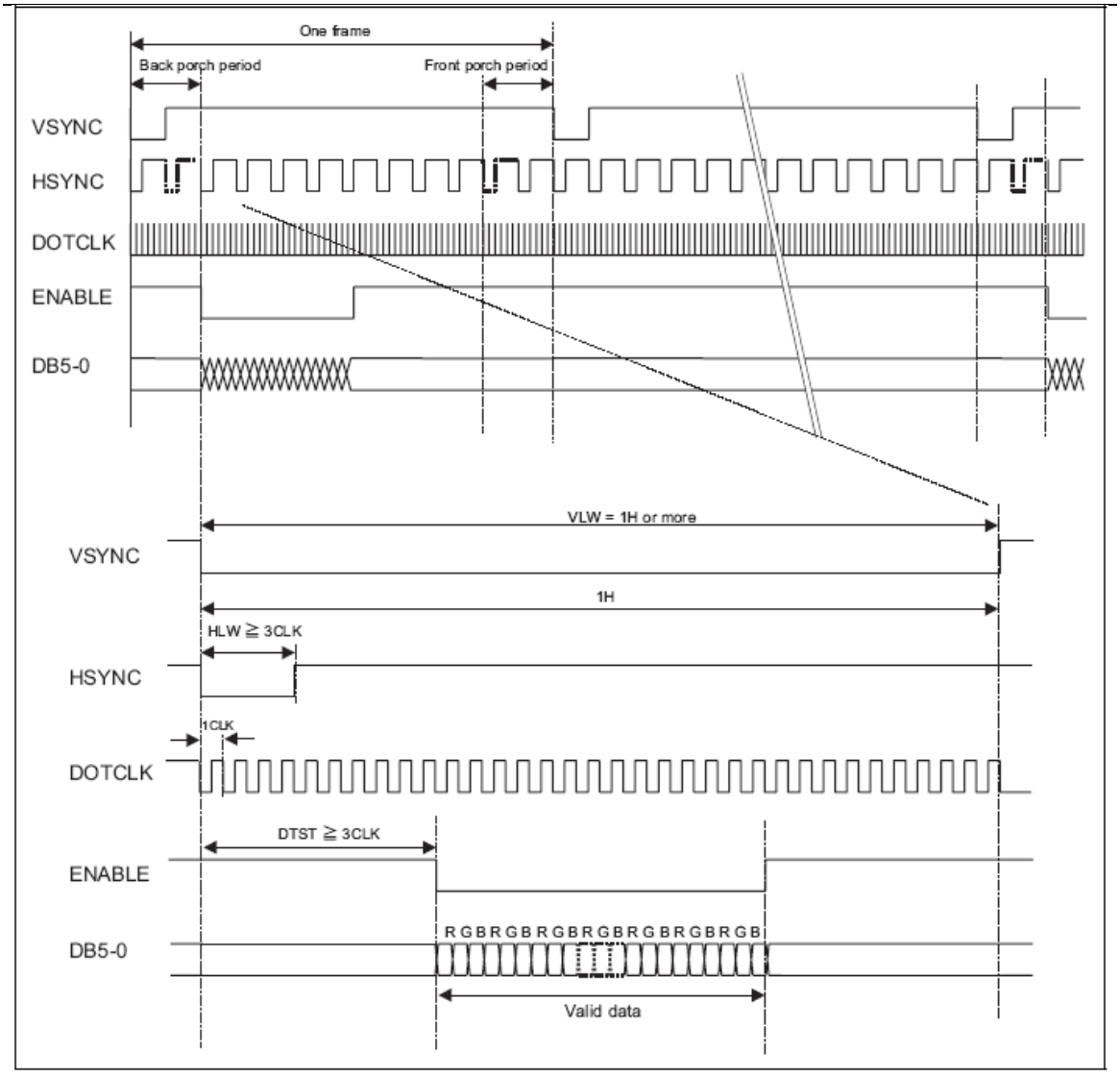


Figure 34

Notes 1: VLW: VSYNC “Low” period HLW: HSYNC “Low” period DTST: data transfer setup time

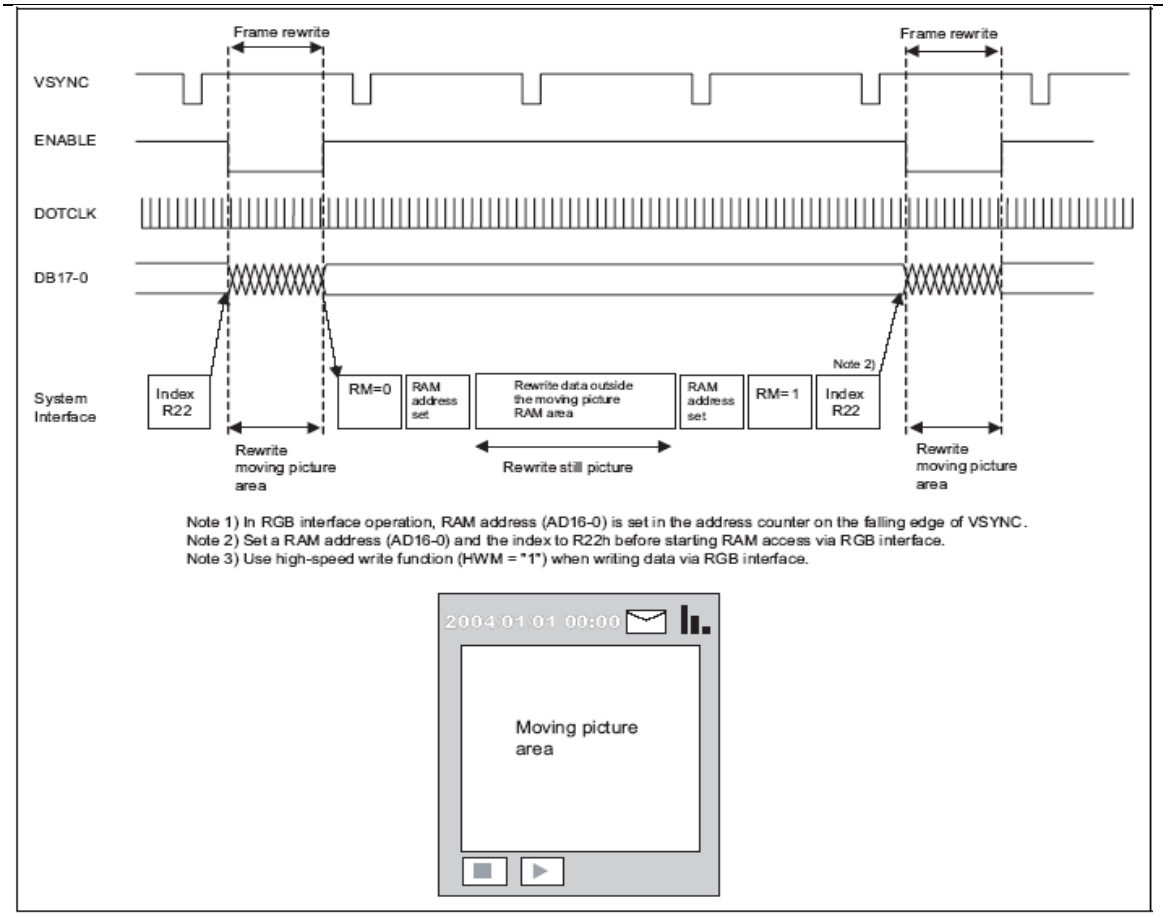


Figure 35: Updating a still picture area while displaying a moving picture

1. The following functions are not available in external display interface operation.

Table 59 Functions Not Available in External Display Interface operation

Function	External Display Interface	Internal Clock Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.

RAM Address and Display Position on the Panel

The FT1509 has memory to store display data of 240RGB x 320 lines. The FT1509 incorporates a circuit to control partial display, which allows switching driving methods between full-screen display mode and partial display mode.

The FT1509 makes display design setting and panel driving position control setting separately and specifies RAM area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image by setting PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

   Normal display BASEE = 1
   Partial display BASEE = 0, PTDE0/1 = 1

5. Change BASEE, PTDE0/1 setting to switch display modes (full-screen and partial display modes).

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing RAM data.

Table 60

	Display ENABLE	**Numbers of lines**	**RAM area**
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h0DB)

Notes 1: The base image is displayed from the first line of the panel.
2: Make sure NL ≤ 320 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h0DB, respectively.

Table 61

	Display ENABLE	**Display position**	**RAM area**
Partial image 1	PTDE0	PTDP0	(PTSA0, PTEA0)
Partial image 2	PTDE1	PTDP1	(PTSA1, PTEA1)

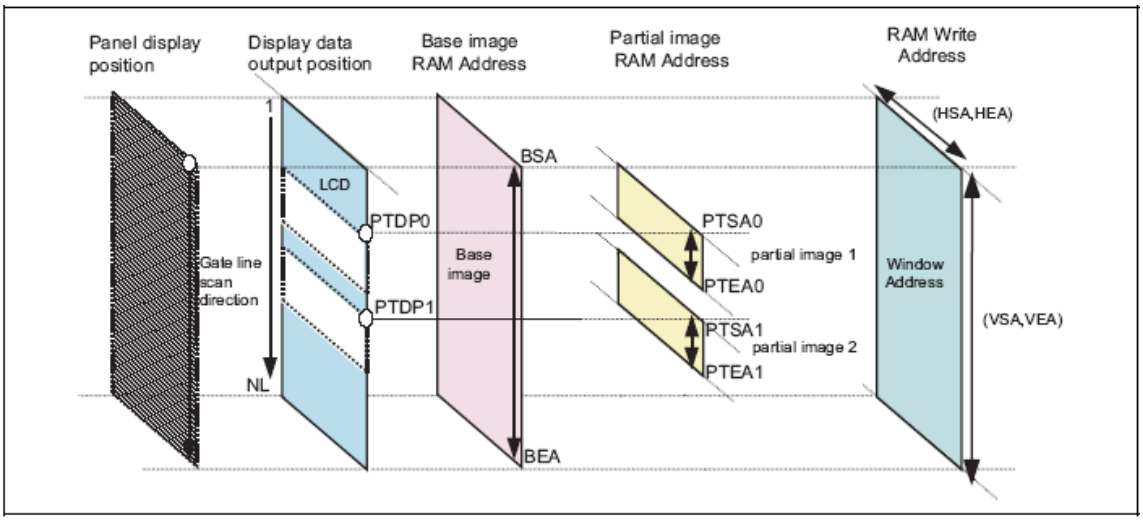


Figure 41: RAM Address, display position and drive position

Restrictions in setting display control instruction

Partial image display
Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partial images can be controlled independently.

$$0 \le PTDP0 \le PTDP0 + (PTEA0 - PTSA0) < PTDP1 \le PTDP1 + (PTEA1 - PTSA1) \le NL$$

The following figure shows the relationship among the RAM address, display position, and the lines

driven for the display.

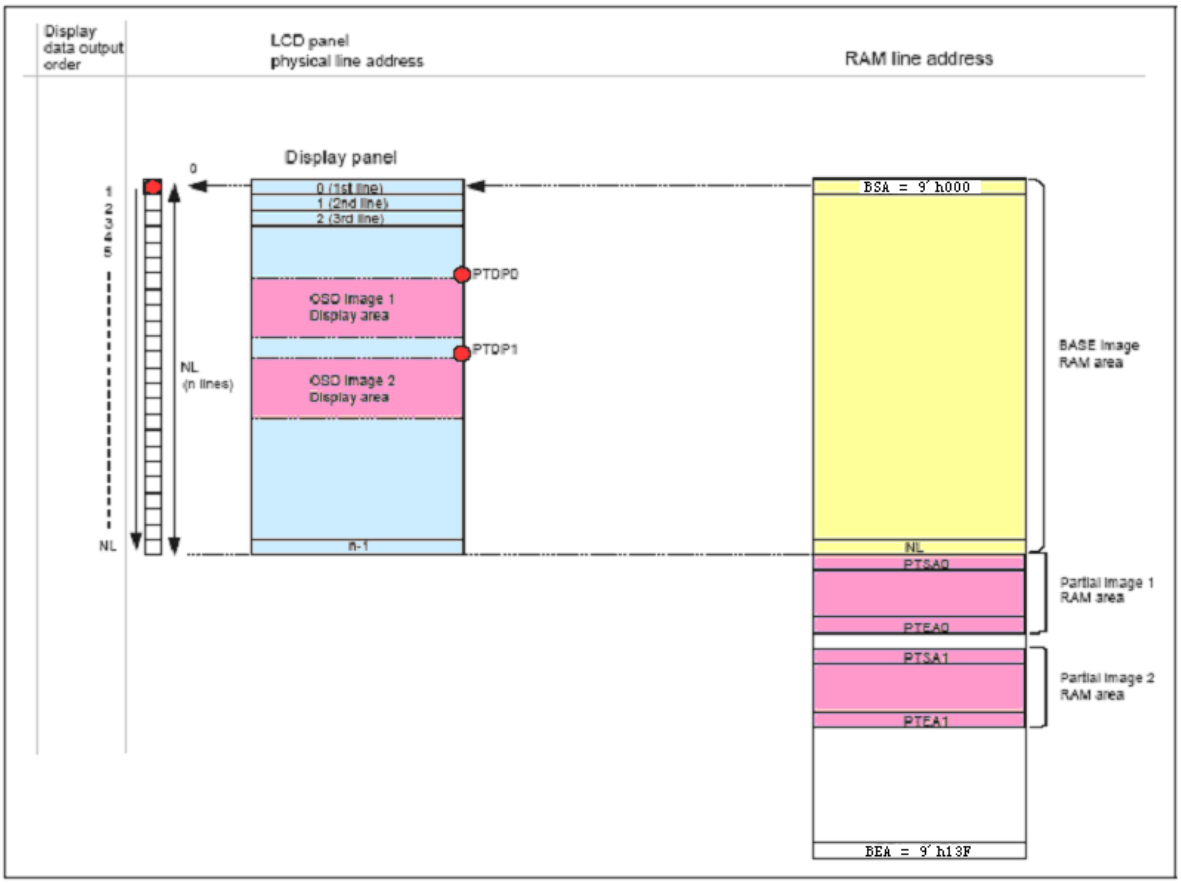


Figure 42: Display RAM address and panel display position

Note: This figure shows the relationship between RAM line address and the display position on the panel. In the FT1509's internal operation, the data is written in the RAM area specified by the window address setting (HEA/HSA[8:0], VEA/VES[8:0]).

Instruction setting example

The followings are examples of display design setting for 240(RGB) x 432(lines) panels.

1. Full screen display (no partial)

The following is an example of full screen display setting.

Table 62

Base image display instruction	
BASEE	1
NL[5:0]	6'h27

PTDE0	0
PTDE1	0

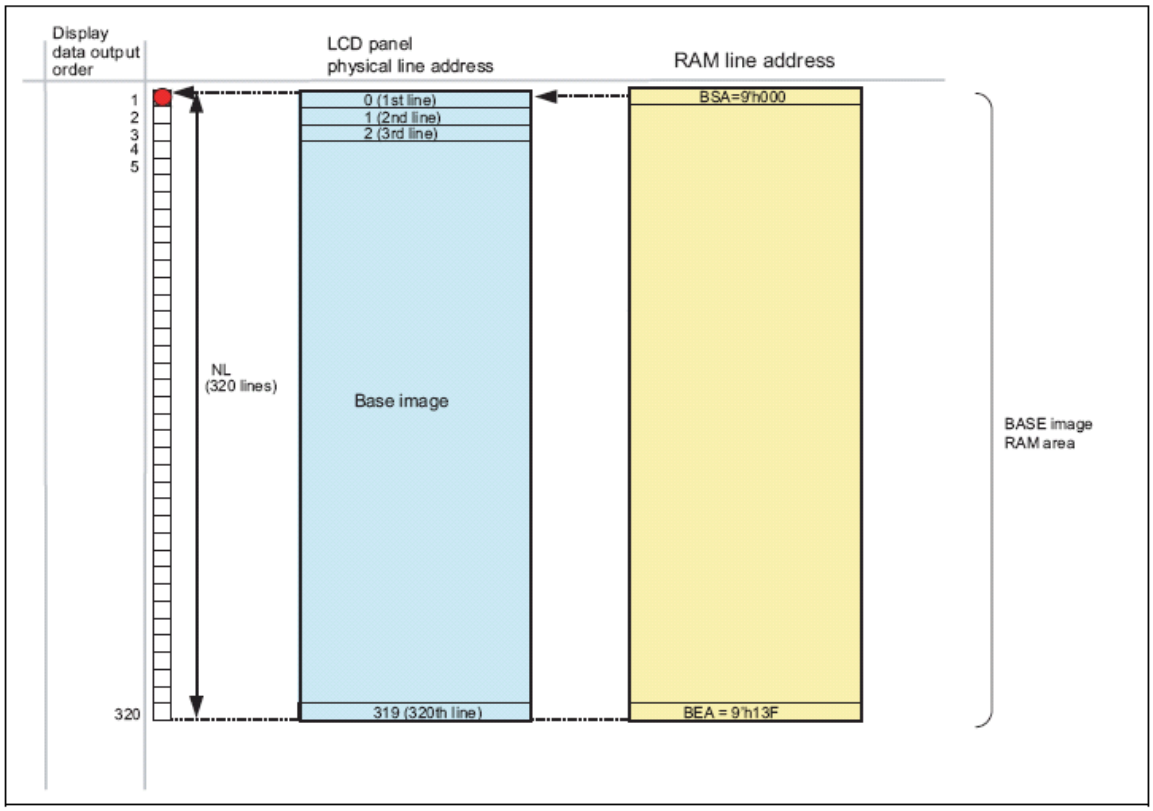


Figure 43: Full screen display (no partial)

2. Partial only

The following is an example of setting for partial image 1 only and turning off the base image. The partial image 1 is displayed at the position specified by PTDP0 bit.

Table 63

Base image display instruction	
BASEE	0
NL[5:0]	6'h27

Partial image 1 display instruction	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h00F
PTDP0[8:0]	9'h080

Partial image 2 display instruction	
PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000

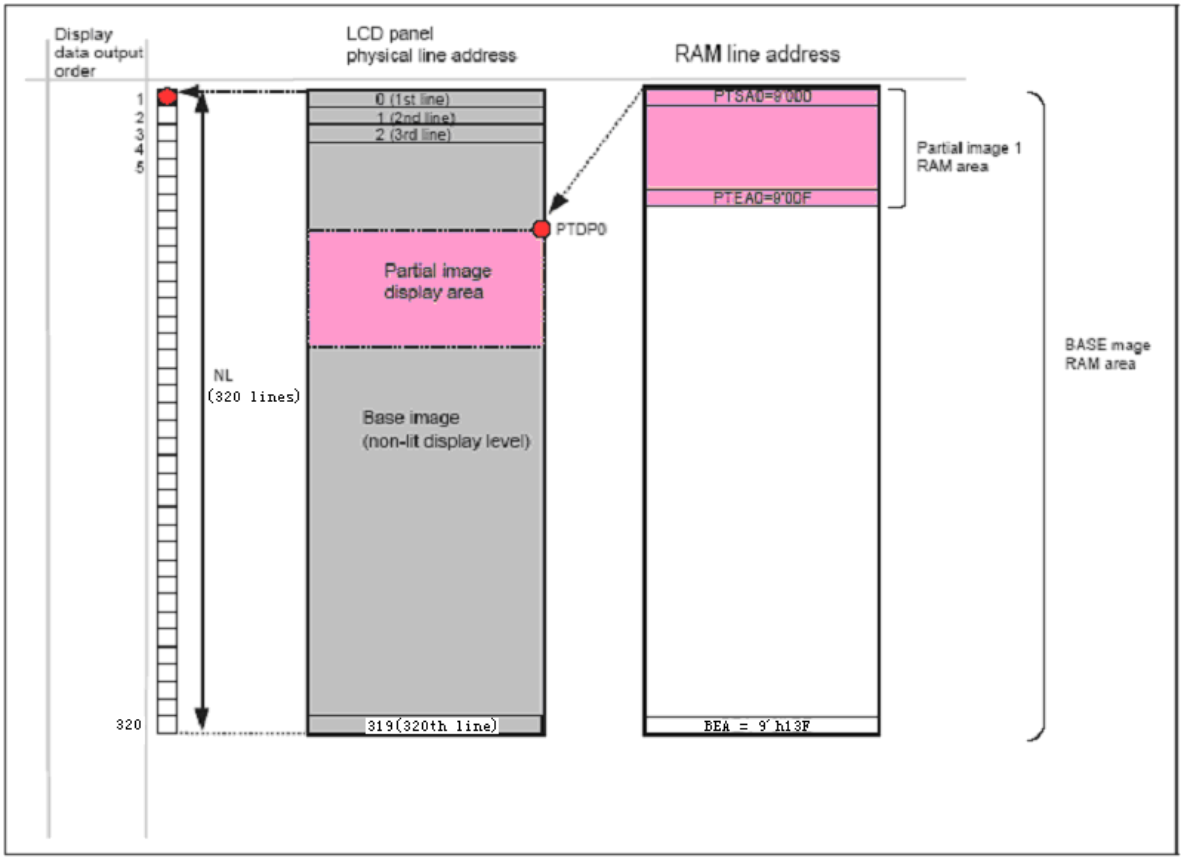


Figure 44: Partial display

Resizing function

The FT1509 supports resizing function (x 1/2, x 1/4), executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit, which sets the contraction factor (x1/2 or x1/4) of the image. This function enables the FT1509 to write the resized

image data （Original resolution < 240*320）directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The FT1509 processes the contraction of an image simply by selecting pixels from original image data. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.

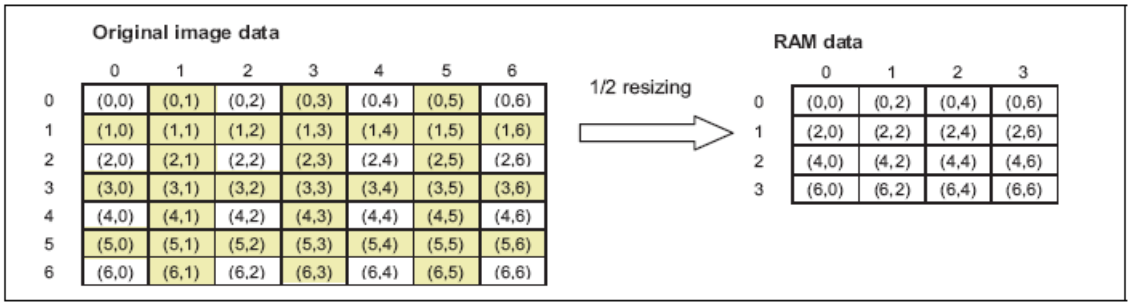


Figure 45: Resizing

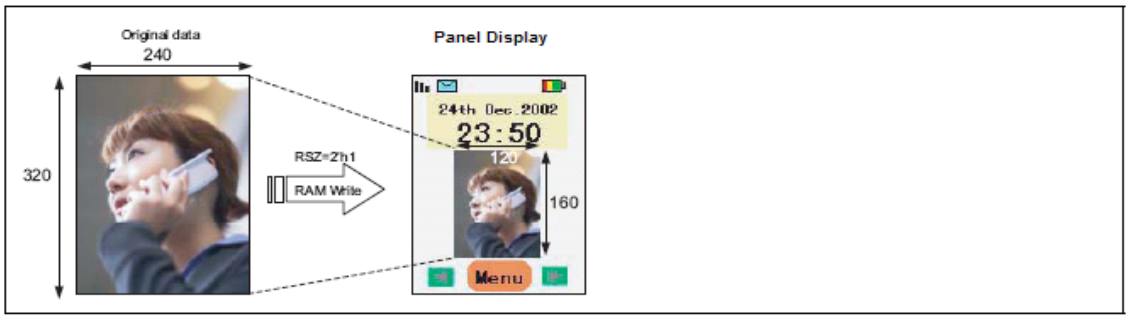


Figure 46: Resizing transfer, display example

Table 64

Original image size (X x Y)	Resized image size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
240x320 (QVGA)	120x160	60x80
176x220 (QCIF)	88x110	44x55
120x160	60x80	30x40
132x176	66x88	33x44

Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

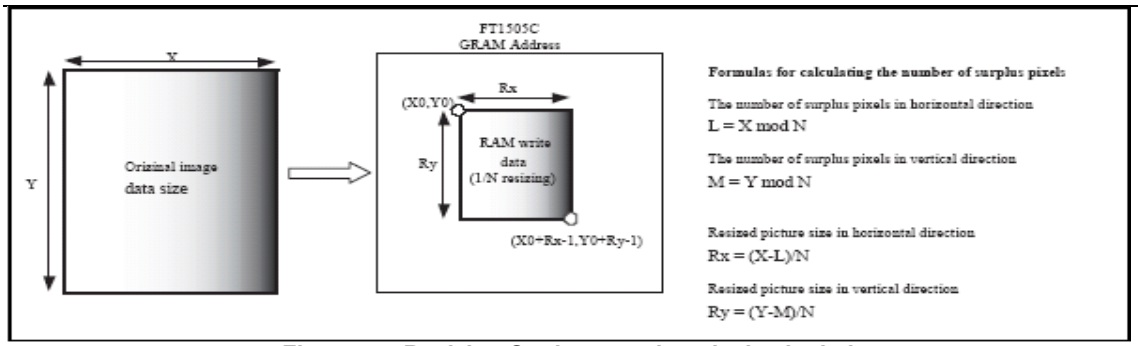


Figure 47: Resizing Setting, surplus pixel calculation

Table 65

Image (before resizing)

Number of data in horizontal direction	X
Number of data in vertical direction	Y
Resizing ratio	1/N

Register setting in the FT1509

Resizing setting	RSZ	N-1
Number of data in horizontal direction	RCV	L
Number of data in vertical direction	RCH	M

RAM writing start address	AD	(X0, Y0)
RAM window address	HSA	X0
	HEA	X0+Rx - 1
	VSA	Y0
	VEA	Y0+Ry - 1

Example of 1/2 resizing

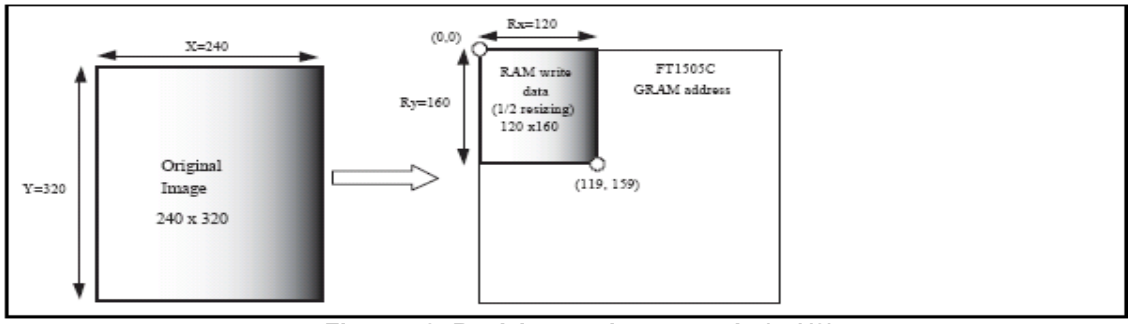


Figure 48: Resizing setting example (x 1/2)

Table 66

Image to transmit

Number of data in horizontal direction	X	176
Number of data in vertical direction	Y	320
Resizing ratio	1/N	1/2

Register setting in the FT1509

Resizing setting	RSZ	2'h1
Number of data in horizontal direction	RCV	2'h0
Number of data in vertical direction	RCH	2'h0

RAM writing start address	AD	17'h00000
RAM window address	HSA	8'h00
	HEA	8'h77
	VSA	9'h000
	VEA	9'h09F

Resizing instruction bits

Table 67 Resizing factor

RSZ[1:0]	Contraction factor
2h'0	No resizing (x 1)
2h'1	1/2 resizing (x 1/2)
2h'2	Setting disabled
2h'3	1/4 resizing (x 1/4)

Table 68 Surplus pixels

Vertical direction 1 pixel = 1 RGB

RCV[1:0]	Surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

horizontal direction 1 pixel = 1 RGB

RCH[1:0]	Surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

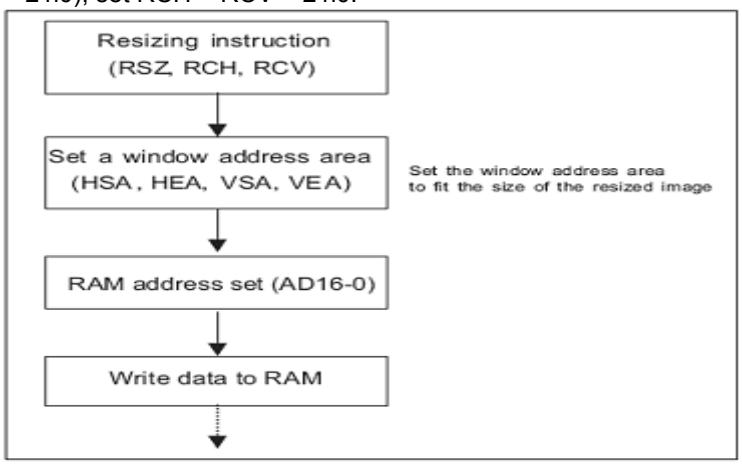


Figure 49: RAM write with resizing

FMARK Function

The F1505 outputs an FMARK pulse when the FT1509 is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

The FMARK output interval is set by FMI[2:0] bits. Set FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. Set FMARKOE = 1 when outputting FMARK pulse from the FMARK pin.

Table 69

FMP[8:0]	FMARK output position
9'h000	0th line
9'h001	1st line
9'h002	2nd line
….	….
9'h14E	334th line
9'h14F	335th line
9'h150~1FF	Setting disabled

Table 70

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

FMP setting example

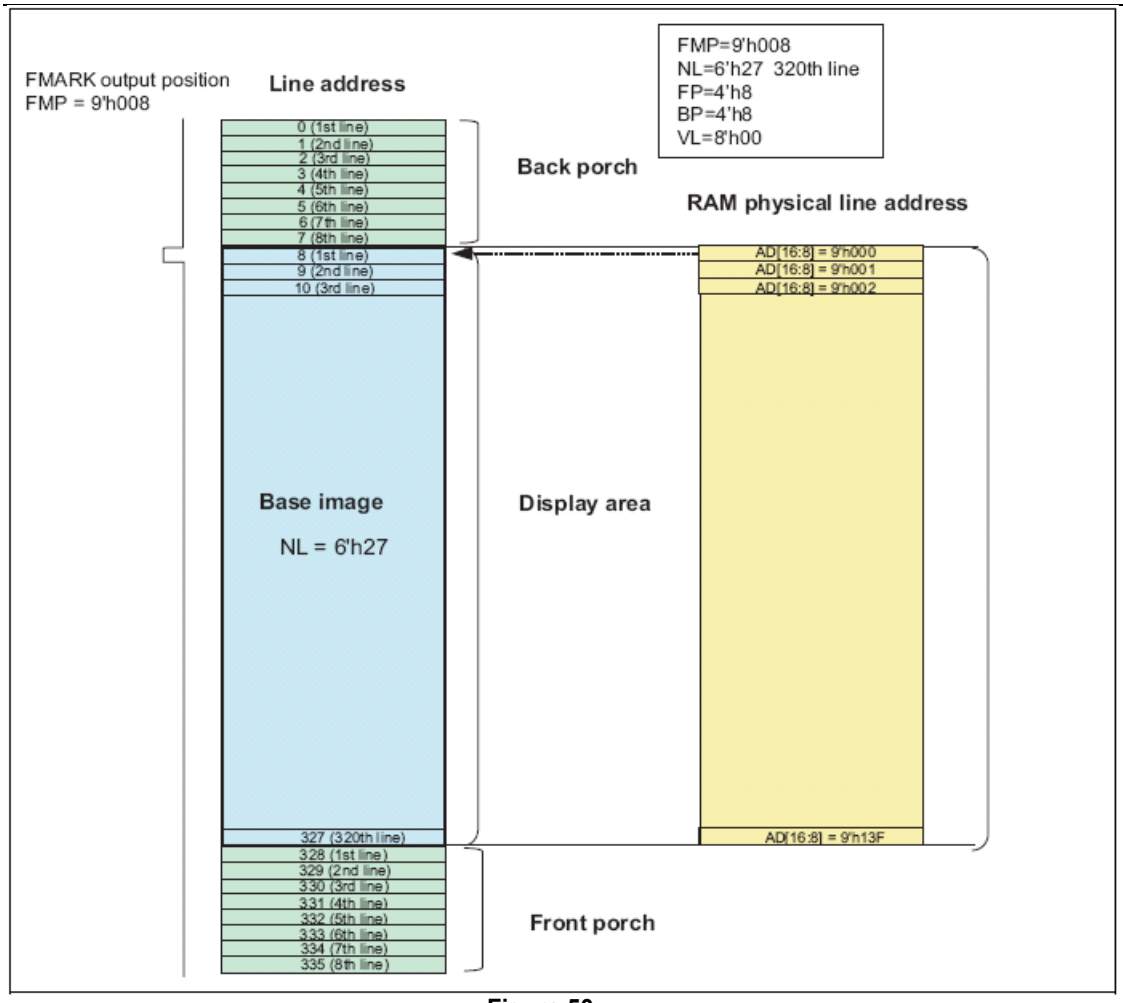


Figure 50

Display operation synchronous data transfer using FMARK

The FT1509 uses FMARK signal as a trigger signal to start writing data to the internal GRAM in synchronization with display scan operation.

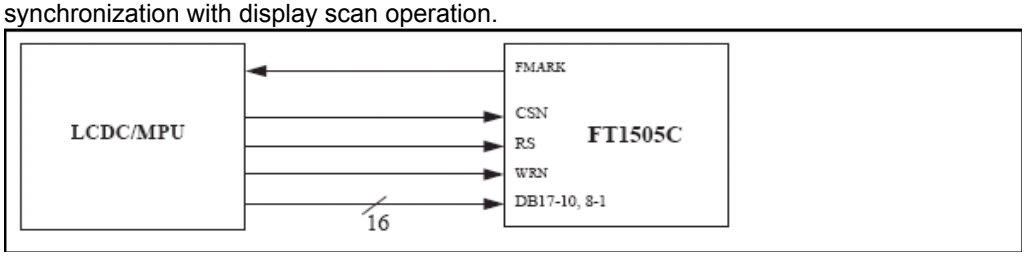


Figure 51: Display synchronous data transfer interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture GRAM area without causing flicker on the display. The data is written in the internal GRAM in order to transfer only the data written over the moving picture display area and minimize the data transfer required for moving picture display.

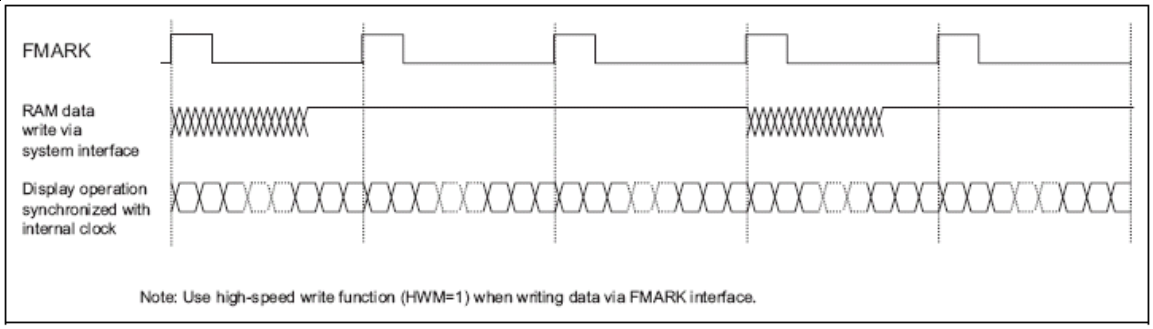


Figure 52: Moving Picture Data Transfers via FMARK function

When transferring data in synchronization with FMARK signal, minimum GRAM data write speed and internal clock frequency must be taken into consideration. They must be more than the values calculated from the following equations.

Internal clock/oscillator frequency (fosc) [Hz]
*= FrameFrequency * (DisplayLInes(NL) + FrontPorch(FP) + BackPorch(BP)) * 16(clocks) * variance*

RAMWrieSpeed(min.)[Hz] > $\frac{240 * \text{DisplayLines (NL)}}{(\text{FrontPorch (FP)} + \text{BackPorch(BP)} + \text{DisplayLines (NL)} - \text{margin}) * 16 \text{ (clock)} * \frac{1}{f_{OSC}}}$

Note: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

Notes:
1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one FMARK cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM write [Hz] > 240 * 320 / {((2+14+320-2) lines * 16 clocks) * 1/394 kHz} = 5.67 MHz

Notes:
1. In this example, it is assumed that the FT1509 starts writing data in the internal RAM on the rising edge of FMARK.
2. There must be at least a margin of 2 lines between the line to which the FT1509 has just written data and the line where display operation on the LCD is performed.
3. The FMARL signal output position is set to the line specified by FMP[8:0] bits.

In this example, RAM write operation at a speed of 5.67 MHz or more, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the FT1509 starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

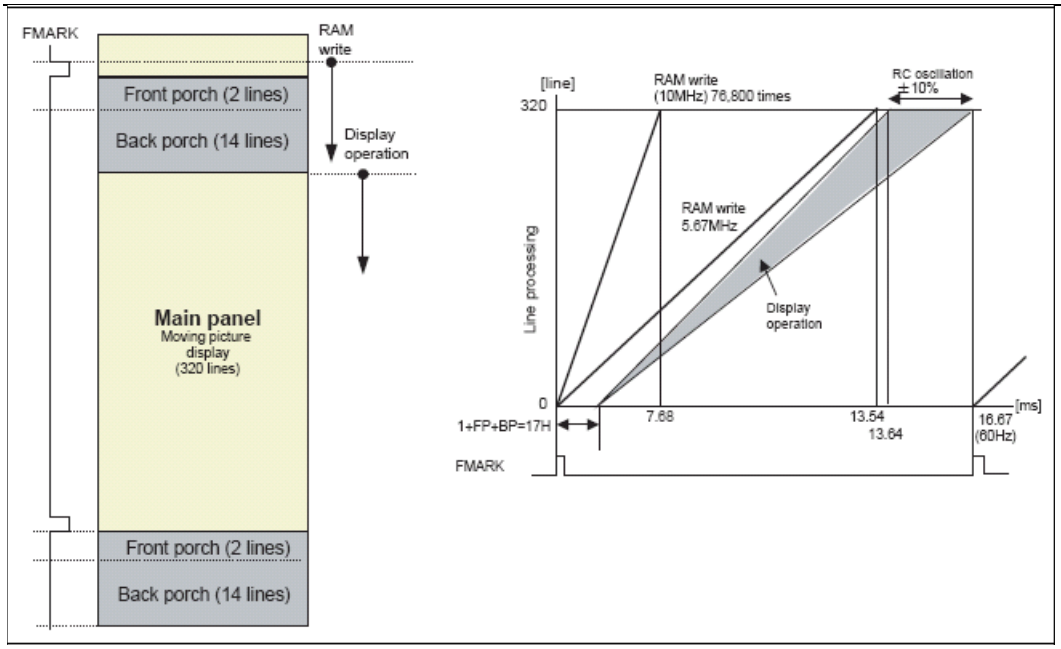


Figure 53: Write/Display Operation Timing

Notes to display operation synchronous data transfer using FMARK signal

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make an enough margin in setting RAM write speed for this operation.

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the FT1509 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area]	
(horizontal direction)	8'h00 ≤ HSA ≤ HEA ≤ 8'hEF
(vertical direction)	9'h000 ≤ VSA ≤ VEA ≤ 9'h13F
[RAM address (AD16-0)]	
(RAM address)	HSA ≤ AD7-0 ≤ HEA VSA ≤ AD16-8 ≤ VEA

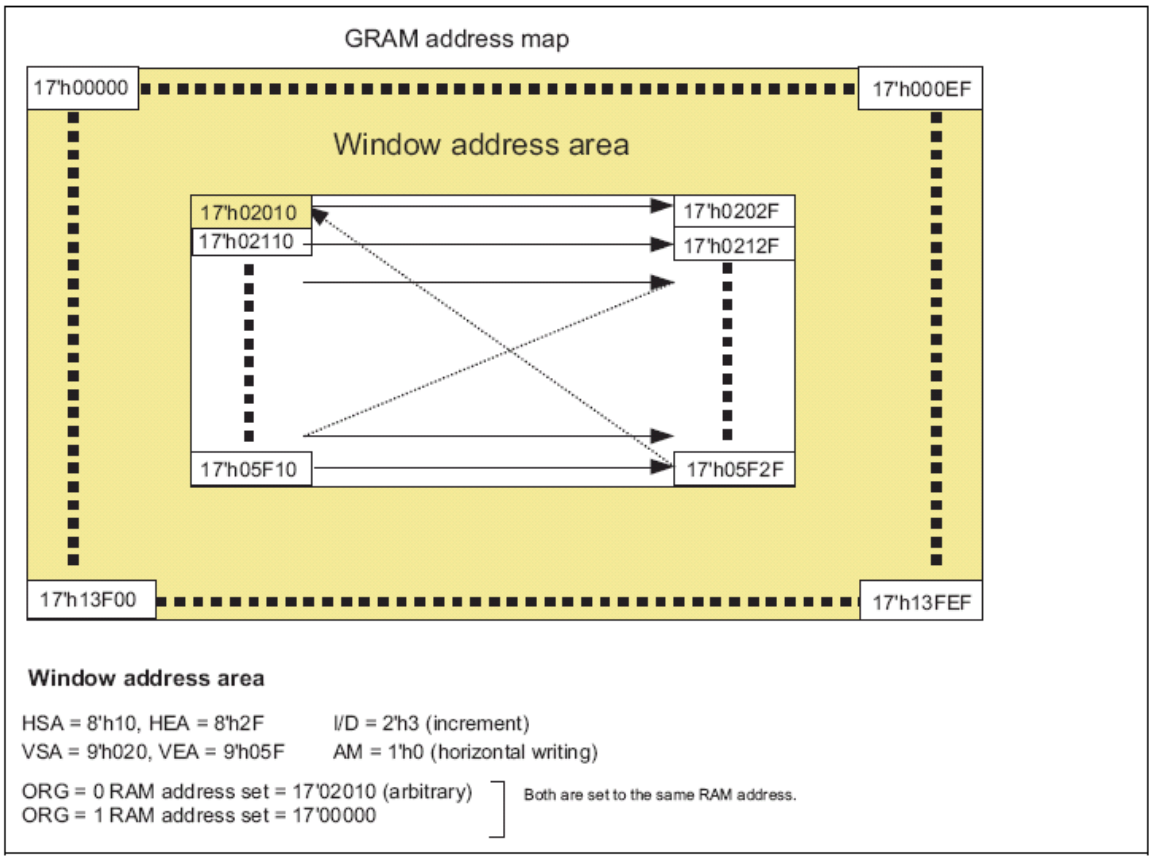


Figure 57: Automatic address update within a Window Address Area

Content Adaptive Backlight Control

The FT1509 supports CABC (Content Adaptive backlight control) function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The display image is dynamically controlled by CABC function. The availability of this function ranges from moving picture such as TV image to still picture such as menu. The histogram of display data is analyzed by CABC function, according to the brightness range of backlight set by parameters. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image.

Note 1: The CABC setting is enable by RC0h IB0 bit setting.

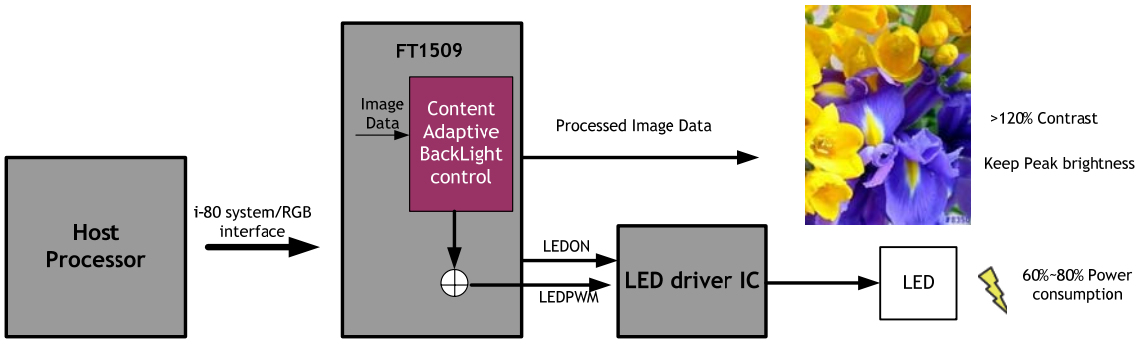
Note 2: The effect of CABC function on power efficiency and display quality depends on image data and the setting. Check display quality on the panel.

Note 3: The CABC function is not available in Partial Mode On and Idle Mode On.

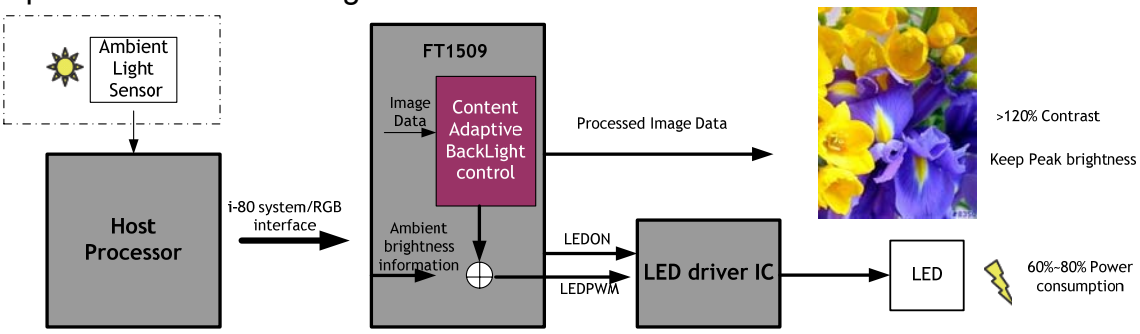
- Control backlight dynamically according to the image histogram.
- PWM pin for LED backlight adjustment
- PWM signal control register set by the host processor. Control dimmer for backlight by combinating PWM setting value internally controlled by the CABC function and maximum PWM setting set by the host processor.

System configuration

Option1: Without ambient light sensor



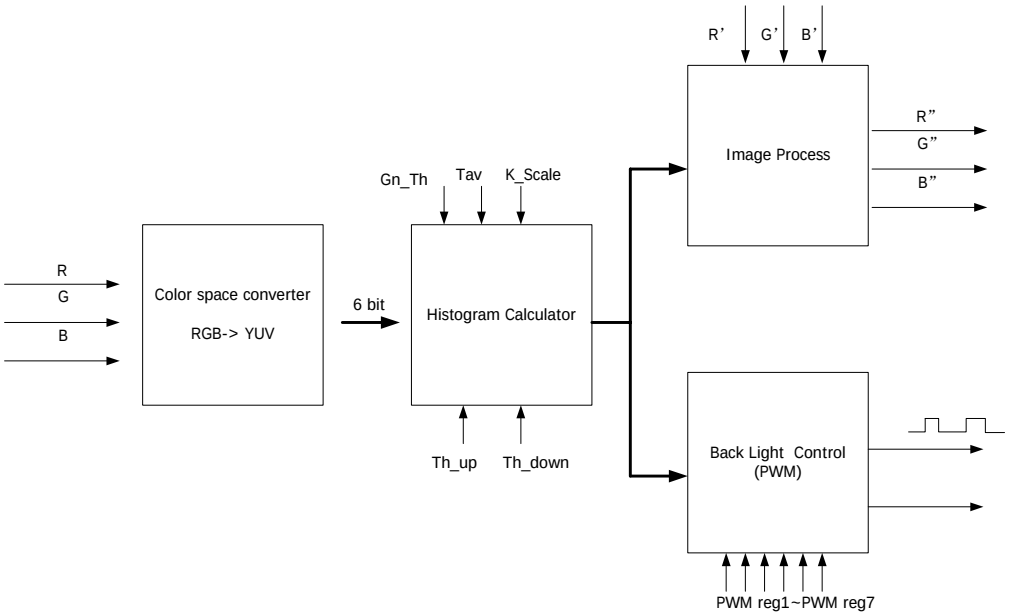
Option 2: with ambient light sensor



CABC parameter setting

The content adaptive backlight control function has the following four functions.

- Picture histogram analysis and display data processed
- Backlight PWM control
- Expand the grayscale of the display image that is turned into white
- Enhanced dynamic picture contrast



These functions are set by the following parameters

Global control register (RC0h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0	0	0	PWMon	0	0	DBLs	DBLs	0	0	0	LEDonR	0	0	0	DBL_Enable
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PWMon: Sets the ON/OFF of PWM control signal. "1"—LED PWM output "0"－No PWM output

DBLs[1:0]: DBL mode select

Value	Operation
2'b00	Manual backlight control by register DBCV (RC8h)
2'b01	Dynamic backlight control just by ambient brightness information
2'b10	Dynamic backlight control just by content information
2'b11	Dynamic backlight control by ambient brightness and content information

LEDonR: control the "LEDON" pin of LED driver chip. "0" means LEDON='1'; "1" means LEDON='0'.

DBL_Enable:

Value	Operation
1'b0	Disable "CABC" function.
1'b1	Enable "CABC" function

Image process setting register1 (RC1h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0	0	0	0	0	0	Per_loss[2]	Per_loss[1]	Per_loss[0]	0	Num_th[5]	Num_th[4]	Num_th[3]	Num_th[2]	Num_th[1]	Num_th[0]
Default		0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0

Per_loss: the maximum percentage number of effective peak area. The percentage number is **Per_loss**/32.

Num_th: the threshold number in picture histogram processing. The threshold number is **Num_th** /4.

Image process setting register2 (RC2h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0	0	0	V_mode	0	TAV	TAV	TAV	Tav_adapt[7]	Tav_adapt[6]	Tav_adapt[5]	Tav_adapt[4]	Tav_adapt[3]	Tav_adapt[2]	Tav_adapt[1]	Tav_adapt[0]
Default		0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0

V_mode: 1'b0 means still picture mode. 1'b1 means video mode.

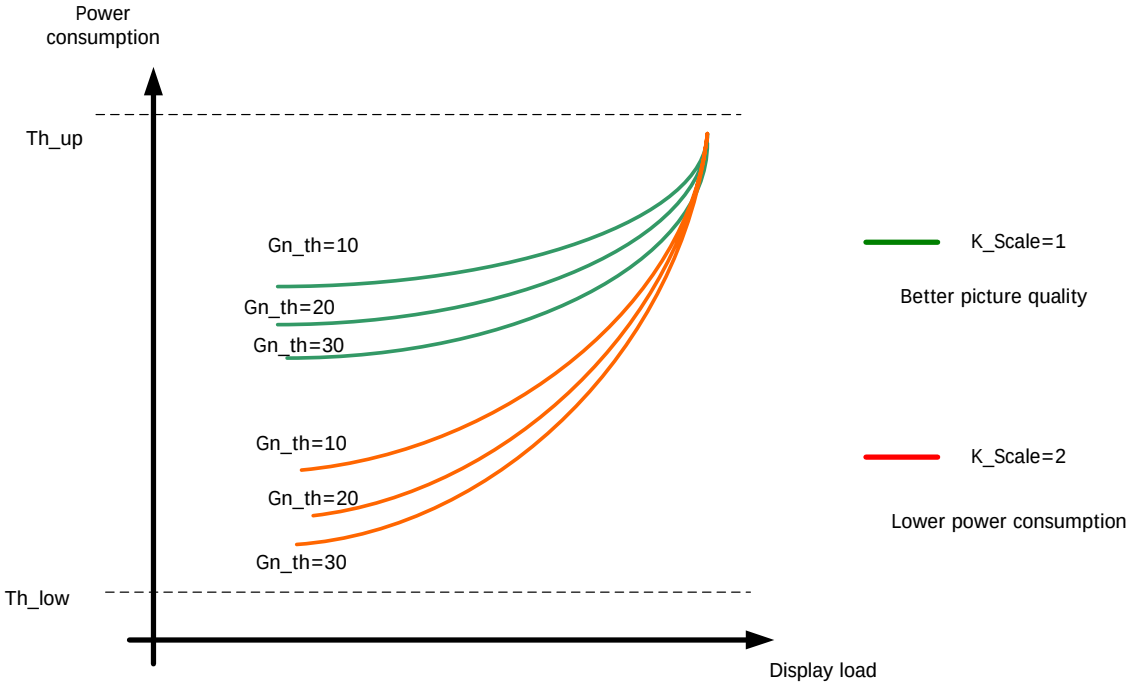
TAV: In still picture mode, this register indicates "PWM value"'s corresponding response to picture load.

Image process setting register3 (RC3h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0	0	K5	K4	K3	K2	K1	K0	0	0	Th_low[5]	Th_low[4]	Th_low[3]	Th_low[2]	Th_low[1]	Th_low[0]
Default		0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	1

K: the radio value for alpha adjustment.

Th_low: the minimum value of "pwmvlaue".



Gamma setting register1 (RC4h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	PWd2[7]~PWd2[0]								PWd1[7]	PWd1[6]	PWd1[5]	PWd1[4]	PWd1[3]	PWd1[2]	PWd1[1]	PWd1[0]
Default		0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0

PWd2[7:0]: coefficients value of Gamma adjustment

PWd1[7:0]: coefficients value of Gamma adjustment

Gamma setting register2 (RC5h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	PWd4[7]~PWd4[0]								PWd3[7]	PWd3[6]	PWd3[5]	PWd3[4]	PWd3[3]	PWd3[2]	PWd3[1]	PWd3[0]
Default		0	0	1	1	0	1	1	1	0	0	0	1	1	1	0	1

PWd3[7:0]: coefficients value of Gamma adjustment

PWd4[7:0]: coefficients value of Gamma adjustment

Gamma setting register3 (RC6h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	PWd6[7]~PWd6[0]								PWd5[7]	PWd5[6]	PWd5[5]	PWd5[4]	PWd5[3]	PWd5[2]	PWd5[1]	PWd5[0]
Default		1	0	0	0	0	1	1	1	0	1	0	1	1	0	1	0

PWd5[7:0]: coefficients value of Gamma adjustment

PWd6[7:0]: coefficients value of Gamma adjustment

Gamma setting register4 (RC7h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0					PWd7[7]	PWd7[6]	PWd7[5]	PWd7[4]	PWd7[3]	PWd7[2]	PWd7[1]	PWd7[0]			

Default	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0

PWd7[7:0]: coefficients value of Gamma adjustment

Manual backlight setting register (RC8h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0					DBCV[7]	DBCV [6]	DBCV [5]	DBCV [4]	DBCV [3]	DBCV [2]	DBCV [1]	DBCV [0]			
Default	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

DBCV[7:0]: coefficients value of manual backlight control

Backlight setting register9 (RC9h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	MBSD[7:0]					LABC[7]	LABC [6]	LABC [5]	LABC [4]	LABC [3]	LABC [2]	LABC [1]	LABC [0]			
Default	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	

LABC[7:0]: coefficients value of manual backlight control
MBSD[7:0]: Minimum backlight brightness

PWM setting register1 (RCAh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0					PWMDIV[7]	PWMDIV [6]	PWMDIV [5]	PWMDIV [4]	PWMDIV [3]	PWMDIV [2]	PWMDIV [1]	PWMDIV [0]			
Default	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

PWMDIV[7:0]: the clock divided value of PWM

PWM setting register2 (RCBh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W/R	1	0					Out_sel	Out_sel	0	0	0	0	0	0	0	PWM_pol	
Default	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	

PWM_pol: the PWM polarity control (“1”: high means LED lights; “0”: low means LED lights)
Out_sel: CABC control signal Output pin configuration

Value	Operation
2’b00	Normal
2’b01	LEDPWM → “FMARK” pin LEDON --
2’b10	LEDPWM → “TS4” pin LEDON → “TS3” pin

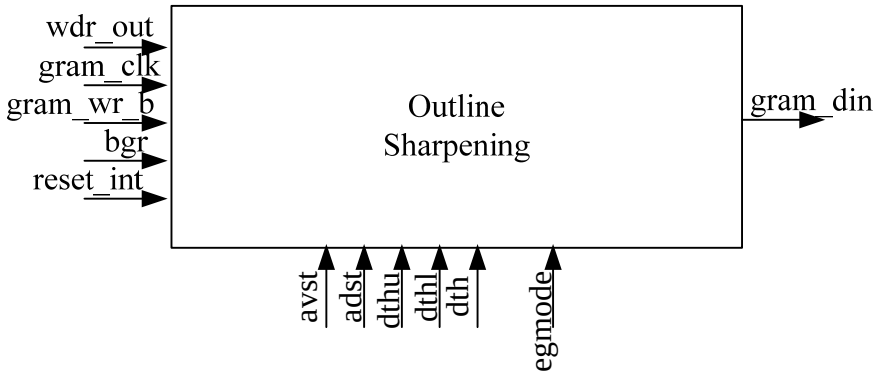
PWM setting register3 (RCFh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	0	0	0	0	0	0	PWM_value [7:0]							
Default	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0

PWM_value [7:0]: DBL calculation result, it could be read by CPU.

Edge Enhancement

The FT1509 supports edge enhancement function. Still picture and movie can be enhance their details edge, can be written onto the RAM by setting image processing parameters, AVST, ADST, DTHU and DTHL and EGMODE=1 and then transfer original data to designated window address.
The characteristics of algorithm used in this function may not fit some types of data to unexpectative result.



The theory of edge enhancement

In the characteristics of algorithm AVST, ADST, DTHU and DTHL bits set parameters that adjust image data.
The following figure shows how the parameters and each stages of operational sequence interact.

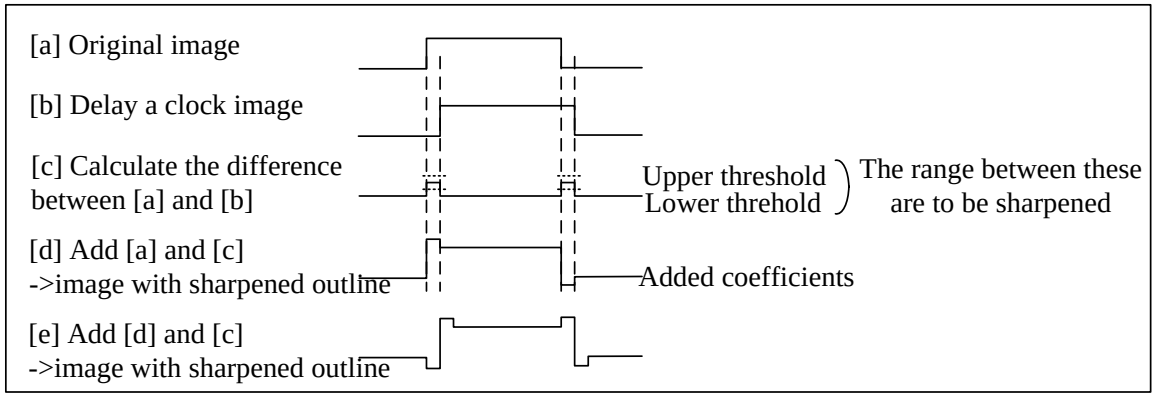


Image process setting register12 (R06h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	EGMODE	AVST[2:0]			0	ADST[2:0]			DTHU[1:0]		DTLU [1:0]		0	DTH[2:0]		
Default		0	0	1	1	0	0	1	1	0		0	1	0	0	1	1

EGMODE: Enable/Disable control of edge enhancement function. When 1'h0 means "Disable", when 1'h1 means "Enable".

AVST: Coefficients

AVST	coefficients
3'h00	0.125(=1/8)
3'h01	0.250(=2/8)
3'h02	0.375(=3/8)
3'h03	0.500(=4/8)
3'h04	0.625(=5/8)
3'h05	0.750(=6/8)
3'h06	0.875(=7/8)
3'h07	1.000(=8/8)

ADST: Added coefficients

ADST	Addedcoefficients
3'h00	0.0(Off)
3'h01	0.5(=1/2)
3'h02	1.0(=2/2)
3'h03	1.5(=3/2)
3'h04	2.0(=4/2)
3'h05	2.5(=5/2)
3'h06	3.0(=6/2)
3'h07	3.5(=7/2)

DTHU: High threshold of the brightness band

DTHU	**Higher threshold**
2'h00	15
2'h01	31
2'h02	47
2'h03	63

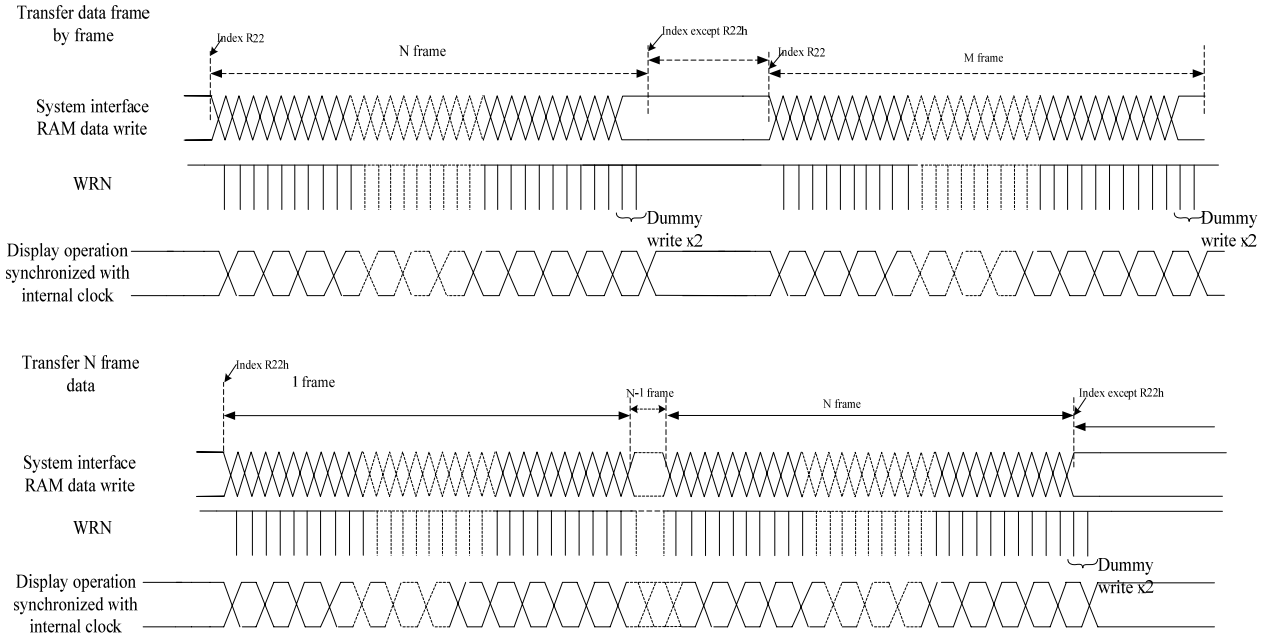
DTHL: Lower threshold of the brightness band

DTHL	Lower threshold
2'h00	0
2'h01	Setting Disabled
2'h02	1
2'h03	2

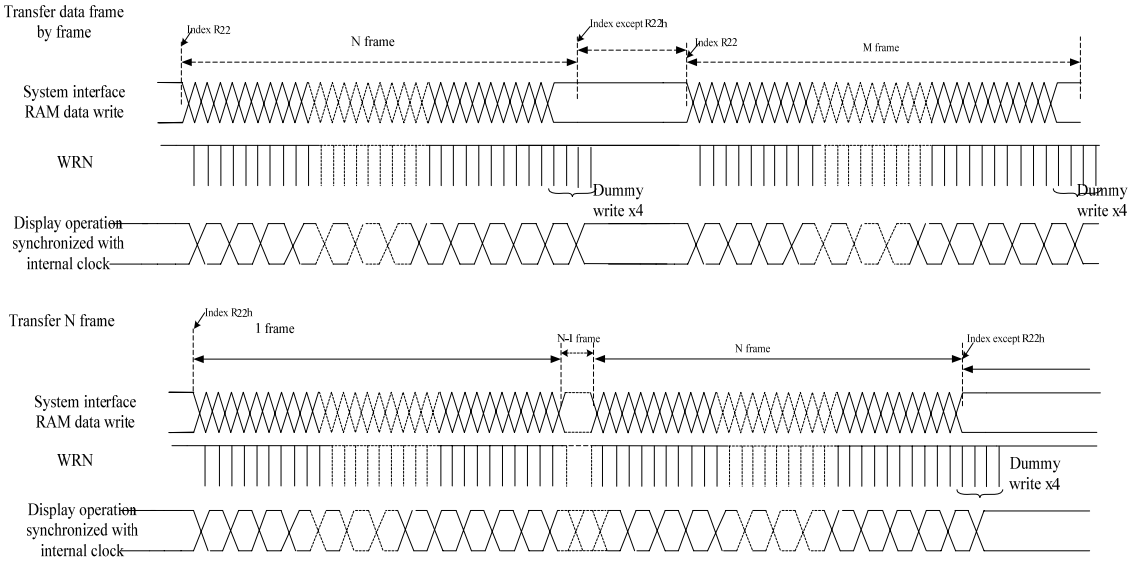
Restriction to outline sharpening function

1. Outline sharpening instruction should be set before writing data to RAM.
2. When writing data to RAM, dummy write must be done 1 times consecutively right after transferring data of one frame that is set by window address setting.

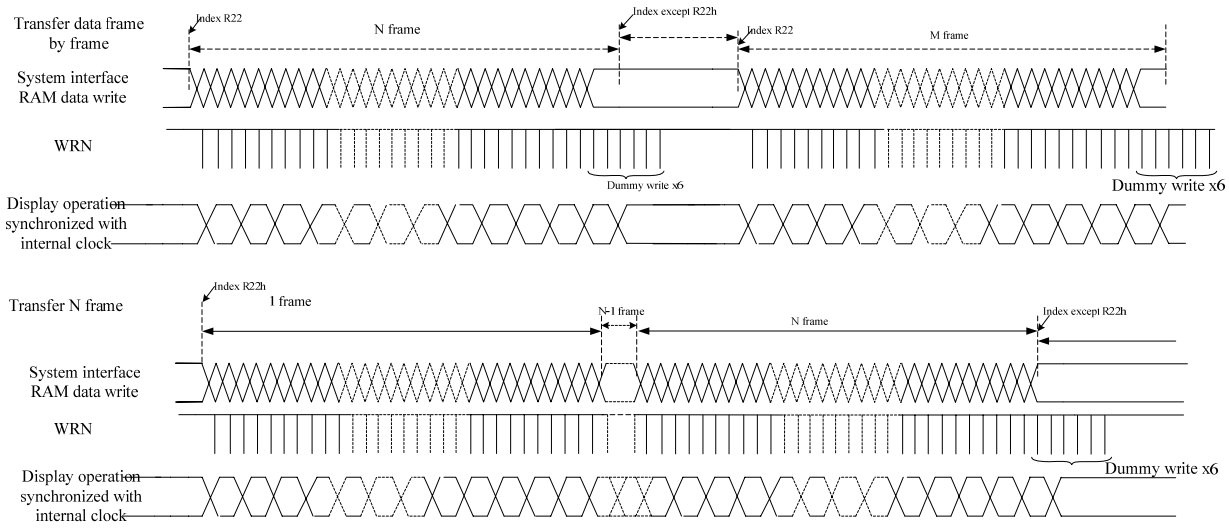
Data transferring RGB mode/FMARK mode/80 system 16/18 bit



Data transferring RGB mode/FMARK mode/80 system 8/9 bit (2-transfer mode)



Data transferring 80 system 8 bit (3-transfer mode)



Scan Mode Setting

The FT1509 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the FT1509 and the LCD panel.

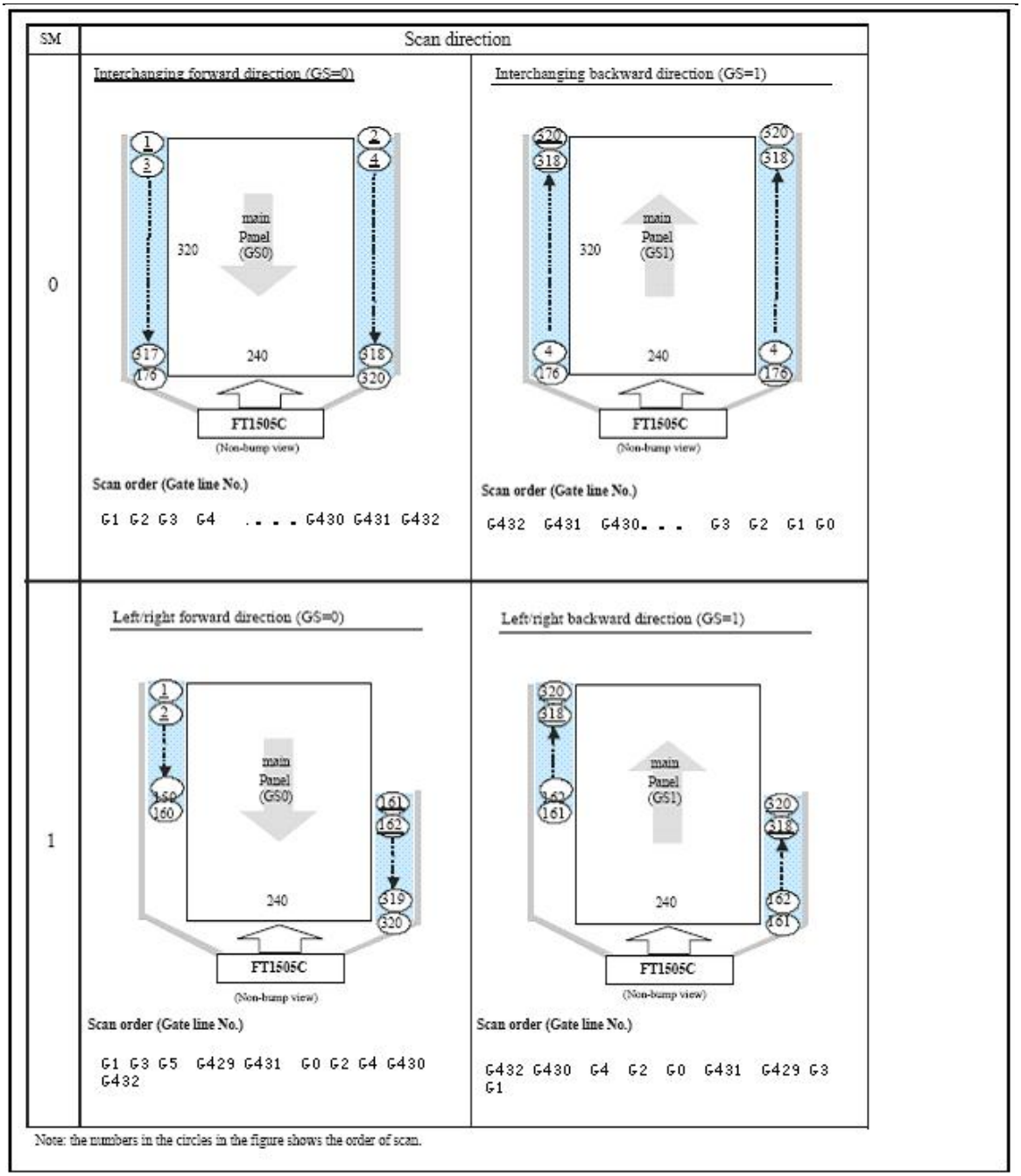


Figure 58

8-color Display Mode

In 8-color display mode, the γ-adjustment registers PKP0-PKP5, PKN0-PKN5, PRP0, PRP1, PRN0,

PRN1 are disabled and the power supplies to V1 to V62 are halted. The FT1509 **does** require GRAM data rewrite for 8-color display by writing the MSB to the rest in each dot data to display in 8 colors.

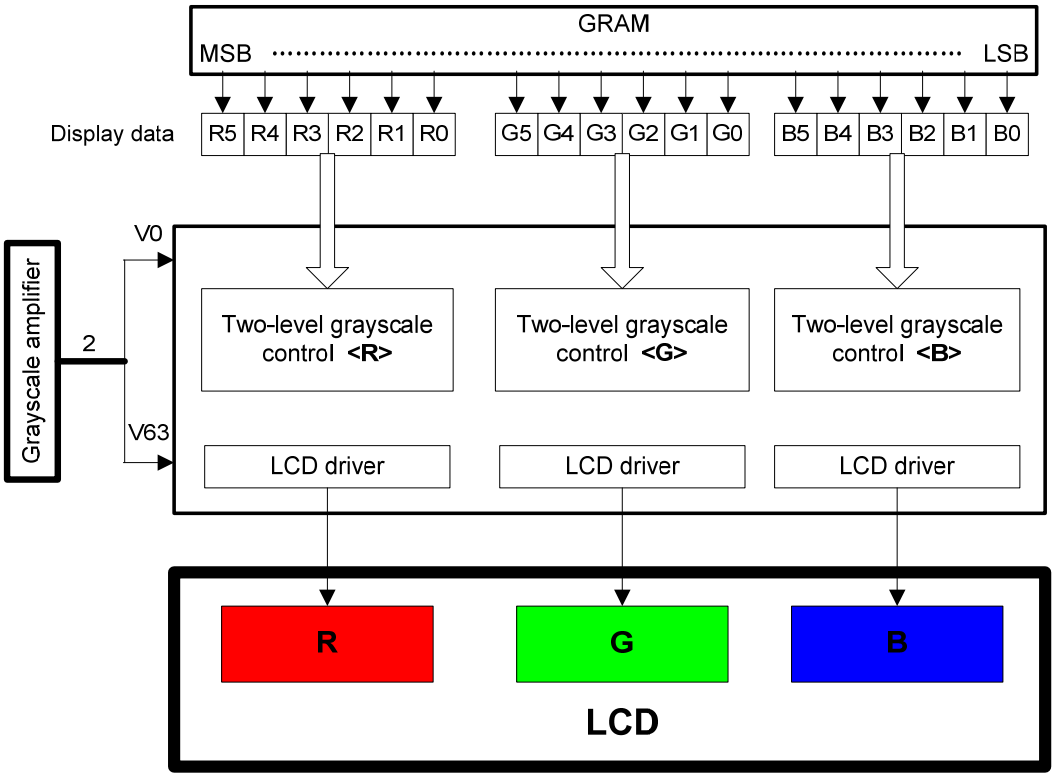


Figure 59

n-line Inversion AC Drive

The FT1509, in addition to the frame-inversion liquid crystal alternating current drive, supports the n-line inversion alternating current drive to invert the polarity of liquid crystal in every n-line periods, where n takes a number from 1 to 64. The n-line inversion can provide a solution when there is a need to improve the display quality.

In determining “n”(the value represented by NW bits +1), check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.

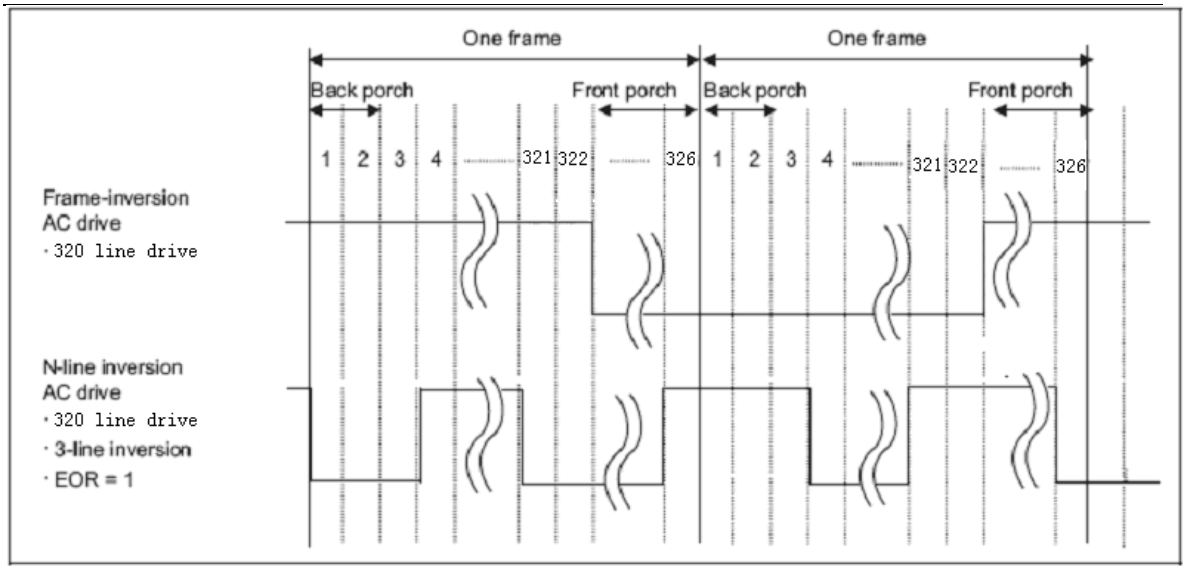


Figure 60

Note: Make sure to set EOR = “1” to prevent direct bias on liquid crystal when selecting n-line inversion drive.

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the FT1509 draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of n-line inversion AC drive, polarity is inverted as the FT1509 draws n line, and a blank period lasting for (BP+FP) periods is inserted when the FT1509 draws one frame.

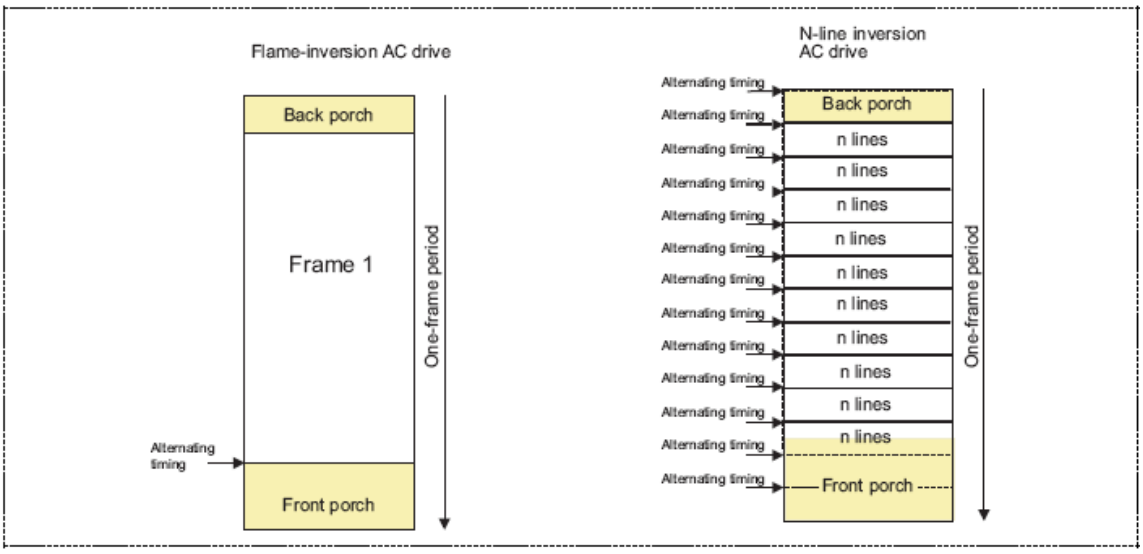


Figure 61

Frame-Frequency Adjustment Function

The FT1509 supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIVI, RTNI bits without changing the oscillation frequency.

The FT1509 allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIVI and RTNI settings, the FT1509 can operate at high frame frequency when displaying a moving picture, which requires the FT1509 to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between liquid crystal drive duty and frame frequency

The following equation represents the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTNI) and the operation clock frequency division ratio setting bit (DIVI).

(Formula to calculate frame frequency)

Frame frequency = fosc/[Clock cycles per line × division ratio × (Line+BP+FP)] [Hz]

fosc: RC oscillation frequency
Line: number of lines to drive a panel (NL bits)
Clock cycles per line: RTNI bits
Division ratio: DIVI bits
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive a panel: 320 lines
1H period: 16 clock cycles (RTNI4-0 = “10000”)
Operation clock division ratio: 1/1
Front porch (FP): 2 line periods
Back porch (BP): 14 line periods

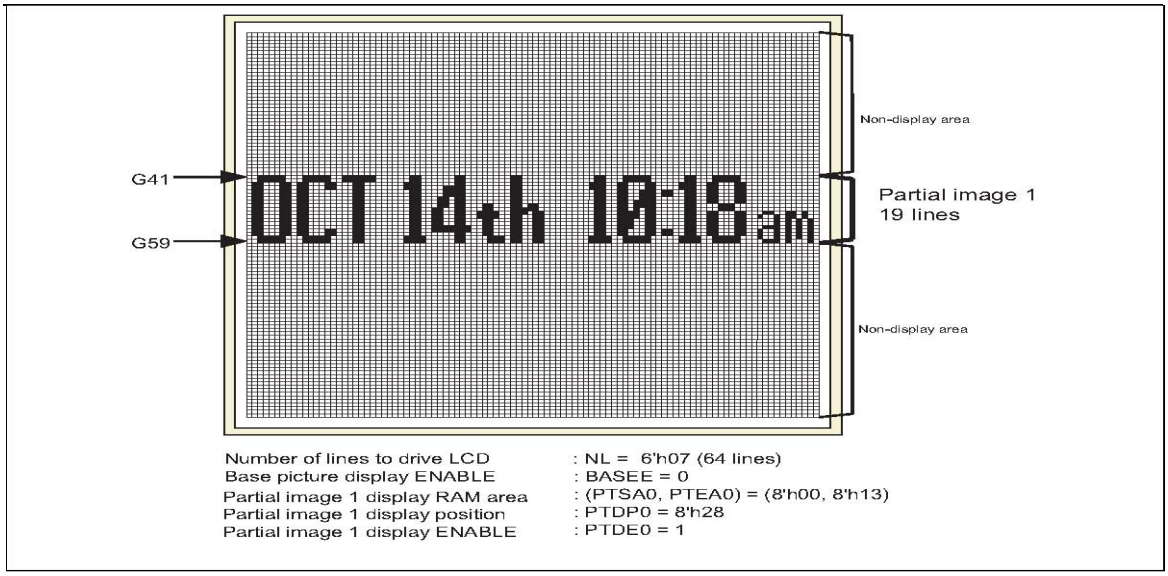
fosc = 60 (Hz) × (0+16) (clocks) × 1/1 × (320 + 2+ 14) (lines) = 323 (kHz)

In this case, the RC oscillation frequency is 323k Hz. Set register (RB0h) RC[2:0] = “100” for internal oscillator or adjust the external RC oscillator to set the frequency to 323k Hz.

Partial Display Function

The partial display function allows the FT1509 to drive lines selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.



Note: See the “RAM Address and Display Position on the Panel” for details on the relationship between the display position on the panel and the RAM area setting for partial image.

Figure 62

Low power consumption drive settings

The FT1509 supports the following low power consumption drive methods to drive the panel with less power requirement. Generally, there is a trade-off between power efficiency and quality of display. Also, the power efficiency depends on the characteristics of the panel. Check which of the following methods can achieve the optimal balance between power consumption and display quality.

1. 8-color display mode (COL)

In this mode (CL = “1”), the FT1509 halts power supplies except for V0 and V63. In this mode, the FT1509 display in 8 colors to save power.

2. Partial display

In this mode, the data is displayed as partial image and the base image is turned off (BASEE = 0). The normal display operation is limited to the partial display area to save power.

The source output level in non-display area can be changed by instruction (PTS[2:0]). The PTS[2:0] setting allows halting the operation of grayscale voltage generating amplifiers except for V0, V63 and slowing down the clock frequency for step-up operation to half the normal operation frequency.

Table 72 Source outputs in non-display area

PTS[2:0]	Source output in non-display area		Non-display area Grayscale amp operation	Non-display area Step-up clock frequency
	Positive polarity	Negative polarity		
3’h0	V63	V0	V0 to V63	Set by DC0, DC1 bits
3’h1	Setting disabled	Setting disabled	-	-

3'h2	GND	GND	V0 to V63	Set by DC0, DC1 bits
3'h3	Hi-Z	Hi-Z	V0 to V63	Set by DC0, DC1 bits
3'h4	V63	V0	V0, V63	1/2 the frequency set by DC0, DC1 bits
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0, V63	1/2 the frequency set by DC0, DC1 bits
3'h7	Hi-Z	Hi-Z	V0, V63	1/2 the frequency set by DC0, DC1 bits

See also "Partial Display Function" for details.

3. Frame frequency setting

The FT1509 allows changing the liquid crystal polarity inversion cycle by changing the frame frequency by setting DIVI, RTNI bits. To improve power efficiency, set a lower frequency in partial display operation, which requires small power consumption. See also "Frame-Frequency Adjustment Function" for details.

Generally, there is a trade-off between power efficiency and quality of display. The power efficiency also depends on the characteristics of the panel. Check the optimal balance between the quality of display on the panel and the power efficiency before use.

4. Liquid crystal inversion drive

The FT1509 allows selecting liquid crystal inversion drive method from frame-inversion AC drive or line-inversion AC drive by setting B/C, NW bits. Select either appropriate LCD driving method for the kind of display on the panel. Also, see "n-line Inversion AC Drive" for details.

Generally, there is a trade-off between power efficiency and quality of display. The power efficiency also depends on the characteristics of the panel. Check the optimal balance between the quality of display on the panel and the power efficiency before use.

5. Optimizing step-up factor

There are cases that power loss in driving liquid crystal can be minimized by optimizing the step-up factor. Whether this method proves to be effective or not depends on the characteristics of the liquid crystal panel. The step-up factor is set by BT[3:0].

LCD panel interface timing

The following are the relationships between external display interface signals and LCD panel signals when the display operation is synchronized with the internal clock signal.

Internal clock operation

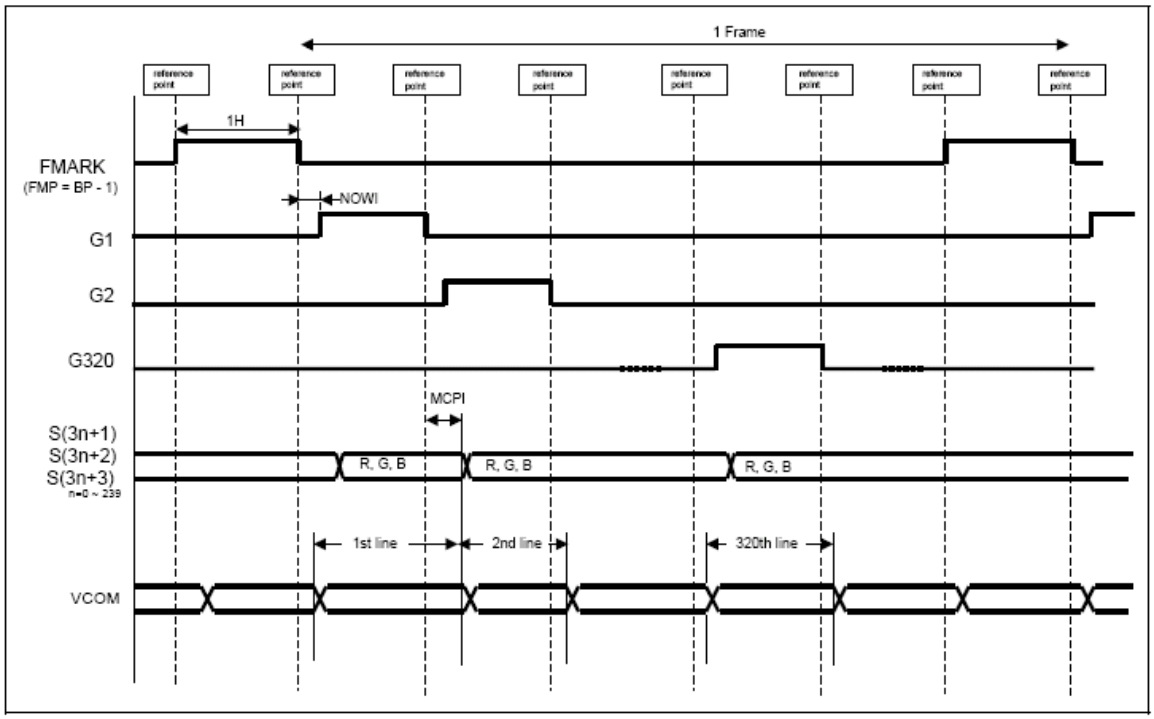


Figure 63

Oscillator

The FT1509 internally incorporates necessary RC elements for oscillator, eliminating the need to connect external elements for RC oscillation. The typical oscillation frequency (fosc) is 358 kHz when using the internal RC oscillator. Adjust the setting of register (RB0h) RC[2:0] to change the oscillation frequency (fosc). To change frame frequency by the RTNI and DIVI settings (Frame frequency adjustment registers).

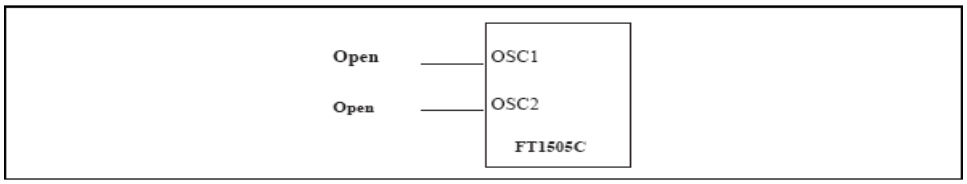


Figure 65

γCorrection function

The FT1509 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels. Furthermore, since the gradient adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

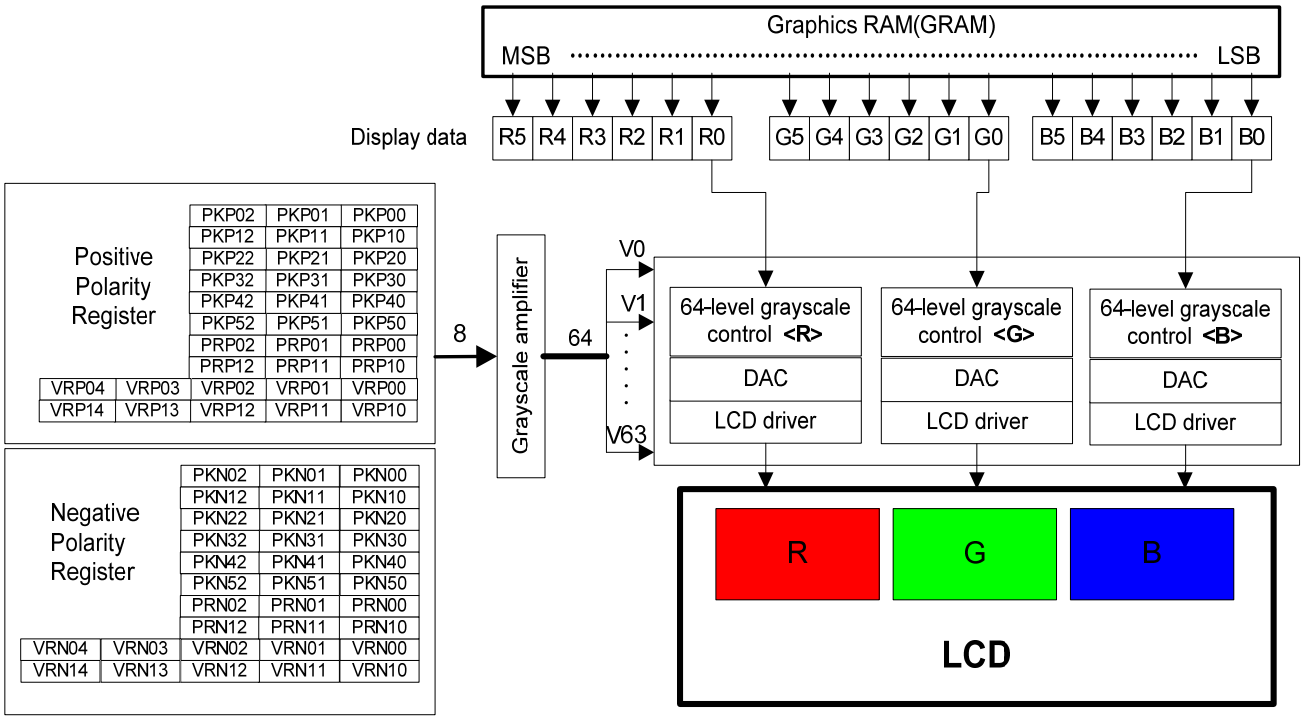


Figure 66: Grayscale control

RAM data (RGB dot data bits) and the source output level

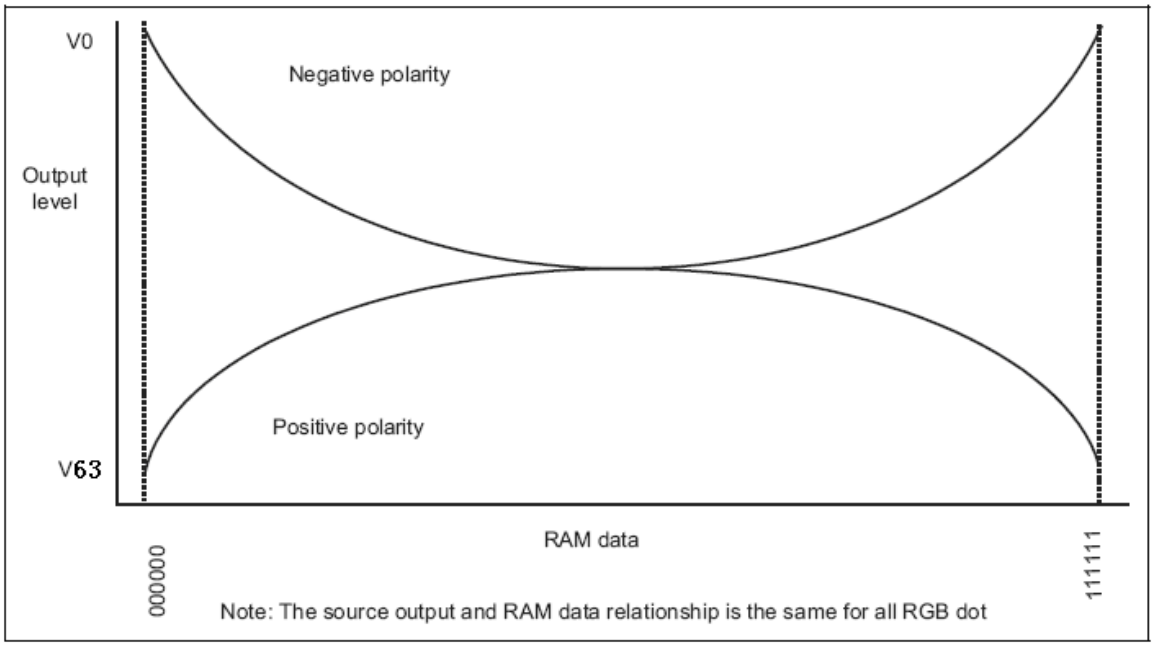


Figure 67

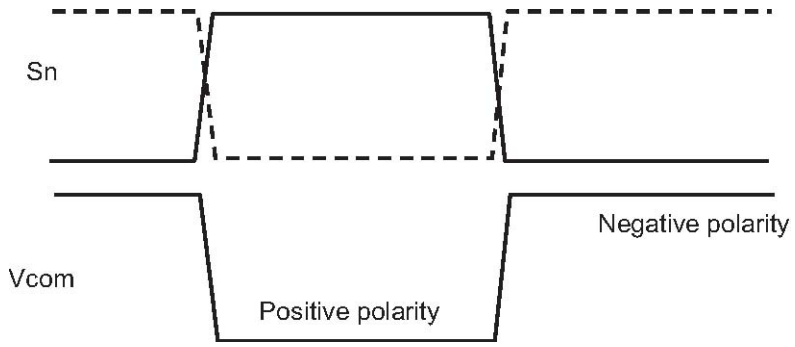


Figure 68: Source output waveform and Vcom polarity

Power Supply Generating Circuit

The following is the configuration of LCD drive voltage generating circuit of the FT1509.

Power supply circuit connection example1 (Vci1=VciOUT)

The VciOUT output circuit changes the VciOUT level in this example.

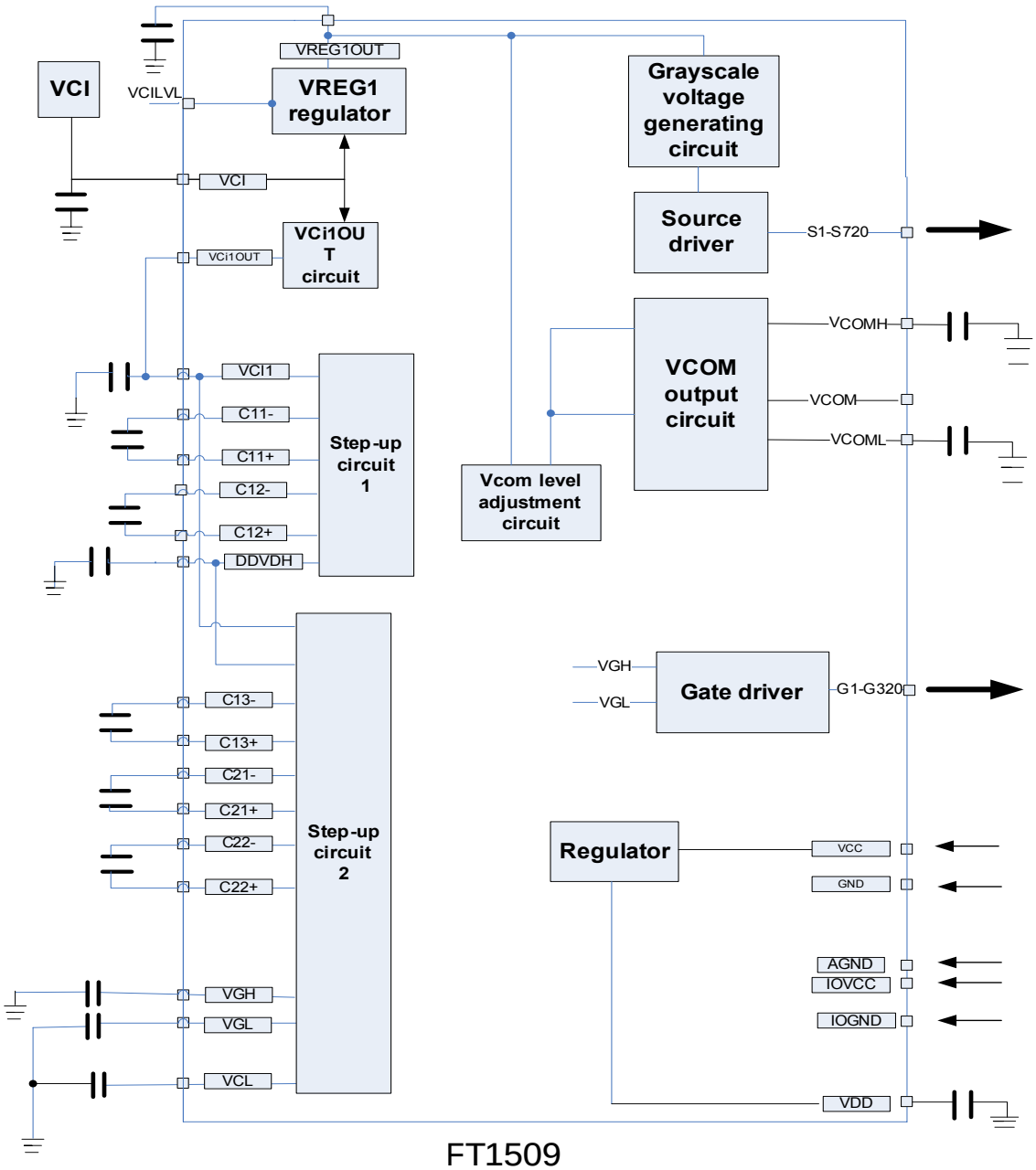


Figure 69

Specifications of external elements for the power supply circuit

The specifications of external elements connected to the power supply circuit of the FT1509 are as follows.

Table 73 Capacitor

Capacitance	Upper voltage limit	Pin connection
1μF Characteristics B	6V	Vci，VCL，VREG1OUT, VciOUT, VcomH， VcomL, C11B/A, C12B/A, C13B/A
	10V	DDVDH, C21B/A，C22B/A
	25V	VGH, VGL

Notes: 1. Checking with the LC module is required.
2. The numbers in the parentheses correspond to the numbers in Figure 79 and Figure 80.

Table 74 Schottky diode

Specification	Pin connection
VF ＜ 0.4V/20mA@25℃, VR≧25V (Recommended diode: HSC226)	**NO NEEDED ！**

Table 76 Internal logic power supply

Capacitor	Recommended voltage proof	Pin connection
IμF (B characteristics)	3V	VDD

Voltage generation diagram

The following are the diagrams of voltage generation in the FT1509 and the TFT display application voltage waveforms and electrical potential relationship.

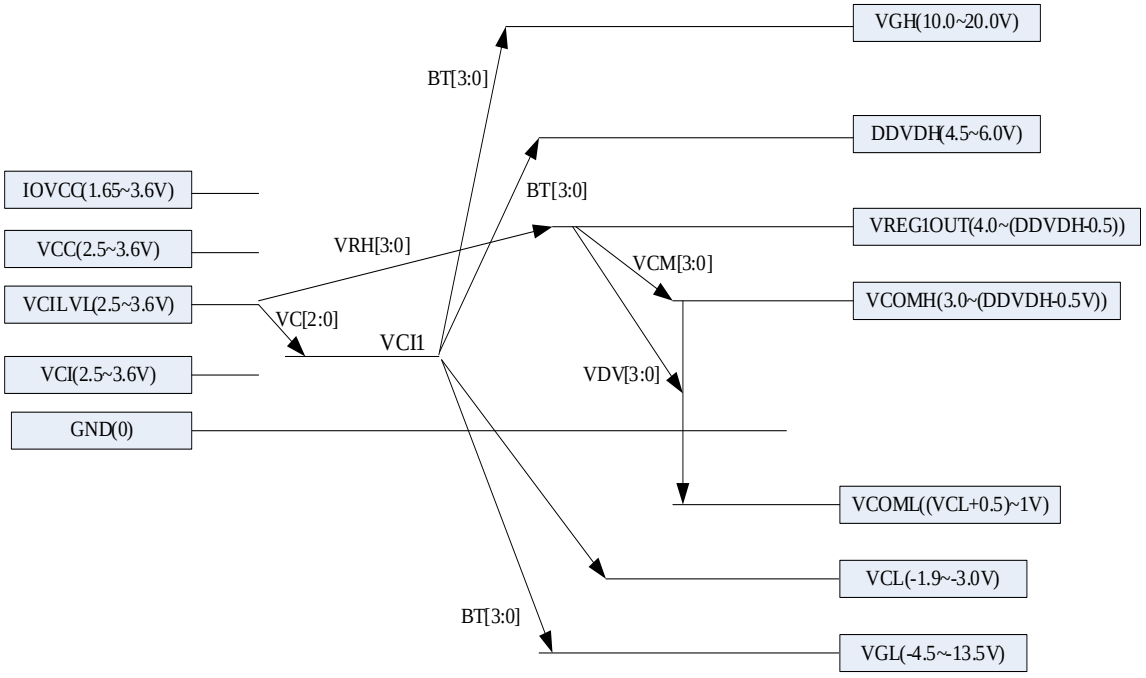


Figure 71: Pattern diagram for voltage setting

Notes: 1. The DDVDH, VGH, VGL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage levels in operation do not conflict with the following conditions: (DDVDH – VREG1OUT) > 0.5V, (DDVDH – VcomH) > 0.5V, (VcomL – VCL) > 0.5V. When the alternating cycle of Vcom is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. In operation, setting voltages within the respective voltage ranges are recommended.

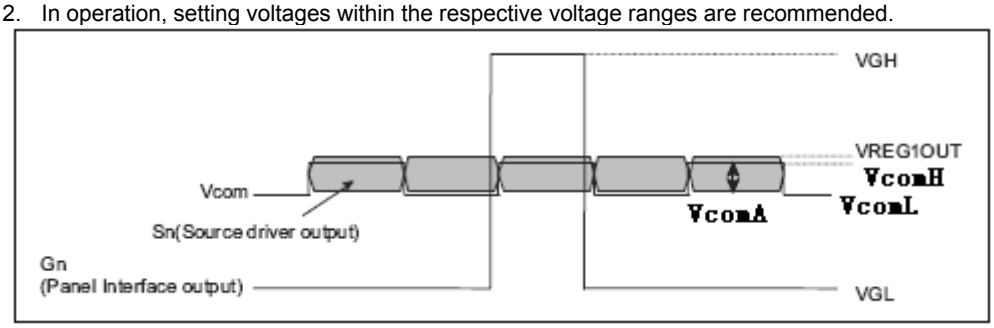


Figure 72: TFT display application voltage waveform and electrical potential

Power Supply Setting sequence

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences (in case of not using internal power supply sequencer).

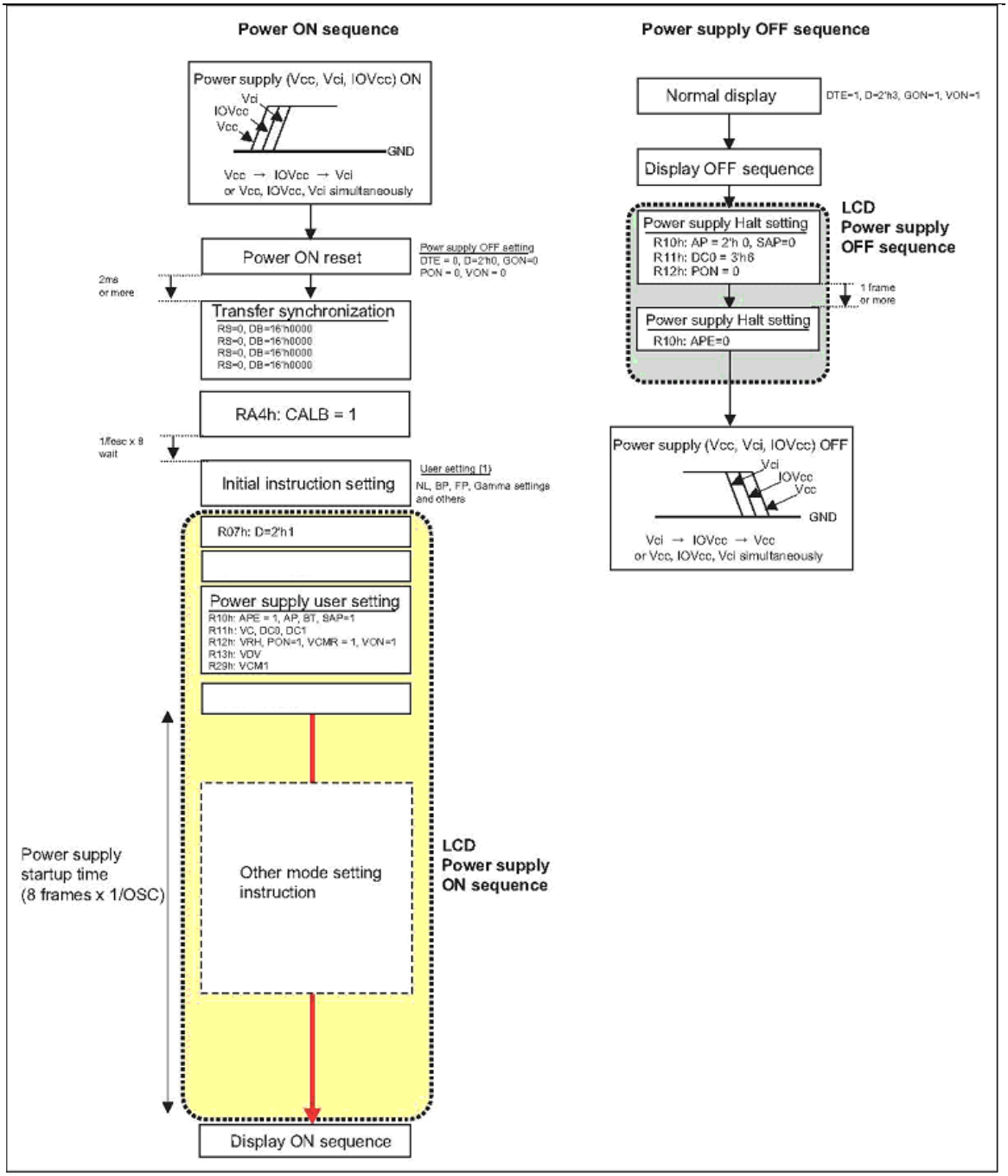


Figure 73

Instruction Setting

The following are the sequences for various instruction settings. When setting instruction in the FT1509, follow the sequence below.

Display ON/OFF

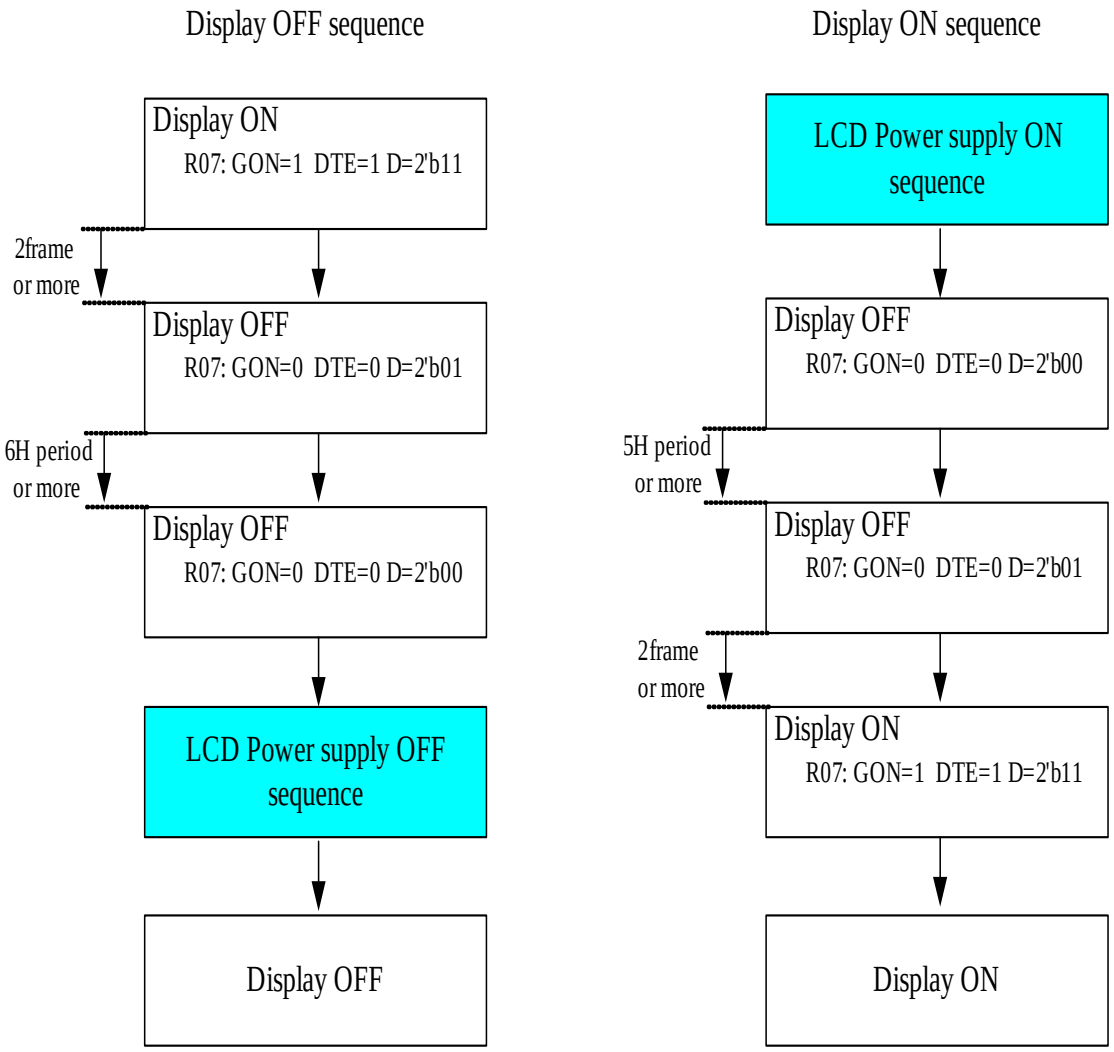


Figure 74

Sleep/Standby mode

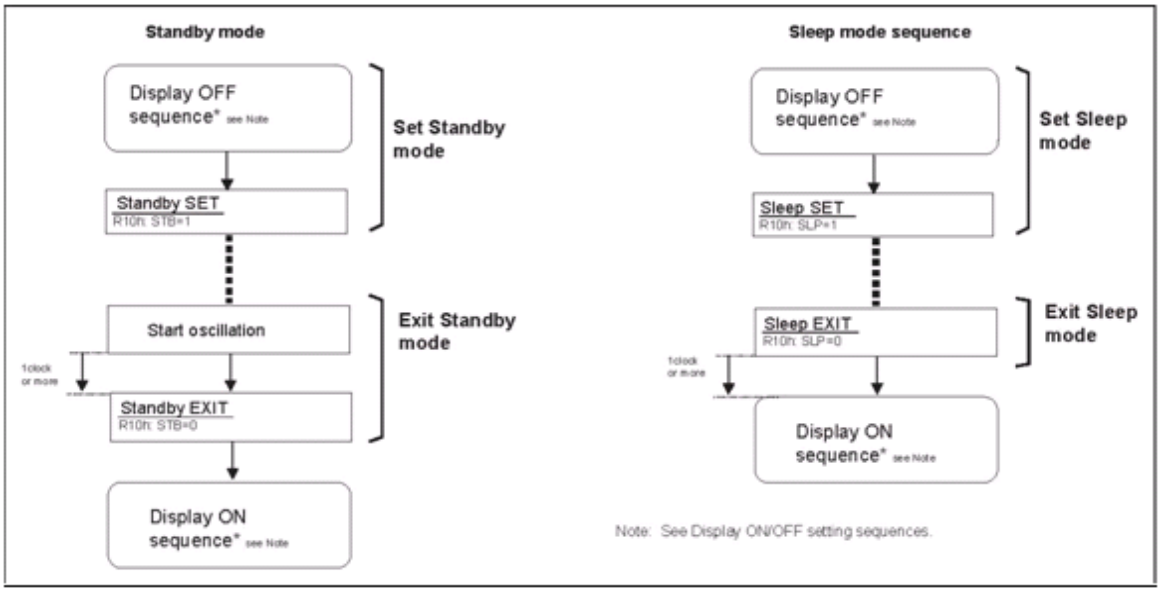


Figure 75

Deep standby mode

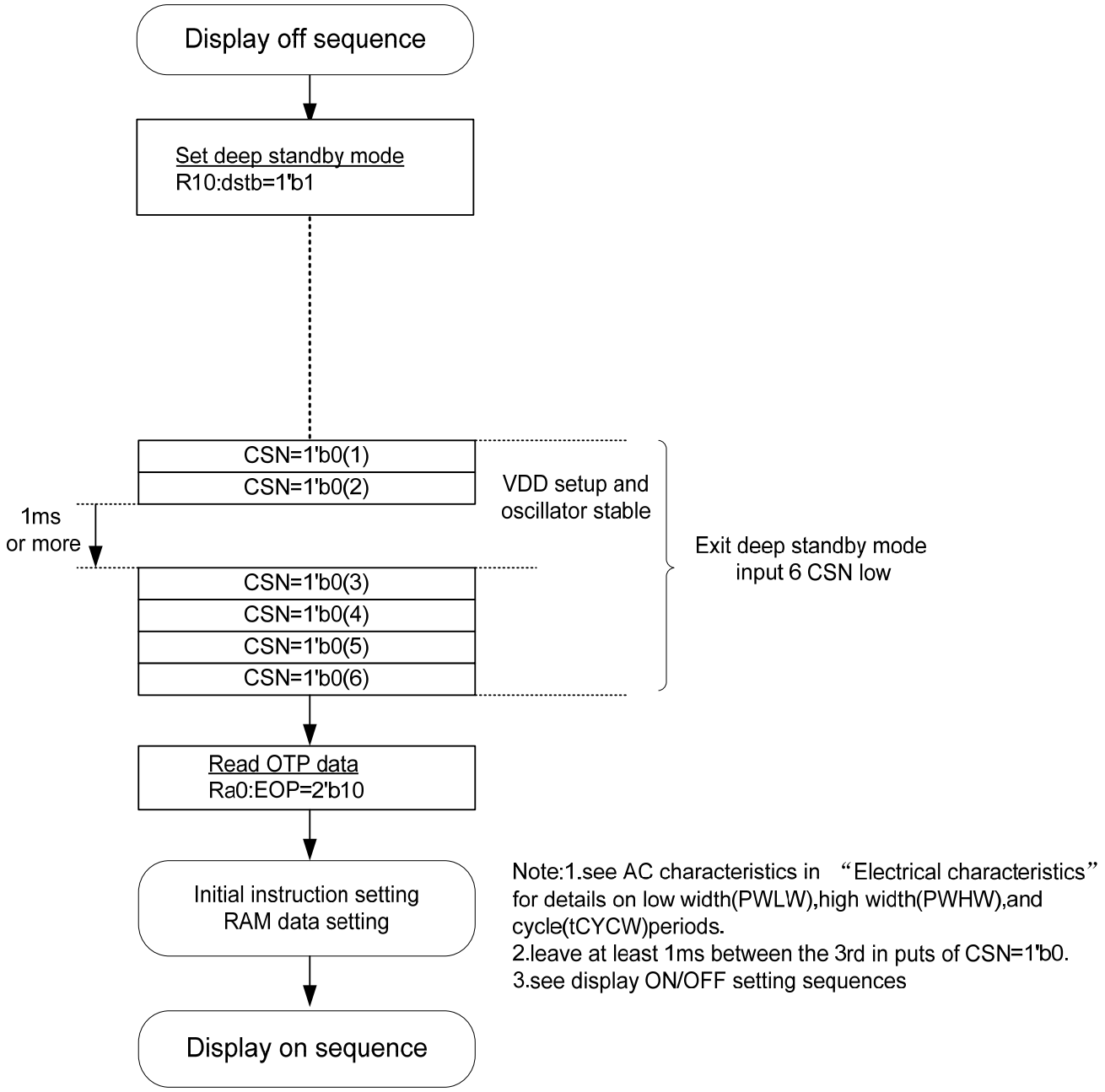


Figure 76

EPROM control

The FT1509 incorporates 8-bits x 3 addresses EPROM. User identification code is written in the EPROM address 0'h. VcomH setting instruction is written in the EPROM addresses 1'h, 2'h. By preparing two addresses to write VcomH setting, it allows changing the VcomH setting. When writing

the VcomH setting for the first time, write the setting in the address 1'h. Write the setting in the address 2'h when writing the setting for the second time. Make sure to write "1" to EVCME0 and EVCME1 bits. When the second VcomH setting is written in the address 2'h, the second setting is enabled.

The VCM_En bit in the RA2h register determines whether the setting in EPROM or the VCM[5:0] setting (externally input instruction) is enabled to set the VcomH level. Set VCM_En = 1, when enabling the EPROM setting. Set VCM_En = 0, when not using the EPROM setting.

When writing the setting to EPROM, make sure to follow the EPROM write sequence.

By performing EPROM read operation, the setting written in EPROM is read out. In this case, follow the EPROM read sequence. In case of setting CALB = 1 (RA4h: calibration to internal operation) after power-on reset, the data written in EPROM is stored in EPROM read register.

EPROM data write control register

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RA0H	0	0	0	0	0	0	0	0	TE	0	EOP[1]	EOP[0]	0	0	EAD[1]	EAD[0]
RA1H	0	0	0	0	0	0	0	0	ED[7]	ED[6]	ED[5]	ED [4]	ED[3]	ED[2]	ED[1]	ED[0]
RA2H																VCM_En

EOP[1:0]	EPROM control bit
2'h0	Halt
2'h1	Write
2'h2	Reset register (load)

EAD[1:0]	EPROM write address
00	User ID code
01	VcomH level setting 1
10	VcomH level setting 1

TE	EPROM write control
0	Data write end
1	Data write start

ED[7:0]	EPROM write data

EAD[1:0]	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
2'h0	0	0	0	0	UID[3]	UID[2]	UID[1]	UID[0]
2'h1	EVCME0	0	EVCM0[5]	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
2'h2	EVCME1	0	EVCM1[5]	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

EPROM data read register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R28H	0	0	0	0	0	0	0	0	0	0	0	0	UID[3]	UID[2]	UID[1]	UID[0]
RAEH	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]	EVCM14	EVCM13	EVCM12	EVCM11	EVCM10	EVCME0	EVCME1	UID[3]	UID[2]	UID[1]	UID[0]
R2A	0	0	0	0	0	0	0	0	EVCME1	0	EVCM1[5]	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

EVCME1/0	
01	Enable EVCM0[4:0] setting(R29h)
11/10	Enable EVCM1[4:0] setting(R2Ah)

VCM_En	
0	Enable VCM[5:0] setting(R13h)
1	Enable EVCM0[4:0] or EVCM1[4:0] setting

EPROM write sequence

(1)EAD=01;

Item	Instructions	Value	Note
1	Power supply, VCI=IOVCC=2.80V DDVDH: No external voltage		
2	Reset		
3	Initial code setup		
4	EPROM CONTROL (RA0)	0x00A0 0x0011	Set EPROM Write function & EPROM write address
5	DDVDH: external 7.5V		
6	Wait 10ms or more		
7	EPROM CONTROL (RA0)	0x00A0 0x0011	Set EPROM Write function & EPROM write address
8	EPROM DATA (RA1)	0x00A1 0x00A0	Set EPROM Write DATA & Set EVCME0=1, SET DATA=20h(for example data=20h).
9	Wait 1ms or more		
10	EPROM CONTROL (RA0)	0x00A0 0x0091	Set EPROM Start Write function
11	Wait 10ms or more		
12	DDVDH: no external voltage		
13	Wait 100ms or more		
14	EPROM CONTROL (RA0)	0x00A0 0x0021	Loading EPROM data
15	EPROM CONTROL (RA0)	0x00A0 0x0001	Loading EPROM data end
16	Wait 1ms or more		
17	Load data (RA2)	0x00A2 0x0001	Loading the EPROM data to replace the R29h register data. VCM_EN=1
18	Wait 1ms or more		
19	Read the data	0x00AE	See the datasheet "EPROM data write control register" section.

(2)EAD=02;

Item	Intructions	Value	Note
1	Power supply, VCI=IOVCC=2.80V DDVDH: No external voltage		
2	Reset		
3	Initial code setup		
4	EPROM CONTROL (RA0)	0x00A0 0x0012	Set EPROM Write function & EPROM write address
5	DDVD: external 7.5V voltage		

6	Wait 10ms or more		
7	EPROM CONTROL (RA0)	0x00A0 0x0012	Set EPROM Write function & EPROM write address
8	EPROM DATA (RA1)	0x00A1 0x00AB	Set EPROM Write DATA & Set EVCME1=1, SET DATA=2Bh(for example data=2bh)
9	Wait 1ms or more		
10	EPROM CONTROL (RA0)	0x00A0 0x0092	Set EPROM Start Write function
11	Wait 10ms or more		
12	DDVDH: No external voltage		
13	Wait 100ms or more		
14	EPROM CONTROL (RA0)	0x00A0 0x0022	Loading EPROM data
15	EPROM CONTROL (RA0)	0x00A0 0x0002	Loading EPROM data end
16	Wait 1ms or more		
17	Load data (RA2)	0x00A2 0x0001	Loading the EPROM data to replace the R29h register data. VCM_EN=1
18	Wait 1ms or more		
19	Read the data	0x002A	See the datasheet "EPROM data write control register" section.

(3)EAD=00;Write/Read USER ID

Item	Instructions	value	Note
1	Power supply, VCI=IOVCC=2.80V DDVDH: No external voltage		
2	Reset		
3	Initial code setup		
4	EPROM CONTROL (RA0)	0x00A0 0x0010	Set EPROM Write function & EPROM write address
5	DDVDH: external7.5V voltage		
6	Wait 10ms or more		
7	EPROM CONTROL (RA0)	0x00A0 0x0010	Set EPROM Write function & EPROM write address
8	EPROM DATA (RA1)	0x00A1 0x0083	Set EPROM Write DATA & Set EVCME0=1, SET UID=0011h(for example)
9	Wait 1ms or more		
10	EPROM CONTROL (RA0)	0x00A0 0x0090	Set EPROM Start Write function
11	Wait 10ms or more		

12	DDVDH: No external voltage		
13	Wait 100ms or more		
14	EPROM CONTROL (RA0)	0x00A0 0x0020	Loading EPROM data
15	EPROM CONTROL (RA0)	0x00A0 0x0000	Loading EPROM data end
16	Wait 1ms or more		
17	Load data (RA2)	0x00A2 0x0001	Loading the EPROM data to replace the R29h register data. VCM_EN=1
18	Wait 1ms or more		
19	Read USER ID	0x0028	Read out the USER ID.The LSB is the USER ID.

Figure 77: EPROM write sequence

FT1509 Recommended resistance and connection example

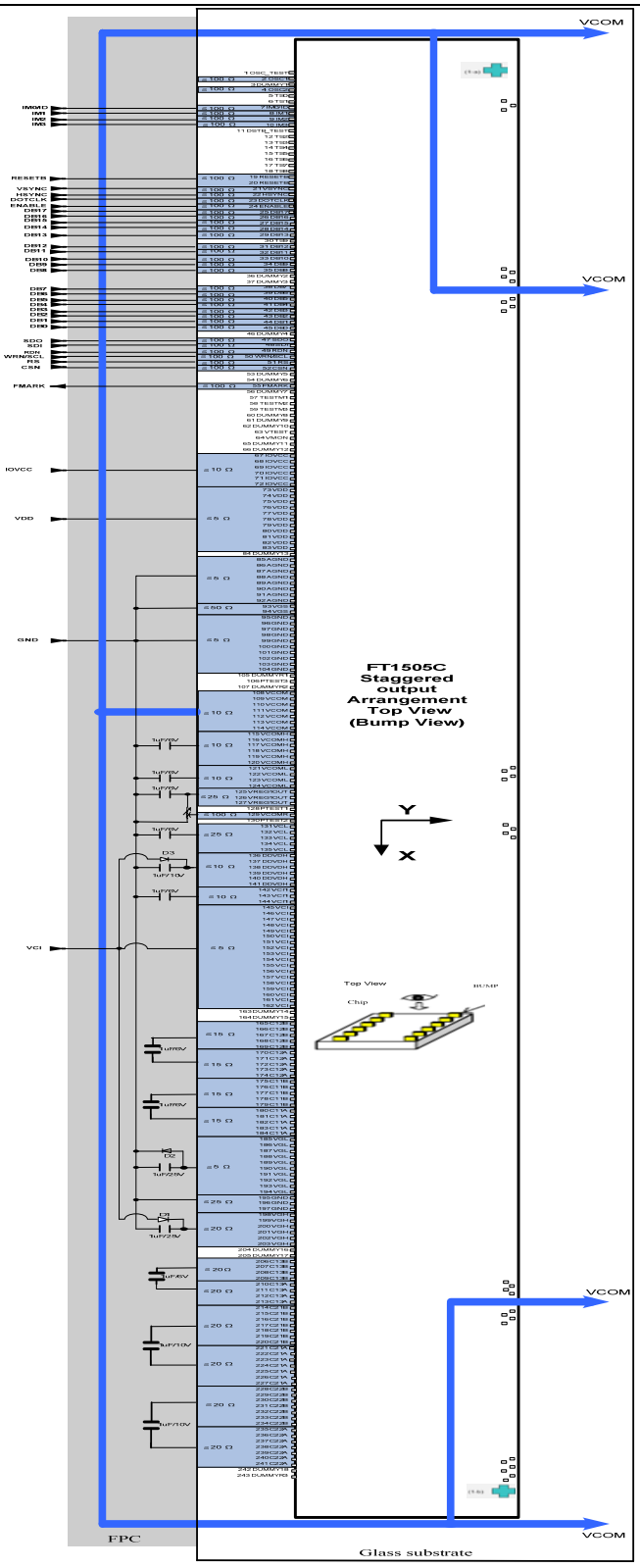

VCOM
VCOM
VCOM
VCOM
FT1505C
Staggered
output
Arrangement
Top View
(Bump View)
Y
X
Top View
Chip
BUMP
FPC
Glass substrate

Figure 78

Absolute Maximum Ratings

Table 77

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	IOVcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci -AGND	V	-0.3 ~ + 4.6	1, 3
Power supply voltage (3)	DDVDH - AGND	V	-0.3 ~ + 6.5	1, 4
Power supply voltage (4)	VGH - VGL	V	+11.0 ~ + 27.0	1, 4
Power supply voltage (5)	AGND - VGL	V	+3.0 ~ +13.0	1, 7
Power supply voltage (6)	DDVDH - VGL	V	+7.0 ~ +19.0	1, 5
Power supply voltage (7)	Vci - VGL	V	+5.5 ~ +16.8	1, 7
Input voltage	Vt	V	-0.3 ~ Vci + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 8
Storage temperature	Tstg	°C	-55 ~ + 110	1

Notes: 1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure Vci (high) ≥ GND (low) and IOVcc (high) ≥ GND (low).
3. Make sure Vci (high) ≥ AGND (low).
4. Make sure DDVDH (high) ≥ AGND (low).
5. Make sure DDVDH (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ AGND (low).
7. Make sure AGND (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

Electrical Characteristics

DC Characteristics

Table 78 (Vci = 2.4V ~ 3.3V, IOVcc = 1.65V ~ 3.3V, Ta = -40°C ~ 85°C) see Note 1

Item	Symbol	Unit	TestCondition	Min.	Typ.	Max.	Notes
Input high-level voltage	VIH	V	IOVcc = 1.65V ~ 3.3 V	0.8 x IOVcc	—	IOVcc	2, 3
Input low-level voltage	VIL	V	IOVcc = 1.65V ~ 3.3 V	– 0.3	—	0.2 x IOVcc	2, 3
Output high voltage (DB0-17 pins, FMARK)	VOH	V	IOVcc = 1.65V ~ 3.3 V IOH = -0.1mA	0.8 x IOVcc	—	—	2
Output low voltage (DB0-17 pins, FMARK)	VOL	V	IOVcc = 1.65V ~ 3.3 V IOL = 0.1mA	—	—	0.2 x IOVcc	2
I/O leak current	ILi	µA	Vin = 0 ~ IOVcc	–1	—	1	4
Current consumption: (IOVcc-GND) Normal operation mode, 262K color	IOP1	µA	fosc=358kHz (320 lines), fFLM=70Hz, IOVcc=Vci= 3.0V, Ta=25°C, RAM data: 18'h00000	—	175	295	5, 6
Current consumption: (IOVcc-GND) 8-color mode, 64-line partial display	IOP2	µA	fosc=358kHz (64 line partial), fFLM=40Hz, IOVcc=Vci= 3.0V, Ta=25°C, RAM data: 18'h00000	—	140	—	5, 6
Current consumption: (IOVcc-GND) RAM access mode 1 normal operation mode	IRAM1	mA	tCYCW=150ns, IOVcc=2.40V,Vci= 2.4V, Ta=25°C, 80-8bit I/F, TRI=1, Consecutive RAM access during display VCM1=5'h1D, AP=3'h3, BC0=0, FP=5, BP=8, gamma registor:0 (default) CL=0 (8 color)	—	2.0	—	6
Current consumption: (IOVcc-GND)+(Vci-GND) Sleep mode	ISLP	µA	Vcc=Vci=3.00V SLP='1' Ta=25c		45		
Current consumption: (IOVcc-GND)+(Vci-GND) Standby mode	ISTB	µA	Vcc=Vci=3.00V STB='1' Ta=25c		20		
Current consumption: (IOVcc-GND)+(Vci-GND) Deep Standby mode	IDST	µA	Vcc=Vci=3.00V DSTB='1' Ta=25c	—	0.1	1.0	5

DC Characteristics

Item	Symbol	Unit	TestCondition	Min.	Typ.	Max.	Notes

LCD power supply current (VCI-GND) 260k color display	I_{ci1}	mA	IOVcc=Vci=3.0V, fosc =358kHz (320 lines), fFLM=70Hz, Ta=25°C, RAM data:18'h00000, REV=0, SAP=1, AP=100, DC0=000, DC1=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 B/C=0, BT=001, VC=001, VRH=0011, VCM=100110, VDV=100000, CL=0 No load on the panel	—	2.8	3.3	5, 6
LCD power supply current (VCI-GND) 8-color mode	I_{ci2}	mA	IOVcc=Vci=3.0V, fosc =358kHz (64 lines) fFLM=40Hz, Ta=25°C, RAM data:18'h00000, REV=0, SAP=1, AP=010, DC0=001, DC1=011, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 B/C=0, BT=001, VC=001, VRH=0011, VCM=100110, VDV=011100, CL=1, PTG=10, ISC=0111 No load on the panel	—	1.0	—	5, 6
Source Output voltage dispersion	ΔVo	mV	—	—	5	—	7
Source Average output voltage variance	ΔV	mV	—	-35	—	35	8

Step-up circuit Characteristics

Table 79

Item		Unit	Test Condition	Min	Typ	Max	Notes
Step-up output voltage	DDVDH	V	IOVcc=Vci= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=001 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, I_{load1} = -1[mA]	4.57	4.84	—	11
	VGH	V	IOVcc=Vci= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=000,DC1=010 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, I_{load1} = -100[mA]	13.72	14.40	—	11
	VGL	V	IOVcc=Vci= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=000,DC1=010 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, I_{load1} = +100[mA]	-6.86	-7.13	—	11
	VCL	V	IOVcc=Vcc= 3.0V, fosc =358kHz, Ta=25°C, VC=3'h7, AP=100,SAP=1, BT=000, DC0=000,DC1=010 C11=C21=C22=1[uF] / B Characteristics, DDVDH=VGH=VGL=1[uF] / B Characteristics, No load on the panel, I_{load1} = 200[mA]	-2.25	-2.30	—	—
Input voltage	Vci	V		2.4	—	3.3	—

AC Characteristics

(Vci=2.4V ~ 3.3V, IOVcc = 1.65V ~ 3.3V, Ta = – 40°C ~ +85°C*) * see Note 1

Table 80 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
RC oscillation clock	fosc	kHz	IOVcc=Vci=3.0V 25°C	250	400	630	9

80-system Bus Interface Timing Characteristics (18/16-bit I/F)

Table 81 Normal write operation
IOVcc = 1.65V ~ 3.3V, Vci= 2.4V ~ 3.3V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure 87	125	-	-

	Read	t_{CYCR}	ns	Figure 87	450	-	-
Write low-level pulse width		PW_{LW}	ns	Figure 87	45	-	-
Read low-level pulse width		PW_{LR}	ns	Figure 87	170	-	-
Write high-level pulse width		PW_{HW}	ns	Figure 87	70	-	-
Read high-level pulse width		PW_{HR}	ns	Figure 87	250	-	-
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 87	-	-	25
Setup time	Write (RS~CSN, WRN)	t_{AS}	ns	Figure 87	0	-	-
	Read (RS~CSN, RDN)				10		
Address hold time		t_{AH}	ns	Figure 87	2	-	-
Write data setup time		t_{DSW}	ns	Figure 87	25	-	-
Write data hold time		t_{HWR}	ns	Figure 87	10	-	-
Read data delay time		t_{DDR}	ns	Figure 87	-	-	150
Read data hold time		t_{DHR}	ns	Figure 87	5	-	-

80-system Bus Interface Timing Characteristics (9/8-bit I/F)

Table 83 Normal Write function
IOVcc = 1.65V ~ 3.3V, Vci= 2.4V ~ 3.3V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure 87	70	-	-
	Read	tCYCR	ns	Figure 87	450	-	-
Write low-level pulse width		PWLW	ns	Figure 87	50	-	-
Read low-level pulse width		PWLR	ns	Figure 87	170	-	-
Write high-level pulse width		PWHW	ns	Figure 87	25	-	-
Read high-level pulse width		PWHR	ns	Figure 87	250	-	-
Write/Read rise/fall time		tWRr, WRf	ns	Figure 87	-	-	25
Setup time	Write (RS~CSN, WRN)	tAS	ns	Figure 87	0	-	-
	Read (RS~CSN, RDN)				10		
Address hold time		tAH	ns	Figure 87	2	-	-
Write data setup time		tDSW	ns	Figure 87	25	-	-
Write data hold time		tHWR	ns	Figure 87	10	-	-
Read data delay time		tDDR	ns	Figure 87	-	-	150
Read data hold time		tDHR	ns	Figure 87	5	-	-

Serial interface Timing Characteristics

Table 84 IOVcc = 1.65V ~ 3.3V, Vci = 2.4V ~ 3.3V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	Figure 88	100	-	20,000
	Read (transmitted)	t_{SCYC}	ns	Figure 88	350	-	20,000
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 88	40	-	-
	Read (transmitted)	t_{SCH}	ns	Figure 88	150	-	-
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 88	40	-	-
	Read (transmitted)	t_{SCL}	ns	Figure 88	150	-	-
Serial clock rise/fall time		t_{SCr}, t_{SCf}	ns	Figure 88	-	-	20
Chip select setup time		t_{CSU}	ns	Figure 88	20	-	-

Chip select hold time	t_{CH}	ns	Figure 88	60	-	-
Serial input data setup time	t_{SISU}	ns	Figure 88	30	-	-
Serial input data hold time	t_{SIH}	ns	Figure 88	30	-	-
Serial output data delay time	t_{SOD}	ns	Figure 88	-	-	130
Serial output data hold time	t_{SOH}	ns	Figure 88	5	-	-

Reset Timing Characteristics

Table 85 IOVcc = 1.65V ~ 3.3V, Vci= 2.4V ~ 3.3V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Resetlow-levelwidth	t_{RES}	ms	Figure89	1	—	—
Resetrisetime	t_{rRES}	µs	Figure89	—	—	10

LCD driver output Characteristics

Table 88

Item	Symbol	Unit	Test condition	Min	Typ	Max	Note
Source Driver output delay time	t_{dds}	µs	Vci=IOVcc =3.0V, DDVDH=5.5V, VREG1OUT=5.0V, fosc=358kHz (320 lines), Ta=25°C REV=0, SAP=010, AP=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 Load resistance R=10kΩ, Load capacitance C=20pF Time to reach the target voltage level ±35mV from the timing of Vcom polarity inversion Transition from the same grayscale level at all source pins	—	17	—	10
VCOM output delay time	t_{ddv}	µs	Vci=IOVcc =3.0V, DDVDH=5.5V, VREG1OUT=5.0V, fosc =358kHz (320 lines), Ta=25°C REV=0, SAP=010, AP=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 Load resistance R=100Ω, Load capacitance C=20pF Time to reach the target voltage level ±35mV from the timing of Vcom polarity inversion Transition from the same grayscale level at all source pins	—	17	—	11

Table 89 Display test

Item	Symbol	Unit	TestCondition	Min.	Typ.	Max.	Notes
LCD power supply current Partial 32-Line Display Load 2.8" Panel White pattern	$I_{partial1}$	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010,	—	3.7	—	

LCD power supply current Partial 32-Line Display Load 2.8" Panel Black Pattern	$I_{partial2}$	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010,	—	4.5	—	
LCD power supply current Partial 32-Line Display Load 2.8" Panel Snow Pattern	$I_{partial3}$	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010,	—	4.2	—	
LCD power supply current 8-color mode Load 2.8" Panel Black pattern	$I_{partial1}$	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010, R91=0300, R98=0103	—	7	—	
LCD power supply current Normal Display Load 2.8" Panel Black Pattern	$I_{partial2}$	mA	IOVcc=Vci=2.8V, fFLM=62Hz, Ta=25°C, SAP=1, BT=001, APE=1, AP=001, DC0=100, DC1=010, VC=000, VRH=1000, VDV=0x15, VCM=0x21, RC=010, R91=0300, R98=0103	—	10	—	

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following figures illustrate the configurations of input, I/O, and output pins.

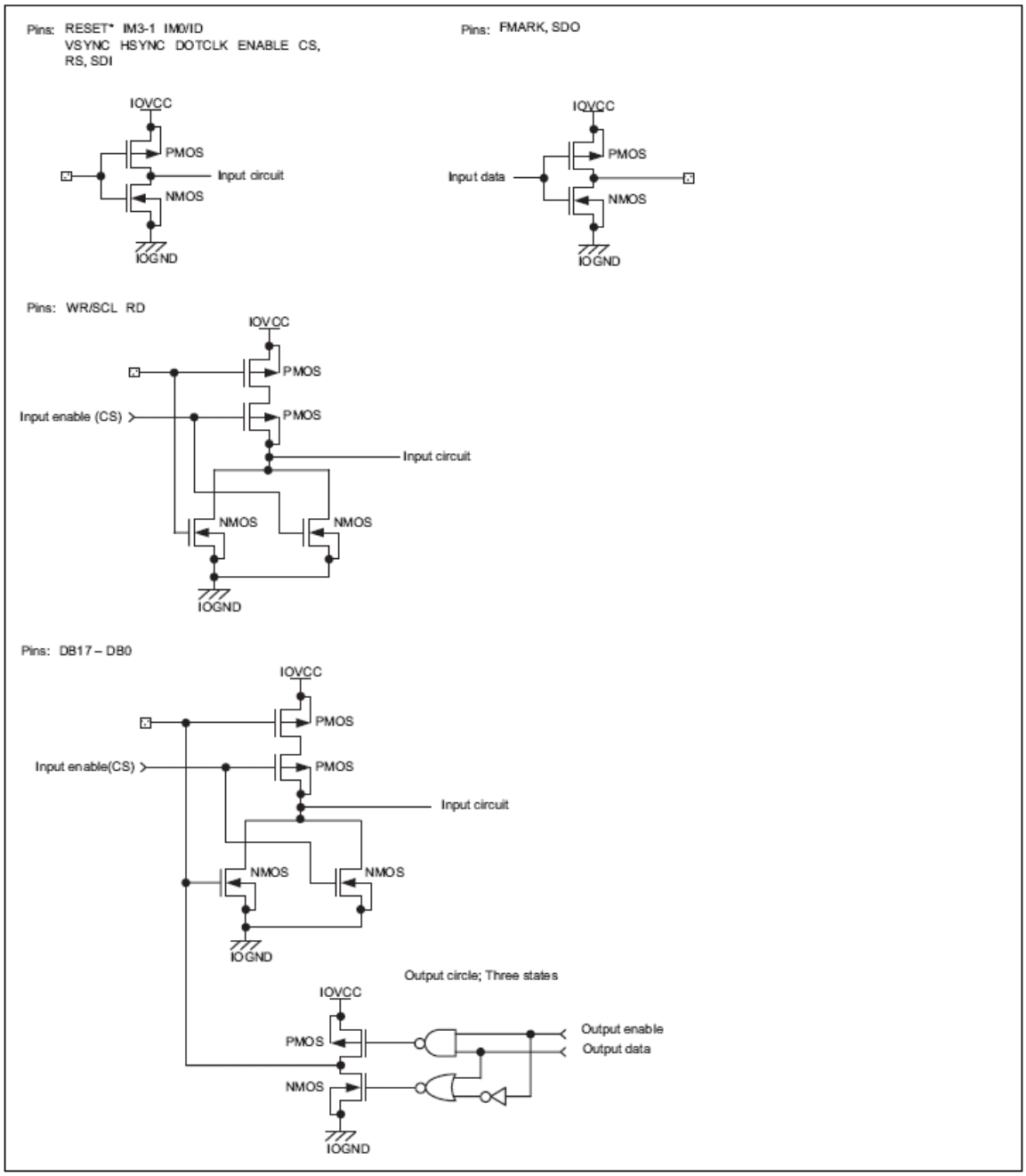


Figure 79

3. The TEST1, TEST2 pins must be grounded (GND). The IM3/2/1 and IM0/ID pins must be fixed at either IOVcc or GND.
4. This excludes the current in the output-drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CSN pin is “High” or “Low” while not accessing via interface pins.
6. The relationship between voltages and the current consumption is as follows.

T.B.D.

Figure 80

7. The output voltage deviation is the difference in the voltages from adjacent source pins for the same display data. This value is shown just for reference.
8. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for each chip with same display data.
9. This applies to internal oscillators when using external oscillation resistor Rf.

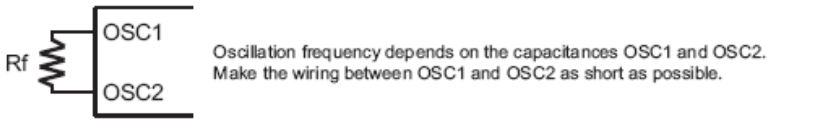


Figure 81

10. Just for reference. The wiring resistance when the FT1509 is mounted on the glass substrate is not taken into consideration. No load is applied on pins except those for measurement. See the reference data “Load current characteristics (T.B.D.)”.
11. Just for reference. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality of display on the actual panel in use.
12. Just for reference. The “DDVDH-VREGOUT≥0.5V” should be mostly followed in normal case, but the actual DDVDH will be a little lower than idea DDVDH due to different loading pattern, so it may be little loose sometimes, meanwhile that “DDVDH-VREG1OUT>0.3V” should be always followed in all actual case.

T.B.D.

Figure 82

Test Circuits

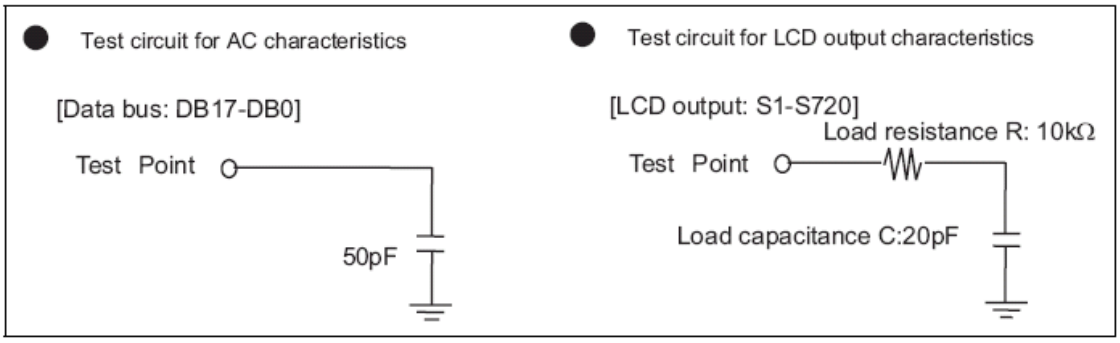


Figure 83

Timing Characteristics 80-system Bus Interface

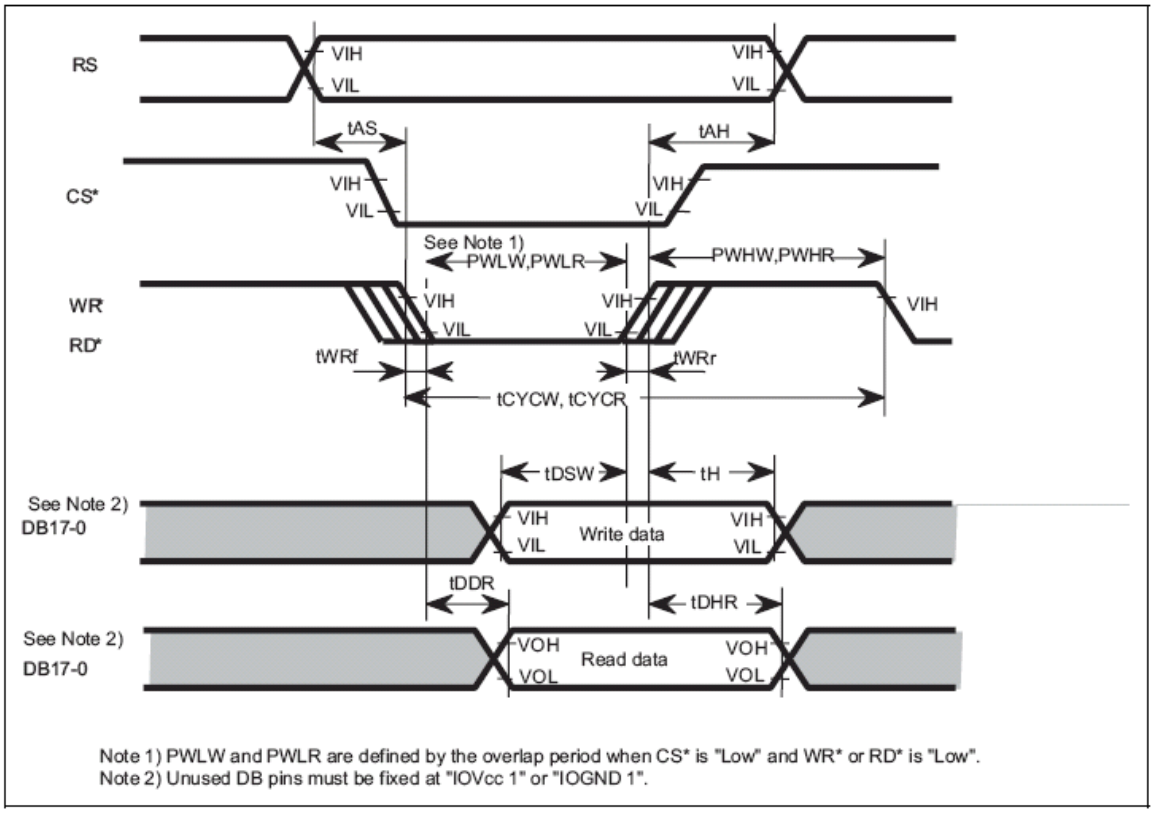


Figure 84

Clock synchronous serial interface

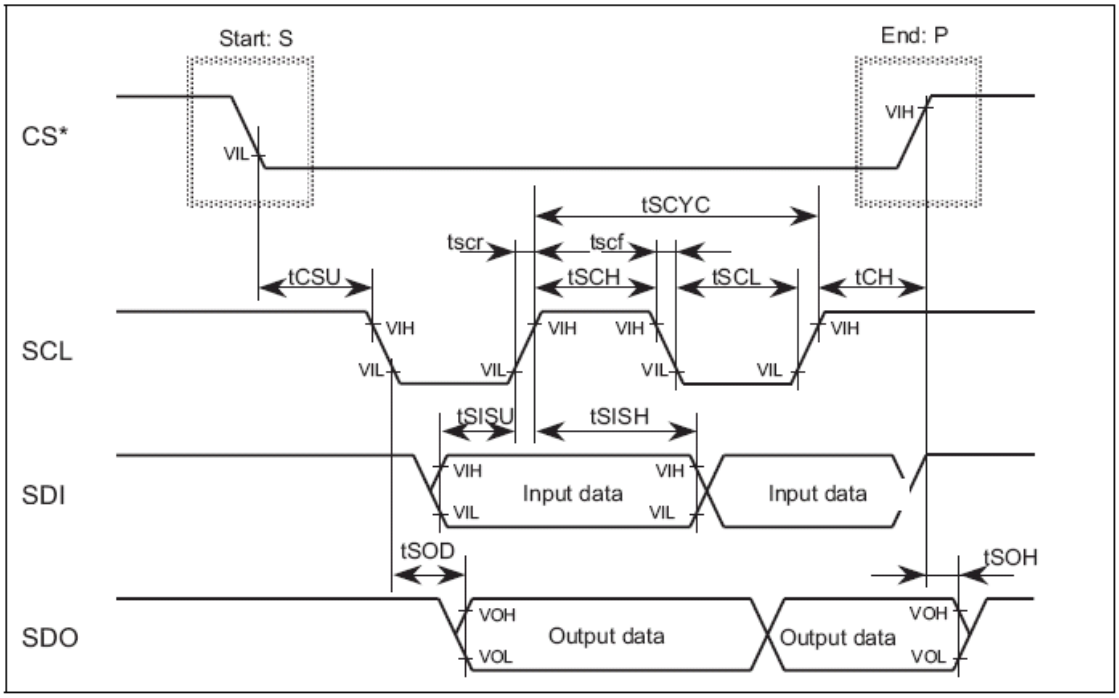


Figure 85

Reset operation

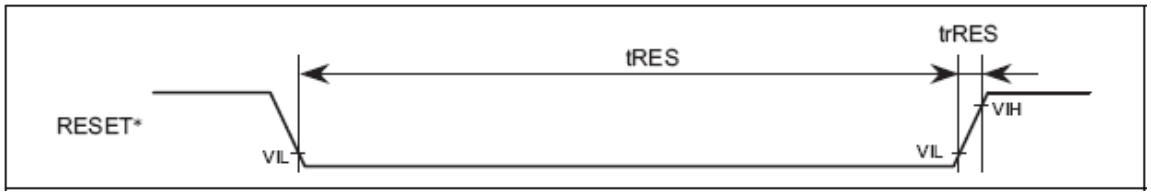


Figure 86

External display interface

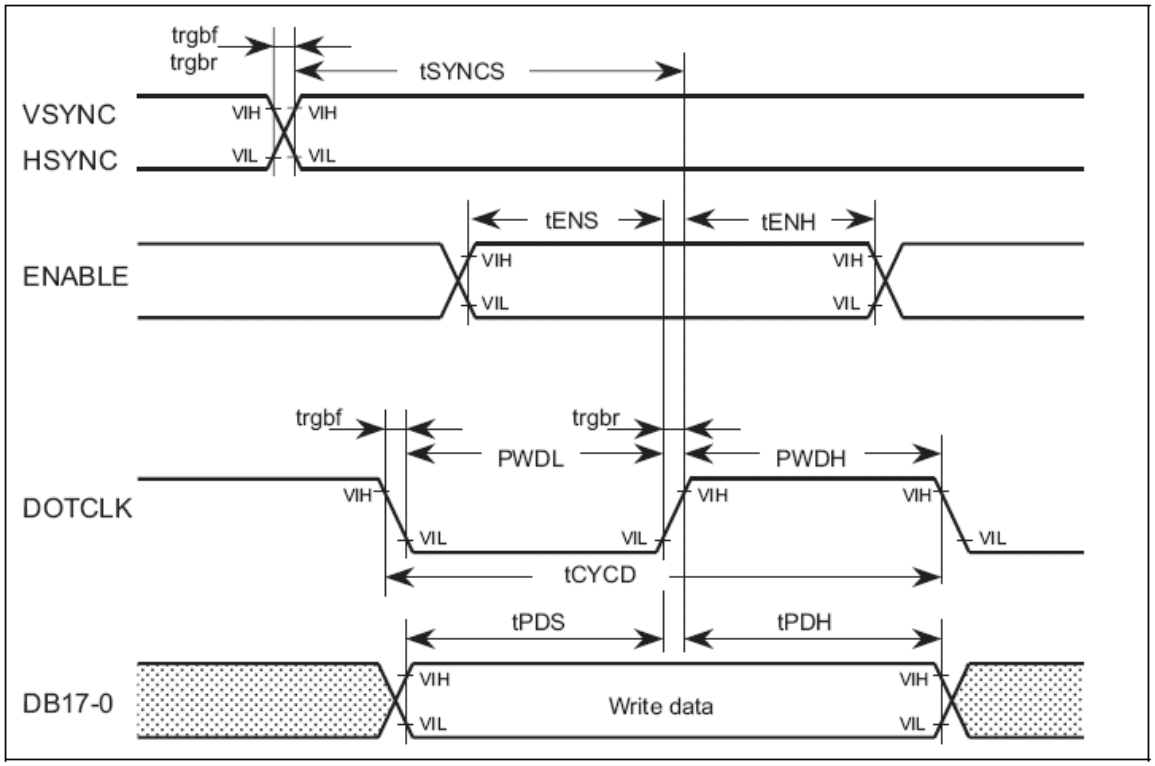


Figure 87

LCD driver outputs

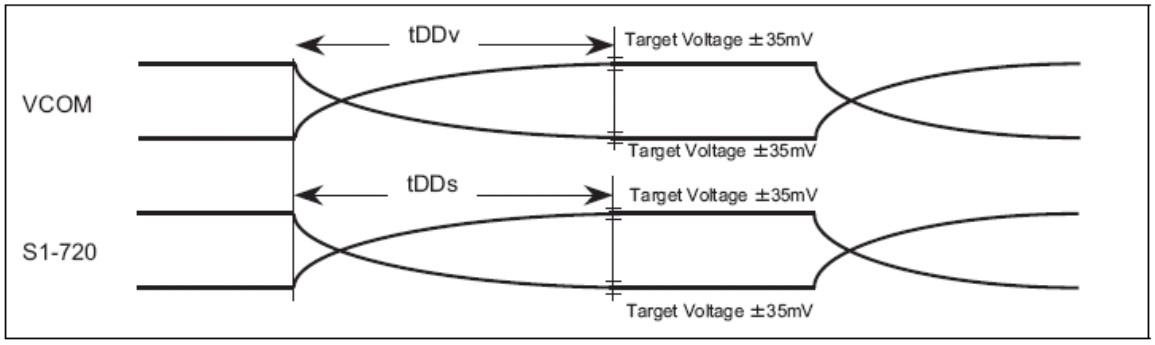


Figure 88

**** May be revised without notice**

REVISION TABLE

version	Revisions	Date
0.5	● Add “Content Adaptive Backlight Control” function ● Add “Edge enhancement” function The above is the difference comparing with FT1505C.	2008-08-01
0.6	● Page 8: Update block diagram ● Page 14: Update Pad arrangement Top view ● Page 15~Page 29: Update pad coordinate	2008-9-9
0.65	● Page 14: correct bump size ● Remove OSC2 pin. OSC1 for external clock input not support external Resistor (Page 8 and Page 10, page 52) ● Add VCILVL and VCC description on page 11	08-09-12
0.70	● Update Table 36 VDV: VCOM amplitude on page 48	08-10-08

END OF DATABOOK