

Wide Input Range Synchronous Buck Controller

Features

- Wide Input Voltage Range: 8V ~ 30V
- Up to 93% Efficiency
- Programmable Switching Frequency up to 500KHz
- No Loop Compensation Required
- CC/CV control
- Programmable CC Current
- Thermal Shutdown
- Available in SOP8L Package

Description

The FT1705 is a synchronous step down regulator with CC control from a high voltage input supply. Operating with an input voltage range of 8V ~ 30V, the FT1705 achieves 4.5A continuous output current with excellent load and line regulation. The switching frequency is programmable from 130KHz to 500KHz and the synchronous architecture provides for highly efficient designs. Current mode operation provides fast transient response and eases loop stabilization.

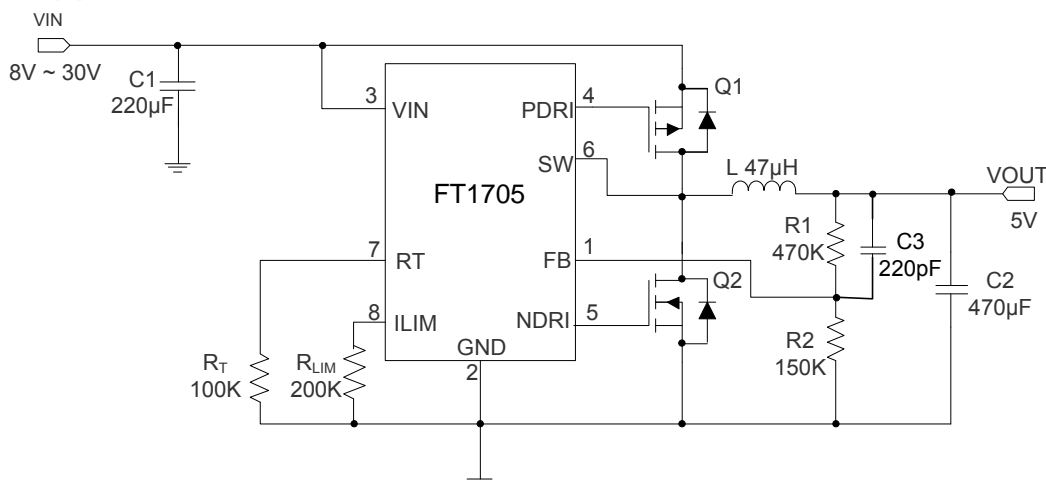
Applications

- Car Charger / Adaptor
- LED Driver
- Pre-Regulator for Linear Regulators
- Distributed Power Systems
- Battery Charger

The FT1705 requires a minimum number of readily available standard external components. Other features include cable compensation, programmable current limit and thermal shutdown.

The FT1705 converters are available in the industry standard SOP8L packages.

Typical Application Circuit

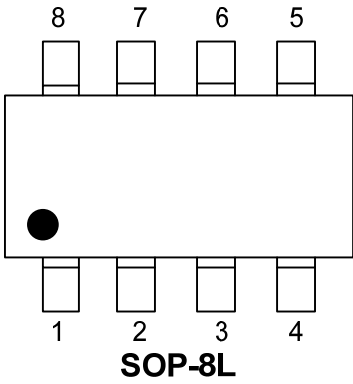


*The output voltage is set by R1 and R2: $V_{OUT} = 1.21V \cdot [1 + (R1/R2)]$.

* R_T : R_T is optional. FT1705 can work when keeping R_T pin floating. The default frequency is 130KHz. The switch frequency is set by R_T : $R_T(k\Omega) = 4800000 / (200 \cdot f_{OSC}(kHz) - 24000)$

*The maximum output current is set by R_{LIM} : $R_{LIM}(k\Omega) = 23 \cdot I_{MAX}(A)$.

Pin Assignment and Description

TOP VIEW		PIN	NAME	DESCRIPTION
 <p>The diagram shows the top view of an SOP-8L package. It is a rectangular package with eight pins. Pins 1, 2, 3, and 4 are on the bottom edge, and pins 8, 7, 6, and 5 are on the top edge. A black dot is located on the left side of the package, between pins 1 and 8.</p>	8	1	FB	Feedback
	7	2	GND	Ground
	6	3	VIN	Input Supply
	5	4	PDRI	PMOS Gate Drive
		5	NDRI	NMOS Gate Drive
		6	SW	Switch Node
		7	RT	Frequency Setting
		8	ILIM	CC Current Setting

Absolute Maximum Ratings (Note 1)

- Input Supply Voltage – 0.3V ~ 35V
- PDRI PIN Voltage..... – 0.3V ~ 35V
- FB, ILIM, RT, NDRI Voltages..... – 0.3V ~ 6V
- SW Voltage – 0.3V ~ (VIN + 1V)
- Operating Temperature Range(Note 2)..... –40℃ ~ +85℃
- Junction Temperature..... +150℃
- Storage Temperature Range..... – 65℃ ~ +150℃
- Lead Temperature (Soldering, 10 sec)..... +265℃

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The FT1705 is guaranteed to meet performance specifications from 0℃ to 70℃. Specifications over the –40℃ to 85℃ operating temperature range are assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics

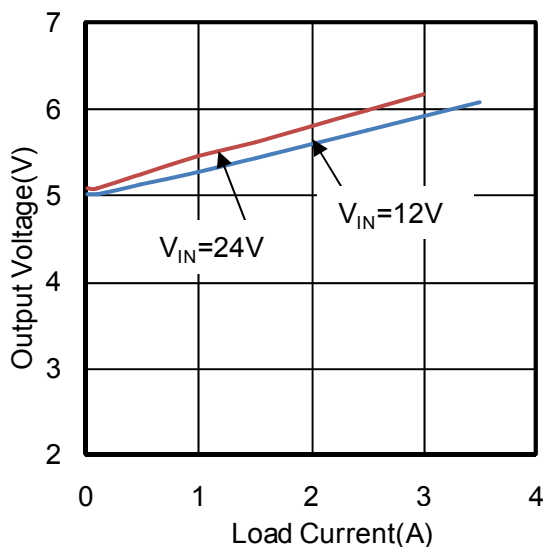
Operating Conditions: $T_A=25^{\circ}\text{C}$, $V_{IN} = 12\text{V}$, $R1 = 470\text{K}$, $R2 = 150\text{K}$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		8		30	V
I_Q	Quiescent Current	$V_{OUT} = 5\text{V}$		14		mA
V_{UVLO}	Input UVLO Threshold			4.35		V
ΔV_{UVLO}	UVLO Hysteresis			200		mV
V_{OVLO}	OVLO Threshold			32.5		V
ΔV_{OVLO}	OVLO Hysteresis			2.5		V
V_{RT}	RT Pin Voltage			0.6		V
V_{FB}	Regulated Voltage			1.21		V
I_{FB}	Feedback Pin Input Current				0.05	μA
f_{OSC}	Oscillator Frequency Range	Float RT Pin		130		kHz
f_{OSC_MAX}	Maximum Oscillator Frequency			500		kHz
DC	Max Duty Cycle				100	%
I_{LIM}	Current Limit Sense Pin Source Current		7	8.5	10	μA
T_{SD}	Thermal Shutdown	Temperature Rising		145/110		$^{\circ}\text{C}$

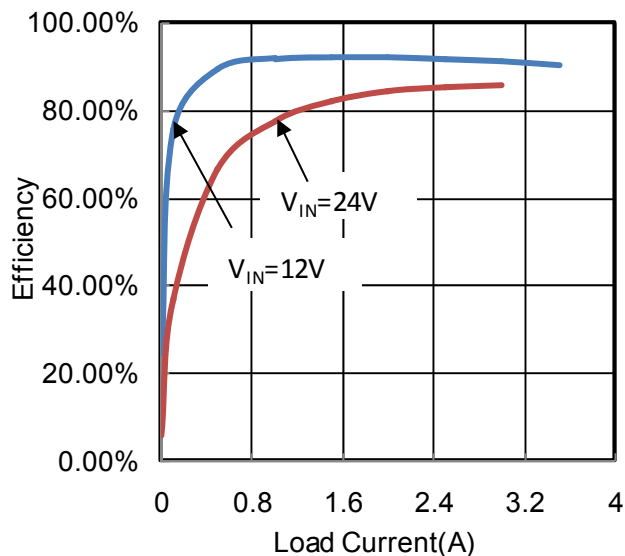
Typical Performance Characteristics

Operating Conditions: $T_A=25^{\circ}\text{C}$, $V_{IN}=12\text{V}$, $R1=470\text{K}$, $R2=150\text{K}$, unless otherwise specified.

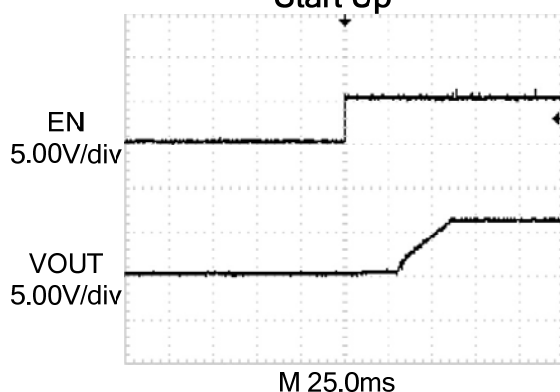
**Output Voltage vs Load Current
(with Cable Compensation)**



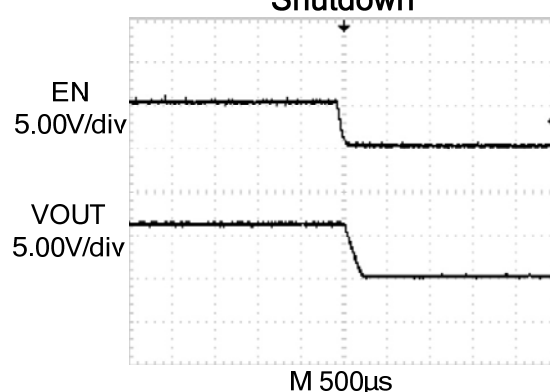
Efficiency vs Load Current



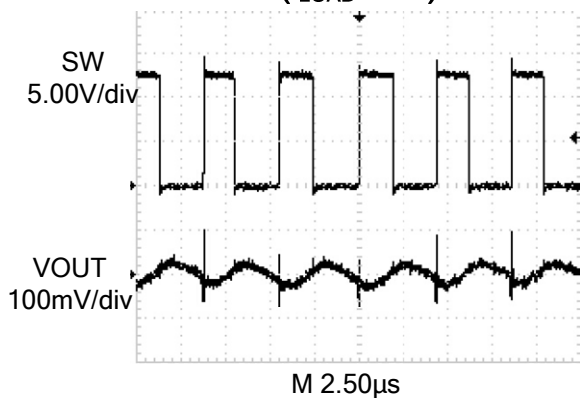
Start Up



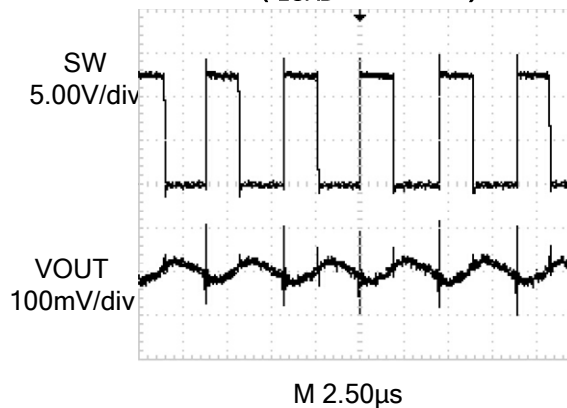
Shutdown

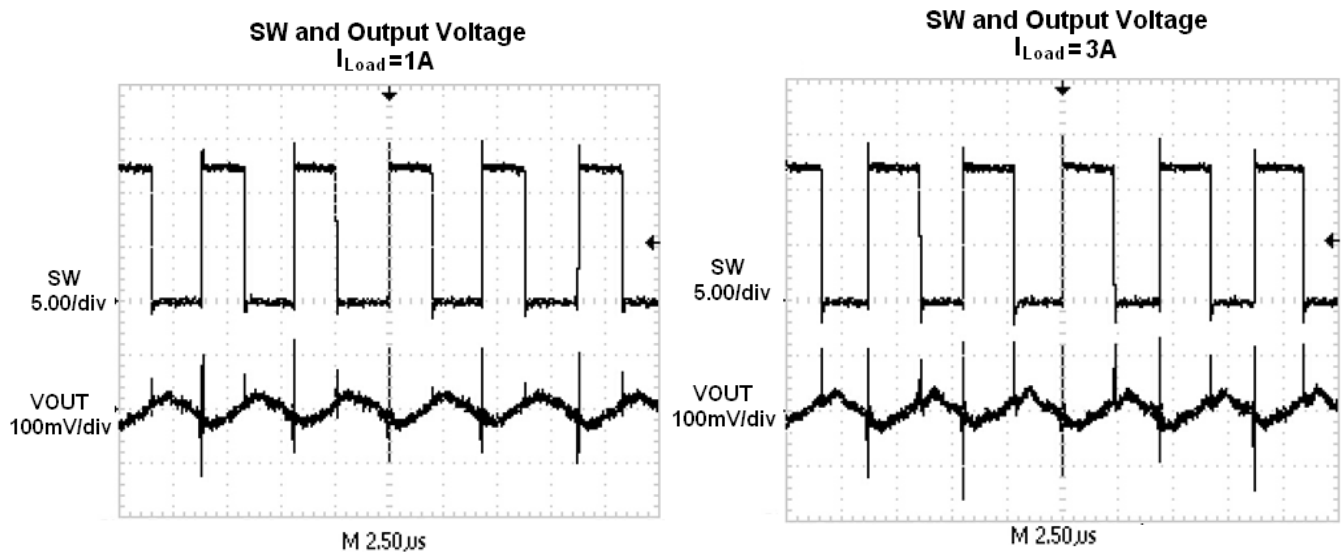


**SW and Output Voltage
($I_{LOAD}=0\text{A}$)**



**SW and Output Voltage
($I_{LOAD}=100\text{mA}$)**





Pin Functions

FB (Pin 1): Feedback Pin. Receive the feedback voltage from an external resistive divider across the output. The output voltage is set by R1 and R2: $V_{OUT} = 1.21V \cdot [1 + (R1 / R2)]$.

GND (Pin 2): Ground Pin.

VIN (Pin 3): Main power supply Pin.

PDRI (Pin 4): the drive for the high-side P-channel MOSFET switch.

NDRI (Pin 5): the drive for the low-side N-channel MOSFET switch.

SW (Pin 6): Switch Node.

RT (Pin 7): The internal oscillator is set with a single resistor between this pin and the GND.

ILIM (Pin 8): Set the maximum output current with a resistor between this pin and GND.

The schematic diagram illustrates a buck converter system with a 1.21V LDO regulator. The circuit is powered by VIN (pin 3) and GND (pin 2). The LDO regulator provides a 1.21V output (Vbias) to the VCC UVLO and THERMAL SHUTDOWN blocks. The VCC UVLO block is connected to the VCC pin (pin 4) and the THERMAL SHUTDOWN block. The THERMAL SHUTDOWN block is connected to the VCC pin (pin 4) and the LOGIC block. The OSCILLATOR block is connected to the RT pin (pin 7) and the LOGIC block. The LOGIC block contains a DrvP and DrvN output, which are connected to the DRIVER block. The DRIVER block is connected to the SW pin (pin 6) and the NDRI pin (pin 5). The REGULATION COMPARATOR block is connected to the FB pin (pin 1) and the LOGIC block. The CURRENT LIMIT COMPARATOR block is connected to the ILIM pin (pin 8) and the LOGIC block. The LOGIC block also contains a ZERO CURRENT DETECT block. The circuit includes a CCP capacitor, a Vref=1.21V reference voltage, and a VCC pin (pin 4) connected to the SW pin (pin 6) and the NDRI pin (pin 5).

The FT1705 operates by a constant frequency, current mode architecture. The output voltage is set by an external divider returned to the FB pin. An error amplifier compares the divided output voltage with a reference voltage of 1.21V and adjusts the peak inductor current accordingly.

The total power dissipation in FT1705 is limited by a thermal protection circuit. When the device temperature rises to approximately +145°C, this circuit turns off the output, allowing the IC to cool. The thermal protection circuit can protect the device from being damaged by overheating in the event of fault conditions. Continuously running the FT1705 into thermal shutdown degrades device reliability.

Current limit detection occurs during the off-time by monitoring the current through the low-side switch using an external resistor, R_{LIM} . The current limit value is defined by R_{LIM} . If during the off-time the current in the low-side switch exceeds the user defined current limit value, the next on-time cycle is

immediately terminated. Current sensing is achieved by comparing the voltage across the low side FET with the voltage across the current limit set resistor R_{LIM} . For example, the current limit value is 4.5A by the $R_{LIM} = 100K$. The current limit value rises when the set resistor R_{LIM} rises. The maximum output current is set by R_{LIM} : $R_{LIM} (k\Omega) = 23 \cdot I_{MAX} (A)$.

Oscillator Frequency

The FT1705 oscillator frequency is set by a single external resistor connected between the RT pin and the GND pin. The resistor should be located very close to the device and connected directly to the pins of the IC (RT and GND). An internal amplifier holds the RT pin at a fixed voltage typically 0.6V. The oscillator frequency rises when the resistor R_T falls. To determine the timing resistance for a given switching frequency, use the equation below:

$$R_T(k\Omega) = 4800000 / (200 \cdot f_{OSC}(kHz) - 24000)$$

Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. For most applications, a resistor in the 10k Ω to 1M Ω range is suggested for R2. R1 is then given by:

$$R1 = R2 \cdot [(V_{OUT} / V_{REF}) - 1]$$

where V_{REF} is 1.21V.

Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the FT1705 integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Choose the proper feedback resistance values for cable compensation refer to the curve in Figure 1. The delta VOUT voltage rises when the feedback resistance R2 value rises, use the equation below:

$$\Delta V_{OUT}(V) = R2(k\Omega) \cdot I_{OUT}(A) / 1100$$

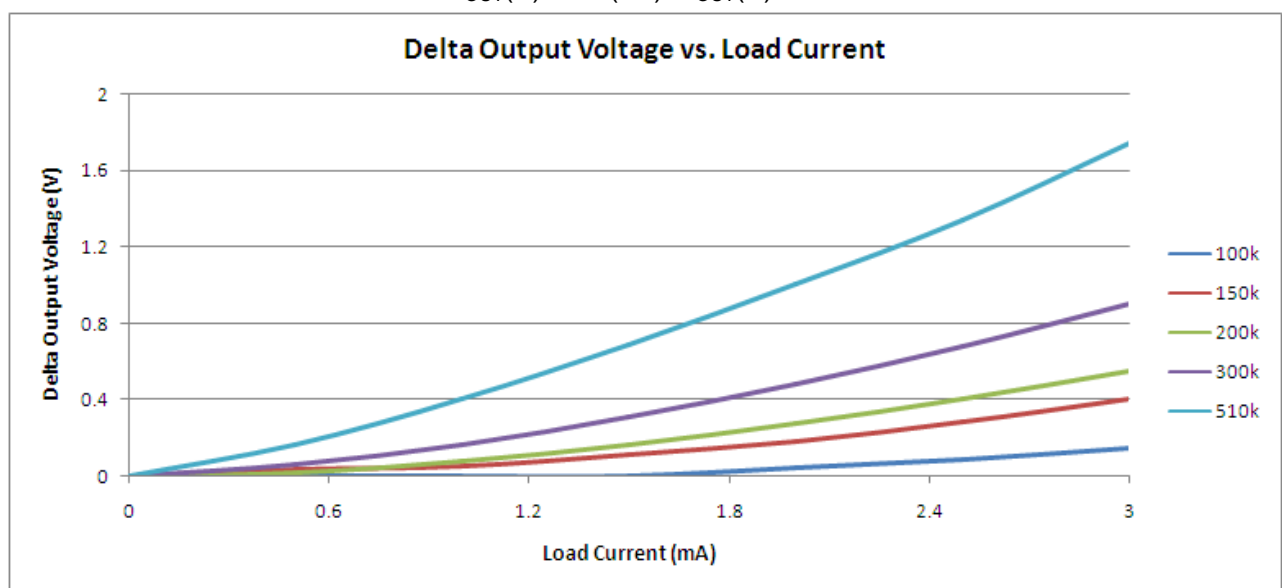


Figure 1. Delta Output Voltage vs Load Current

Inductor Selection

For most applications, the value of the inductor will fall in the range of 4.7μH to 47μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is $\Delta I_L = 1800\text{mA}$ (40% of 4.5A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 6.3A rated inductor should be enough for most applications (4.5A + 1800mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the FT1705 requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN} . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \left[\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}} \right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: $\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$ where $L1$, $L2$, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground. The resulting $\Delta Q/\Delta t$ is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L . In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$. The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Board Layout Suggestions

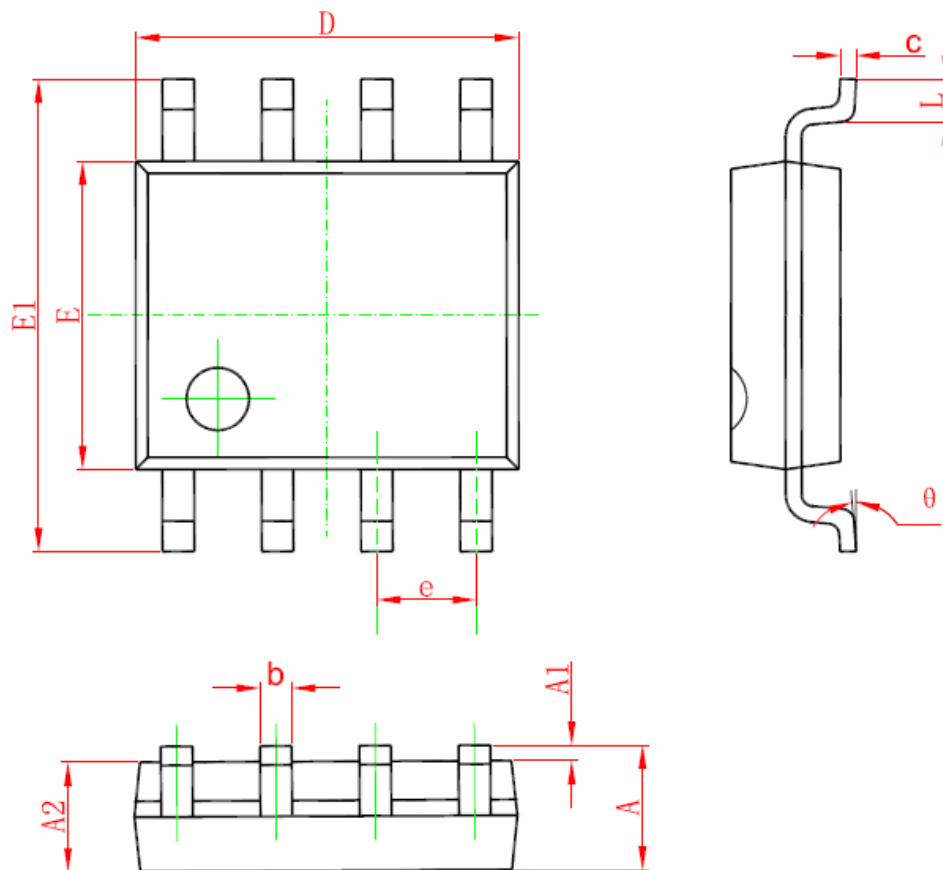
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the FT1705. Check the following in your layout.

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins (V_{IN} and GND).
3. SW node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW node to prevent stray capacitive noise pick-up.

Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.

Packaging Information

SOP-8L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Subject changes without notice.