Product Data Sheet

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FT5302

Capacitive Touch Panel controller

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Index

1. Description

FT5302 series ICs are single chip capacitive touch panel controller ICs with a built-in 8 bit Micro-controller unit (MCU). It adopts the mutual capacitance approach, which supports true multi-touch capabilities. In conjunction with a mutual capacitive touch panel, FT5302 facilitates user friendly input functions, which can be used for portable devices, such as cellular phones, digital cameras, and notebook personal computers.

2. Typical Applications

FT5302 accommodates a wide range of applications from with a set of buttons up to a 2D touch sensing device.

- Mobile phones, smart phones, MIDs
- Portable MP3 and MP4 media players
- Navigation systems, GPS
- Netbook
- Game consoles
- Car applications
- POS (Point of Sales) devices

3. Features

- Mutual capacitive sensing techniques
- True multi-touch with up to 5 points of absolution X and Y coordinates
- Immune to RF interferences
- Auto calibration: Insensitive to capacitance and environmental variations
- Supporting up to 20 transmit lines and 12 receive lines
- Supporting up to 7” touch screen (from 4.3” to 7”)
- Fully programmable scan sequences with individually adjustable receive lines and transmit lines to support various of applications
- Scan rate larger than 60Hz
- Touch resolution of 300 dots per inch (dpi) or higher -- depending on the panel size
- SPI/I2C/UART interfaces
- Operating voltage: 2.8V ~ 3.6V

- Capable of driving single channel (transmit/receive) resistance: ~ 15K Ω
- Capable of supporting single channel (transmit/receive) capacitance: 60 pF
- The optimal sensing mutual capacitor: 1pF~2.5pF
- Individual IO power supply from 1.8V~3.3V
- The accuracy of the ADC is 12bit
- Built-in MCU with 20KB of program SRAM, 4KB of data SRAM and 256B internal data space
- 11 internal interrupt sources and 2 external interrupt sources
- 3 operating modes

  Active

  Monitor

  Hibernate
- Operating temperature range: -40°C ~ +85°C
- System can be booted from multiple sources:

  Internal non-volatile memory
  An external host processor

4. Functional Description

4.1. Architectural Overview

Figure 4-1 shows the overall architecture for FT5302.

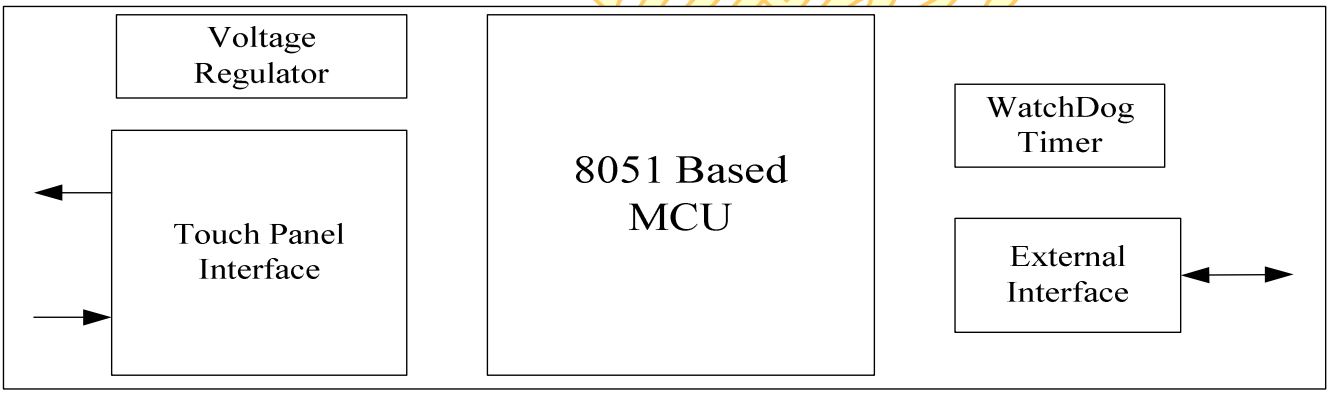


Figure 4-1 FT5 system architecture diagram

FT5302 can be divided into the following functional groups:

- Touch panel interface circuits

  The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So, it supports both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces, which will be explained in detail in a later section.

- 8051 based MCU

  This MCU is 8051 compatible with some enhancements. For example, larger program and data memories are supported. In addition, a Multiplier Accumulator (MAC) unit is implemented to speed up the touch detection algorithms. Furthermore, a One Time Programmable (OTP) is implemented to store programs and some key parameters.

  Complex signal processing algorithms are implemented with firmware running on this MCU to further process the received signals in order to detect the touches reliably. Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

  The MCU executes the program stored in the on chip program memory (SRAM). Upon power-up, the program can be downloaded (booted) from the following three sources:

  On chip OTP

  The FLASH connected to the host processor

  The detailed boot procedure will be discussed later

- External Interface

  The SPI or I2C is supported by different package.

  INT: an interrupt signal to inform the host processor that touch data is ready for read

  WAKE: an interrupt signal for the host to change F5302 from Hibernate to Active mode

- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input 3.3V supply

4.2. MCU

This section describes some critical features and operations supported by the 8051 compatible MCU. Figure 4-2 shows the overall structure of the MCU block. In addition to the 8051 compatible MCU core, we have added the following circuits:

MAC: A 16x8 multiplier with a 32 bit accumulator

Program memory: 20KB SRAM

Data memory: 4KB SRAM

Real time clock (RTC): A 32KHz RC oscillator

Timer: A number of timers are available to generate different clocks

Master clock: A 27MHz RC oscillator

Clock Manager: To control various clocks under different operation conditions of the system

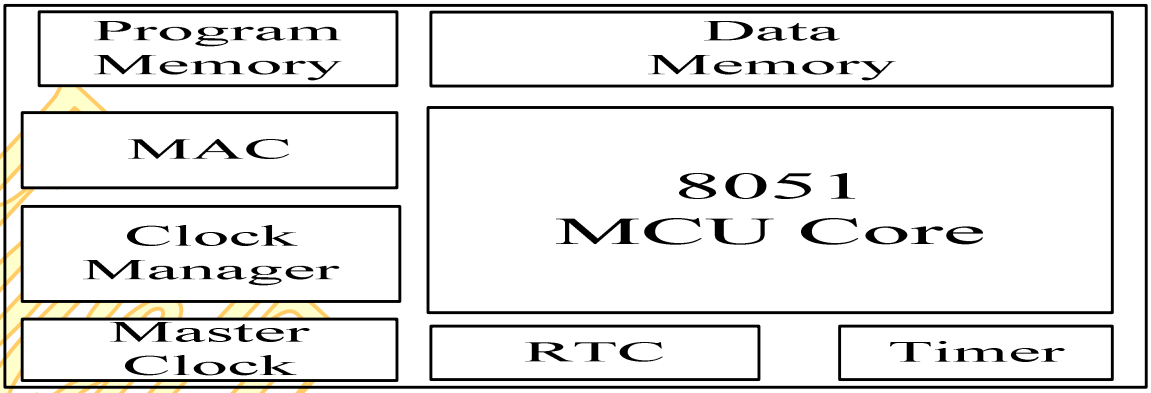


Figure 4-2 MCU block diagram

4.3. Operation Modes

FT5302 operates in the following three modes:

Active

Monitor

Hibernate

Active mode**:** When in this mode, FT5302 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT5302 to speed up or to slow down. The minimum scan period is 12 ms per frame.

Monitor mode**:** When in this mode, FT5302 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5302 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

Hibernate mode**:** In this mode, the chip is placed in a power down mode. It shall only respond to the "WAKE" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

4.4. Boot

Upon power up, FT5302 shall load the program onto the program memory and start executing the program. This is called the boot procedure. The program can be booted with the following two methods:

- From an internal non-volatile memory
- From the Host through a serial interface

The user can select one of the above boot methods by configuring MSET_N[1:0] pins and the INT pin. The following

table shows the configuration of these pins and the corresponding boot method. A pull up resistor is connected to the MSET_N[1:0] port, respectively. The voltage of the IO is VDDA if it is NC.

MSET_N[1:0]	INT	Boot #	Boot method
2'b11	N/A	0	From OTP to program SRAM with the DMA method
2'b10	N/A	1	From a host processor to program SRAM via I2C
2'b01	LOW	3	From a host processor to program SRAM via SPI0

4.5. Host Interface

Figure 4-3 shows the interface between a host processor and FT5302. The interface for other FT5302 series chips is identical. This interface consists of the following three sets of signals:

- Serial interface
- Interrupt from FT5302 to the host
- Wake up signal from the host to FT5302

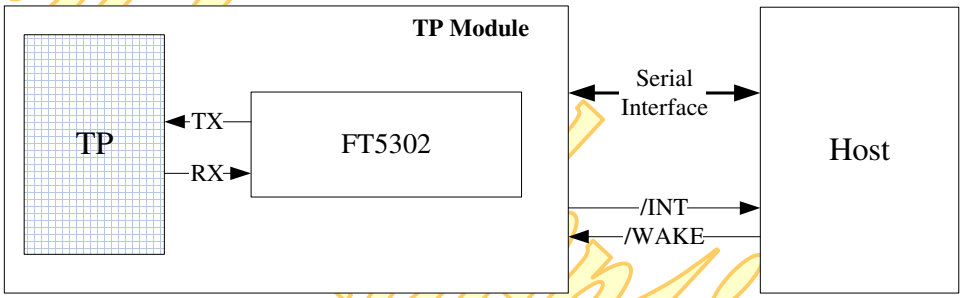


Figure 4-3 Host interface diagram

Three serial interfaces, SPI and I2C are supported. The details of this interface are described in detail in Section 4.6. The interrupt signal, /INT, is used for FT5302 to inform that host that data are ready for the host to receive. The /WAKE signal is used for the host to wake up FT5302 from the Hibernate mode. Upon exiting the Hibernate mode, FT5302 shall enter the Active mode.

4.6. Serial Interface

FT5302 supports the following interfaces, which can be used by a host processor or other devices: SPI and I2C

4.6.1. SPI

SPI is a 4 wire serial interface. The following is a list of the 4 wires:

SCK: serial data clock

MOSI: data line from master to slave

MISO: data line from slave to master

SLVESEL: active low select signal

SPI transfers data at 8bit packets. The phase relationship between the data and the clock can be defined by the two registers: phase and polck. Some data transfer examples can be found in Figure 4-4 to Figure 4-7.

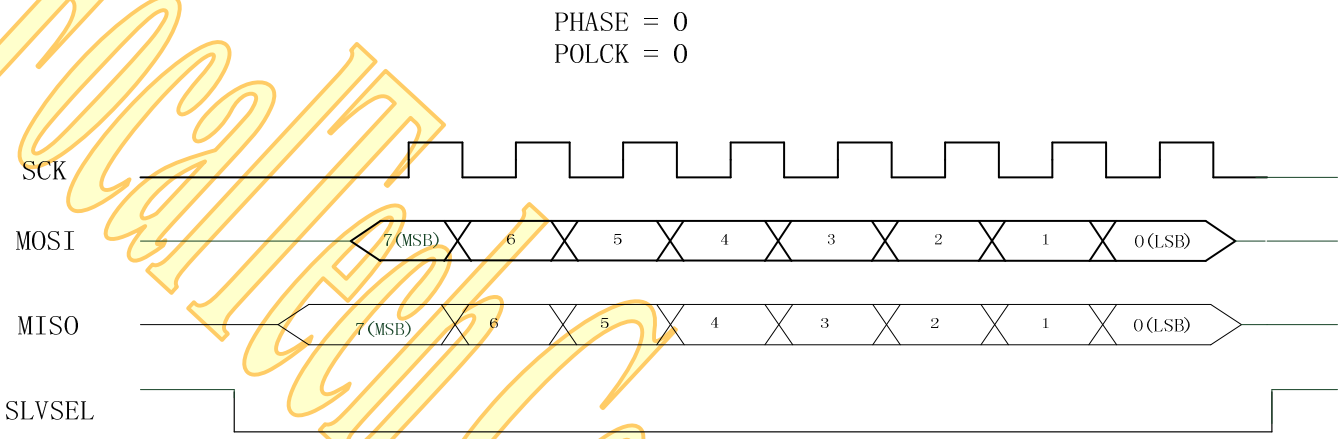


Figure 4-4 SPI data transfer format (Phase=0, POLCK=0)

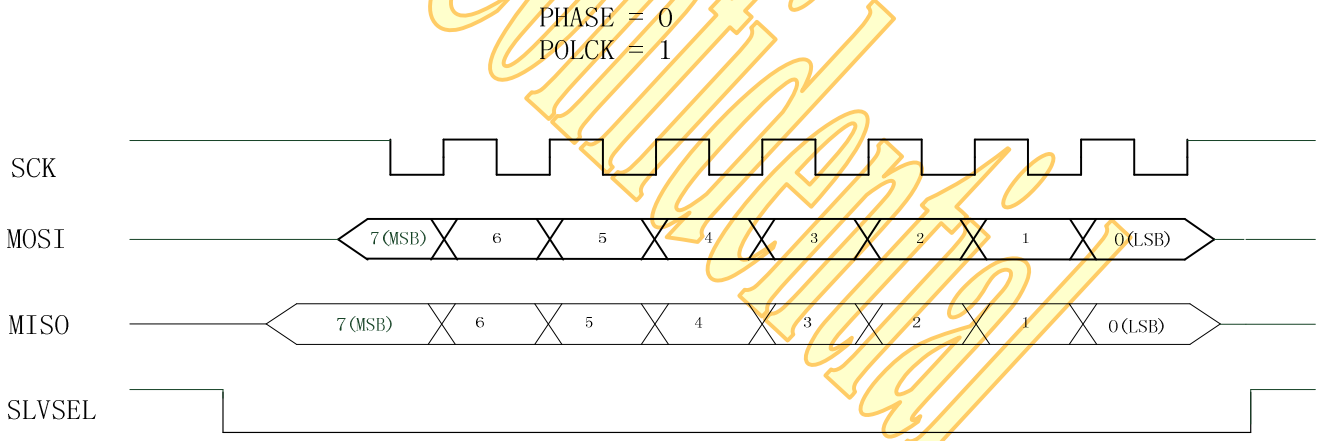


Figure 4-5 SPI data transfer format (PHASE=0, POLCK=1)

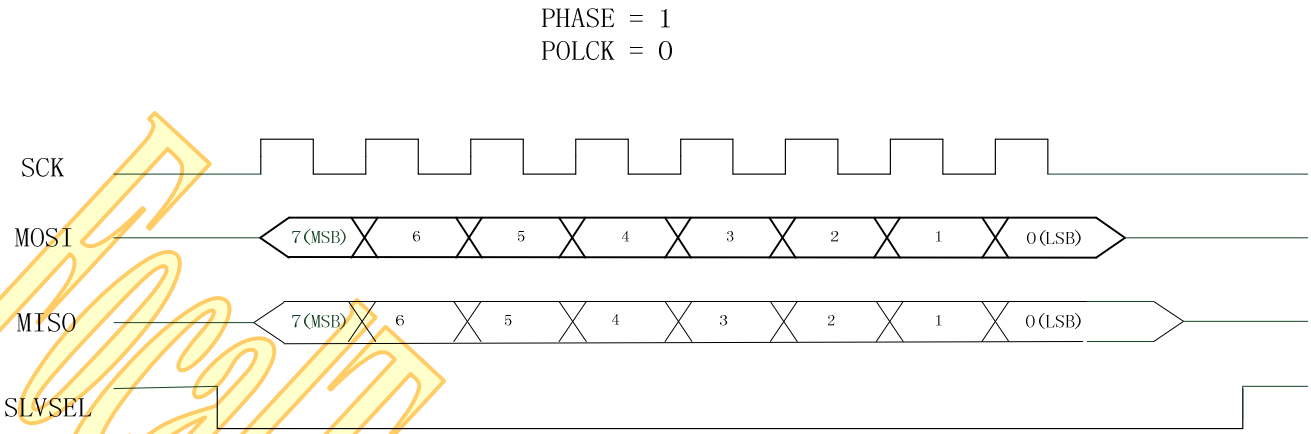


Figure 4-6 SPI data transfer format (Phase=1, POLCK=0)

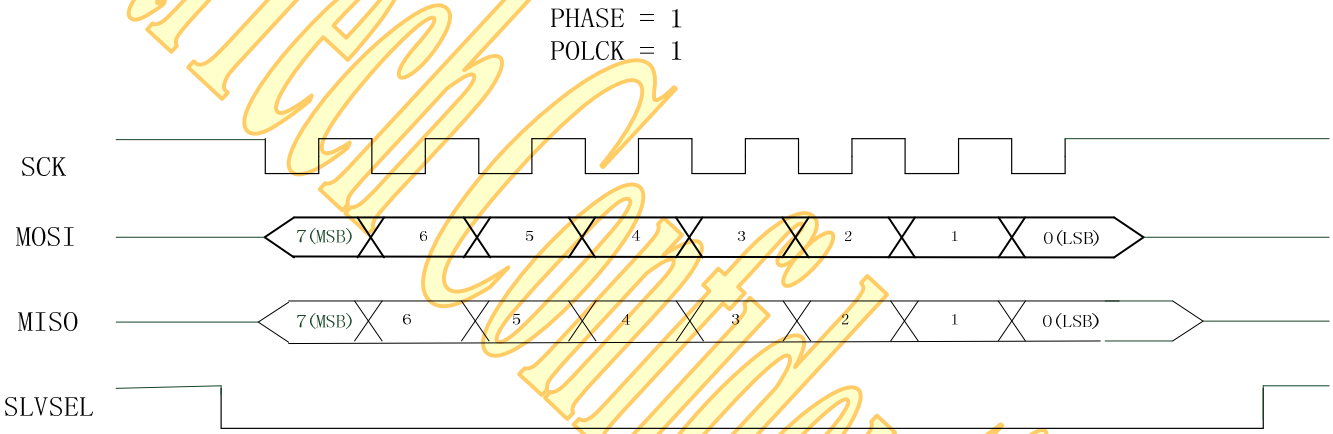


Figure 4-7 SPI data transfer format (Phase=1, POLCK=1)

SPI can be configured into either Master or Slave mode via the MAS bit of the SPI0CON register. When in the Master mode, the SPI needs to supply the data clock, whose frequency relationship with the Master clock (27MHz) can be set by CLKDVD bits of the SPI0CON register. When it is configured in the Slave mode, the clock, SCK, is supplied by the external Master. The maximum data clock frequency must not be higher than $\frac{F_{clk\_per}}{8}$.

4.6.2. I2C

FT5302 I2C is always configured in the Slave mode. The data transfer format is shown in Figure 4-8.

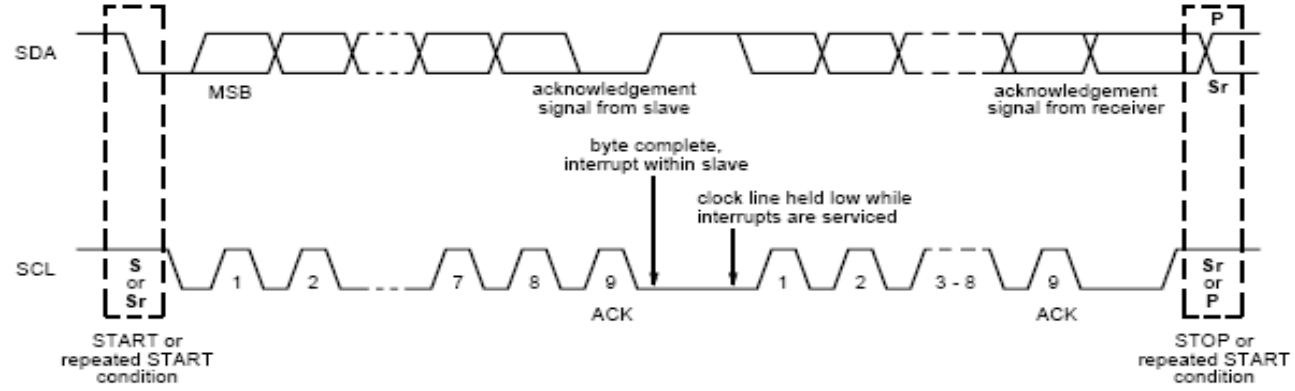


Figure 4-8 I2C serial data transfer format

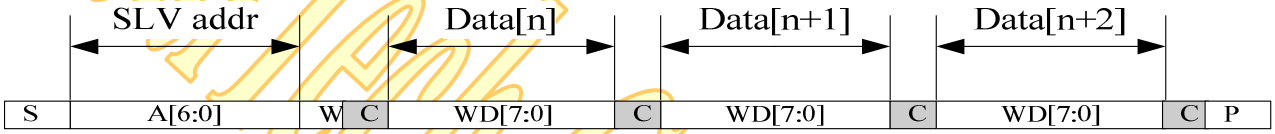


Figure 4-9 I2C master write, slave read

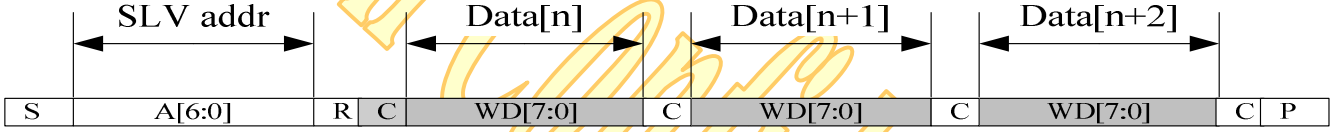


Figure 4-10 I2C master read, slave write

Table 4-1 lists the meanings of the mnemonics used in the above figures.

Table 4-1 Mnemonics description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b1: Read
C	ACK

P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

4.7. Serial Interface Timing

4.7.1. SPI Interface Timing Characteristics

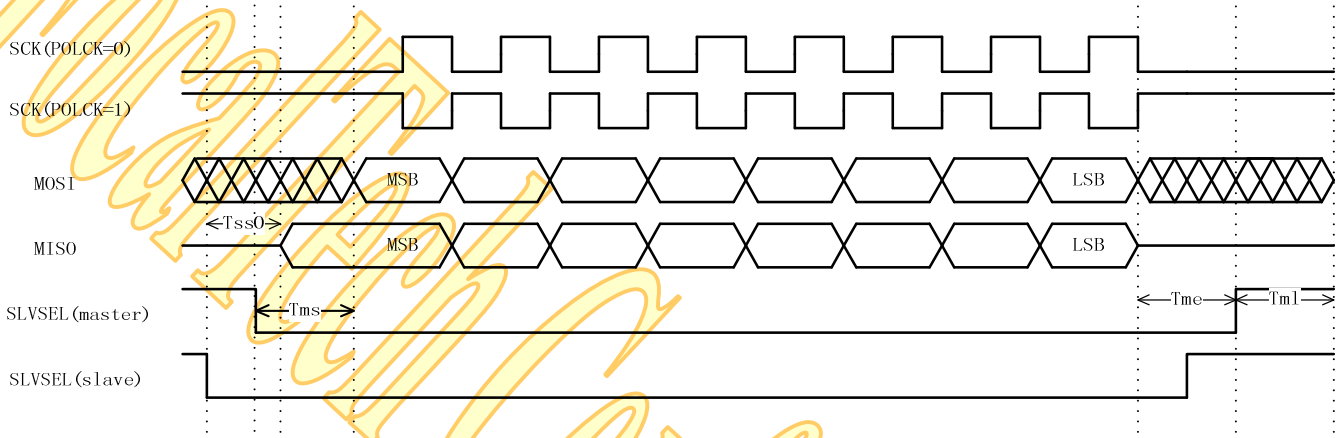


Figure 4-11 SPI Timing PHASE = 0

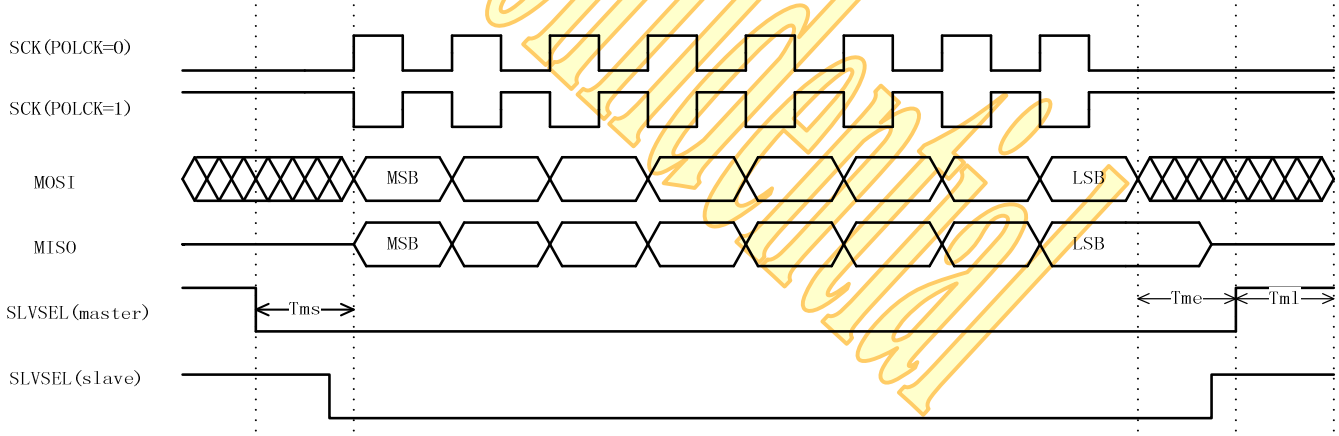


Figure 4-12 SPI Timing PHASE = 1

Tms: The time between the first cycle of SCK and the beginning of the valid SLVSEL in the master mode

Tme: The time between the end of last cycle of SCK and the beginning of invalid SLVSEL in the master mode

Tml: The minimum trailing time of the invalid SLVSEL in the master mode

Tss: The time between the beginning of the valid SLVSEL and the first bit valid output data in the slave mode and when phase = 0

Table 4-5 SPI Timing characteristics

Symbol	Unit	Value
Tms	cycle of SCK	1
Tme	cycle of SCK	1
Tml	cycle of SCK	1
Tss0	cycle of SPI internal clock	4

4.7.2. UART Interface Timing Characteristics

UART has two wires, txd and rxd, connected to external devices. It adopts asynchronous transmission mechanism, therefore, the phase between data and clock is not an issue after the baud rate is configured on both sides.

4.7.3. I2C Interface Timing Characteristics

parameter	Unit	MIN	MAX
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

5. Electrical Specifications

5.1. Absolute Maximum Ratings

Table 4-2 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC -– VSSD	V	-0.3 ~ +3.6	1, 2
Power Supply Voltage 2	VDDA1 - VSSA1	V	-0.3 ~ +3.6	1, 3
Power Supply Voltage 3	VDDA2 -– VSSD	V	-0.3 ~ +3.6	1, 4
Power Supply Voltage 8	VPP	V	-0.3 ~ +8	1
Input Voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1
Operating Temperature	Topr	℃	-40 ~ +85	1, 5
Storage Temperature	Tstg	℃	-55 ~ +110	1

Notes:

1. If used beyond the absolute maximum ratings, FT5302 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure IOVCC(high)≥VSSD (low)
3. Make sure VDDA1(high)≥VSSA1 (low)
4. Make sure VDDA2(high)≥VSSA2 (low)
5. The DC/AC characteristics of die and wafer products are guaranteed at 85℃

5.2. DC Characteristics

Table 4-3 DC Characteristics (VDDA1=VDDA2=2.6~3.3V, IOVCC=1.65~3.3V, Ta=-40~85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V	IOVCC=1.65V ~ 3.3V	0.8 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V	IOVCC=1.65V ~ 3.3V	-0.3	--	0.2 x IOVCC	
Output high -level voltage	VOH	V	IOVCC=1.65V ~ 3.3V IOH=-0.1mA	0.8 x IOVCC	--	--	

Output low -level voltage	VOL	V	IOVCC=1.65V ~ 3.3V IOH=0.1mA	--	--	0.2 x IOVCC	
I/O leakage current	ILI	μA	Vin=0~IOVCC	-1	--	1	
Current consumption (IOVCC – VSSD) + (VDDA1 – VSSA1) + (VDDA2 – VSSD) Normal operation mode	Iopr	mA	IOVCC=VDDA1=VDDA2 = 2.8V Ta=25℃	--	7	8	
Current consumption (IOVCC – VSSD) + (VDDA1 – VSSA1) + (VDDA2 – VSSD) Monitor mode	Imon	mA	IOVCC=VDDA1=VDDA2 = 2.8V Ta=25℃	--	3	--	
Current consumption (IOVCC – VSSD) + (VDDA1 – VSSA1) + (VDDA2 – VSSD) Sleep mode	Islp	mA	IOVCC=VDDA1=VDDA2 = 2.8V Ta=25℃	--	0.03	--	
Step-up output voltage	V8X	V	IOVCC=VDDA1=VDDA2 = 2.8V	18	20	--	
Input voltage	VDDA2	V		2.6	--	3.6	

5.3. AC Characteristics

Table 4-4 AC Characteristics of oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDDA2 = 2.8V 25℃	25	27	29	
OSC clock 2	fosc2	KHz	VDDA2 = 2.8V Ta=25℃	29	32	35	

Table 4-5 AC Characteristics of TX & RX

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
TX acceptable clock	ftx	KHz		100	150	270	
TX output rise time	Ttxr	nS		--	20	--	
TX output fall time	Ttxf	nS		--	20	--	
RX input voltage	Trxi	V		1.2	--	1.5	

Notes:

1. DC/AC electrical characteristics of bare die and wafer products are guaranteed at +85℃.

5.4. I/O Ports Circuits

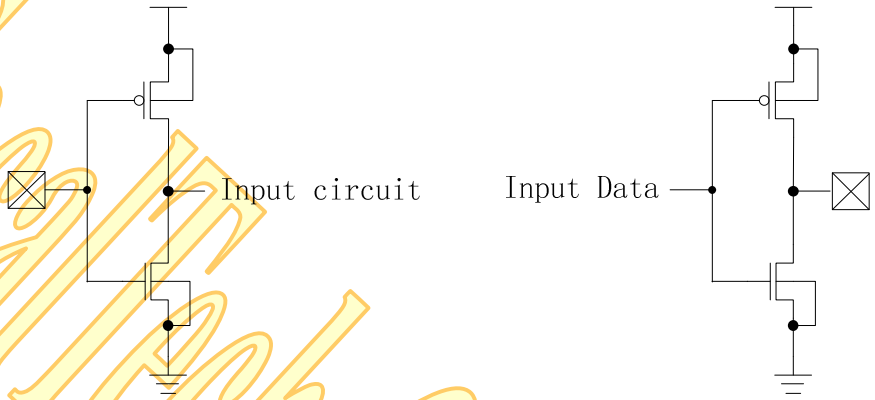


Figure 4-13 Input & Output port circuits

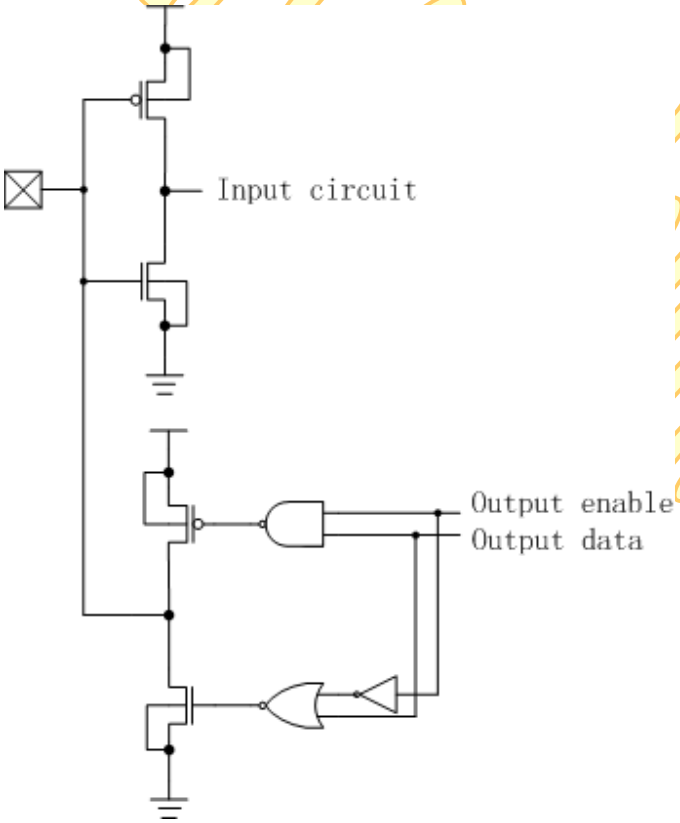


Figure 4-14 In/out port circuit

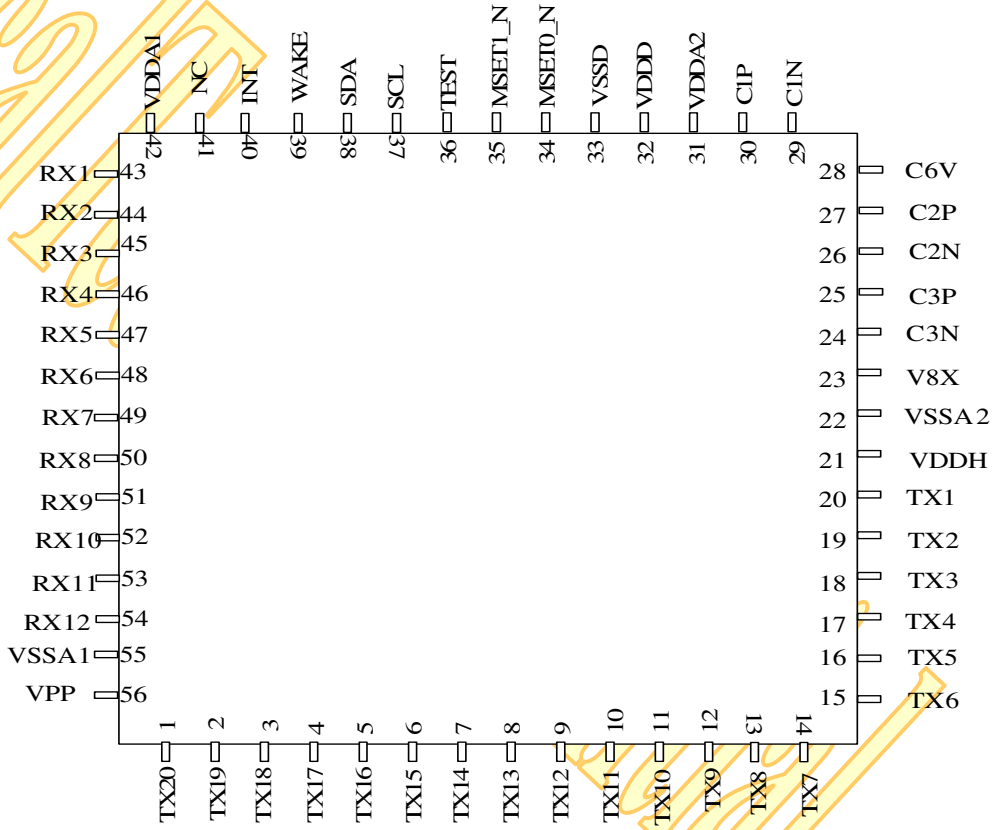
6. Pin Configurations

6.1. Pin List of FT5302

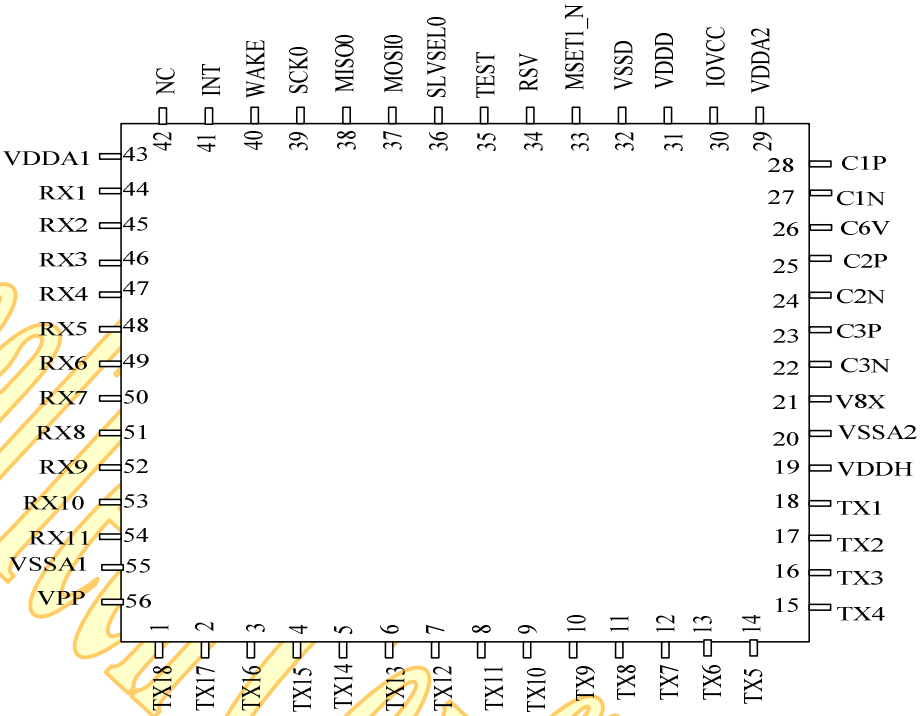
Name	Pin Number		Type	Description
	FE4	FE6		
TX20	1		O	Transmit output pin
TX19	2		O	Transmit output pin
TX18	3	1	O	Transmit output pin
TX17	4	2	O	Transmit output pin
TX16	5	3	O	Transmit output pin
TX15	6	4	O	Transmit output pin
TX14	7	5	O	Transmit output pin
TX13	8	6	O	Transmit output pin
TX12	9	7	O	Transmit output pin
TX11	10	8	O	Transmit output pin
TX10	11	9	O	Transmit output pin
TX9	12	10	O	Transmit output pin
TX8	13	11	O	Transmit output pin
TX7	14	12	O	Transmit output pin
TX6	15	13	O	Transmit output pin
TX5	16	14	O	Transmit output pin
TX4	17	15	O	Transmit output pin
TX3	18	16	O	Transmit output pin
TX2	19	17	O	Transmit output pin
TX1	20	18	O	Transmit output pin
VDDH	21	19	PWR	High voltage power supply (12 – 18V) from the charge pump LDO
VSSA2	22	20	GND	Analog ground
V8X	23	21	I/O	Charge pump output at 8 times of the input voltage. A 1μF ceramic capacitor to ground is required.
C3N	24	22	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C3P

C3P	25	23	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C3N
C2N	26	24	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C2P
C2P	27	25	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C2N
C6V	28	26	I/O	Charge pump output, needs an 1μF ceramic capacitor to ground
C1N	29	27	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C1P
C1P	30	28	I/O	Charge pump power boost for an external ceramic capacitor of 1μF connected to C1N
VDDA2	31	29	PWR	Analog power supply (2.8V)
IOVCC		30	PWR	I/O power supply
VDDD	32	31	PWR	Digital power supply (1.8V)
VSSD	33	32	GND	Digital ground
MSET0_N	34		I	Boot method select
MSET1_N	35	33	I	Boot method select
RSV		34	I	Reserved
TEST	36	35	I	Test mode enable
SLVSEL0/SCL	37	36	I	SPI slave select / I2C SCL
MOSI0/SDA	38	37	I/O	SPI0 data iutput in master mode and data input in slave mode / I2C SDA
MISO0		38	O	SPI data output
SCK0		39	I	SPI clock input
AWAKE	39	40	I	External interrupt from the host
INT	40	41	O	External interrupt to the host
NC	41	42	I/O	Not connected
VDDA1	42	43	PWR	Analog power supply
RX1	43	44	I	Receiver input pins
RX2	44	45	I	Receiver input pins
RX3	45	46	I	Receiver input pins
RX4	46	47	I	Receiver input pins
RX5	47	48	I	Receiver input pins
RX6	48	49	I	Receiver input pins
RX7	49	50	I	Receiver input pins

RX8	50	51	I	Receiver input pins
RX9	51	52	I	Receiver input pins
RX10	52	53	I	Receiver input pins
RX11	53	54	I	Receiver input pins
RX12	54		I	Receiver input pins
VSSA1	55	55	GND	Analog ground
VPP	56	56	PWR	OTP Program power supply



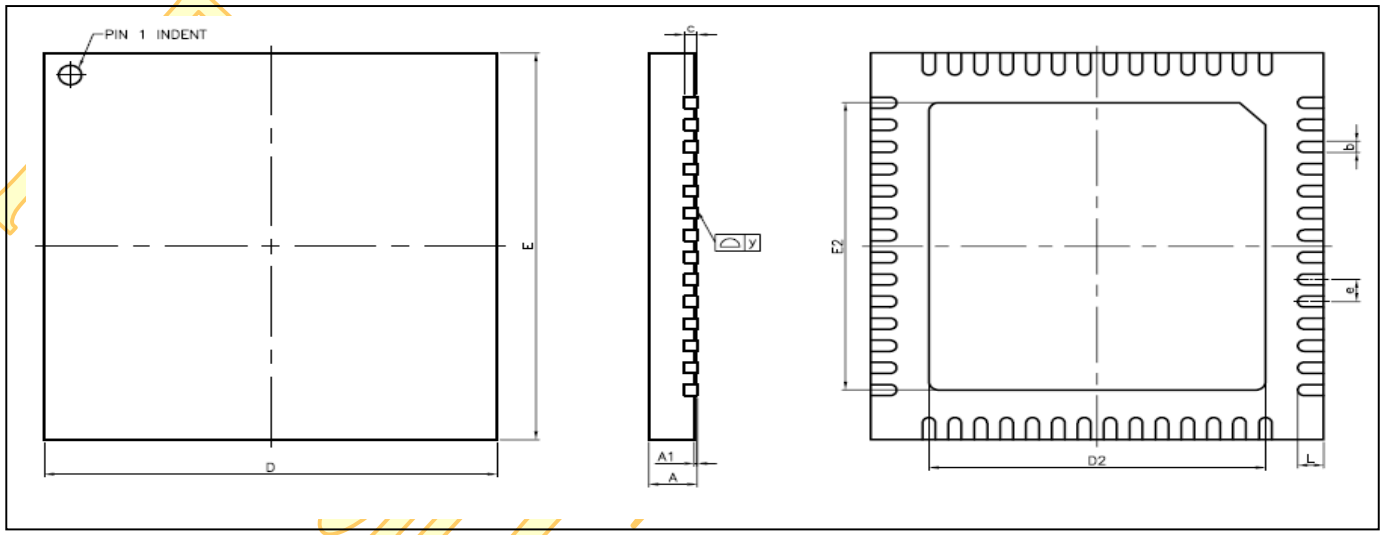
FT5302FE4 package diagram



FT5302FE6 package diagram

7. Package information

7.1. Package information of QFN-56 package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	---	0.20 REF	---
D	6.90	7.00	7.10
D2	5.15	5.20	5.25
E	6.90	7.00	7.10
E2	5.15	5.20	5.25
e	---	0.40	---
L	0.35	0.40	0.45
y	0.00	---	0.075

7.2. Order Information

Package Type	**QFN**
	56 Pin (7 * 7)
	D0.75 - 0.4
Product Name	**FT5302FEx**

Note:

1). The last two letters in the product name indicate the package type and lead pitch and thickness.

2). The second last letter indicates the package type.

F : QFN-7*7

3). The last letter indicates the lead pitch and thickness.

E : 0.8 – D0.4

T : Track Code
G : "G" for Green process.
Y : Year Code
WW : Week Code
SV : Lot Code

Product Name	Package Type	# TX Pins	# RX Pins
FT5302FE4	QFN-56	20	12
FT5302FE6	QFN-56	18	11

REVISION TABLE

version	Revisions	Date
1.0	First draft	2010-03-31

END OF DATABOOK