Product Data Sheet

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FT5502

Capacitive Touch Panel Controller

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Index

1. Description

FT5502 series ICs are single chip capacitive touch panel controller ICs with a built-in 8 bit Micro-controller unit (MCU). It adopts the mutual capacitance approach, which supports true multi-touch capabilities. In conjunction with a mutual capacitive touch panel, FT5502 facilitates user friendly input functions, which can be used for portable devices, such as cellular phones, digital cameras, and notebook personal computers.

2. Typical Applications

FT5502 accommodates a wide range of applications from with a set of buttons up to a 2D touch sensing device.

- Touch pad
- Portable MP3 and MP4 media players
- Navigation systems, GPS
- Digital cameras
- Game consoles
- Car applications
- POS (Point of Sales) devices
- Writing pad
- DV
- Mouse
- LCD monitor
- Smart Remote Controller

3. Features

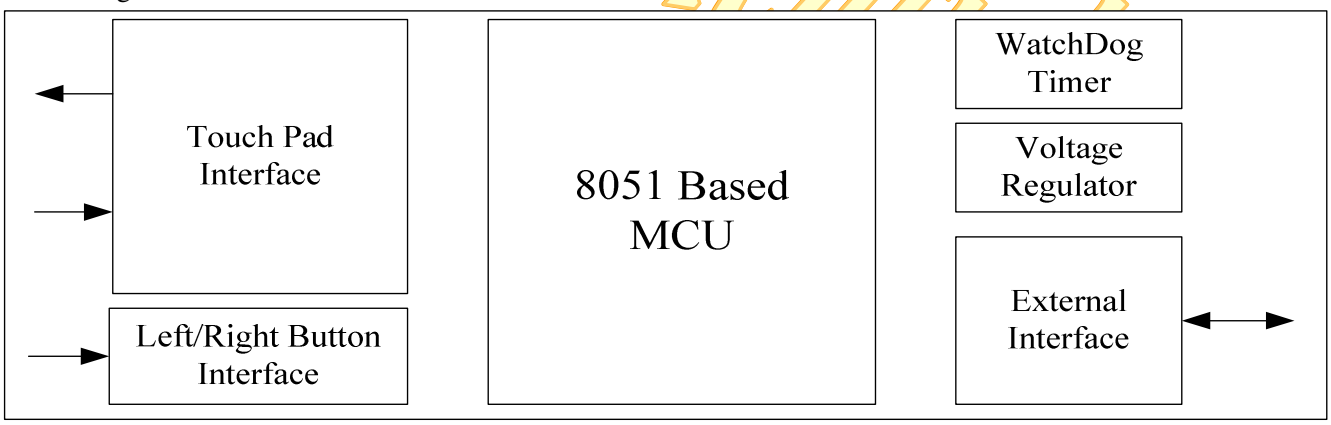
- Low cost solution
- Mutual capacitive sensing techniques
- True multi-touch with up to 5 points of absolution X and Y coordinates
- Auto calibration: Insensitive to capacitance and environmental variations

- Supporting up to 15 transmit lines and 10 receive lines
- Supporting up to 3.8" touch screen
- Fully programmable scan sequences with individually adjustable receive lines and transmit lines to support various of applications
- Scan rate larger than 80Hz
- Touch resolution of 100 dots per inch (dpi) or higher -- depending on the panel size
- Standard PS/2 interface. Provide full PS/2 mode support
  Include: Stream mode, Remote mode
- I2C interfaces
- Operating voltage: 2.8V ~ 3.6V
- Capable of driving single channel (transmit/receive) resistance: ~ 15K Ω
- Capable of supporting single channel (transmit/receive) capacitance: 50 pF
- The optimal sensing mutual capacitor: 1pF~2pF
- Built-in MCU
- Operating temperature range: -40°C ~ +85°C

4. Functional Description

4.1. Architectural Overview

Figure 4-1 shows the overall architecture for FT5502.



FT5502 can be divided into the following functional groups:

- Touch panel interface circuits

  The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So, it supports both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces, which will be explained in detail in a later section.

- Left/Right Button Interface
- 8051 based MCU

  8051 compatible MCU

  Communication protocol software is implemented on this MCU to exchange data and control information with the host processor

  On chip OTP: a One Time Programmable (OTP) is implemented to store programs and some key parameters

- External Interface

  PS/2: an interface for data exchange with host

  I2C: an interface for data exchange with host

  INT: an interrupt signal to inform the host processor that touch data is ready for read. It is only available in the I2C mode

  WAKE: an interrupt signal for the host to change F5502 from Hibernate to Active mode. It is only available in the I2C mode

- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input 3.3V supply

4.2. MCU

This section describes some critical features and operations supported by the 8051 compatible MCU. Figure 4-2 shows the overall structure of the MCU block. In addition to the 8051 compatible MCU core, we have added the following circuits:

Real time clock (RTC): A 32KHz RC oscillator

Timer: A number of timers are available to generate different clocks

Clock Manager: To control various clocks under different operation conditions of the system

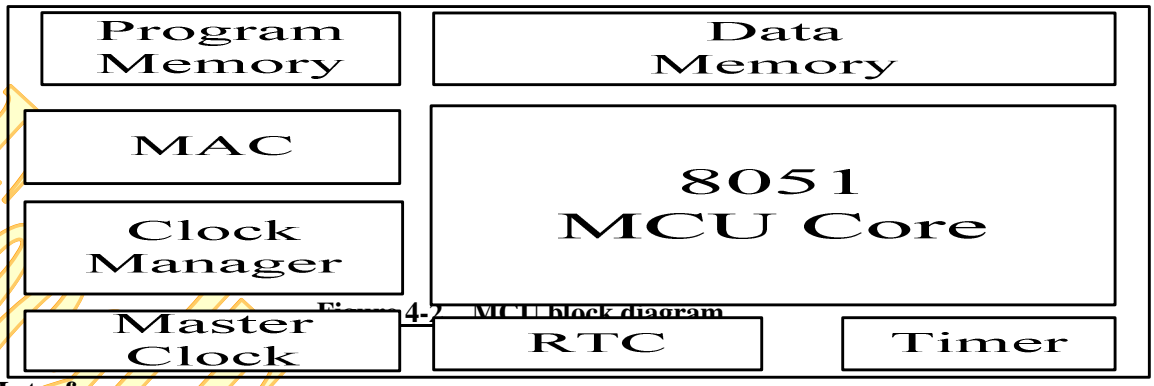


Figure 4-2 MCU block diagram

4.3. Host Interface

Table 4-3 shows the PS/2 interface between the host processor and FT5502. This interface consists of the following three sets of signals:

- PS/2_CLK
- PS/2_DATA

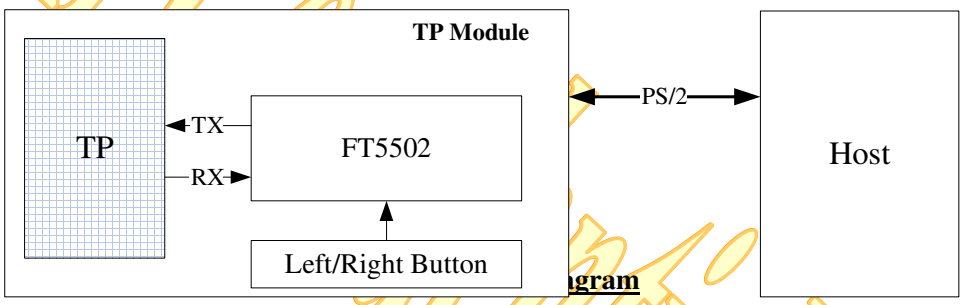


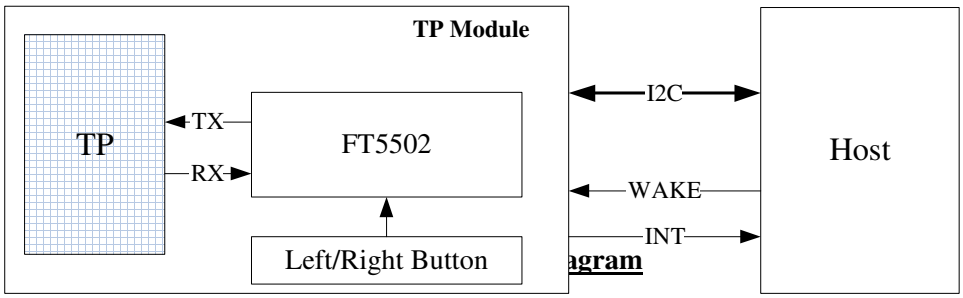
Figure 4-3 I2C to Host interface diagram

The details of this interface are described in detail in Section 4.4.

Figure 4-4 I2C to Host interface diagram

It shows the interface between a host processor and FT5502. The interface for other FT5502 series chips is identical. This interface consists of the following three sets of signals:

- Serial interface
- Interrupt from FT5502 to the host
- Wake up signal from the host to FT5502



agram

The details of this interface are described in detail in Section 4.4. The interrupt signal, /INT, is used for FT5502 to inform that host that data are ready for the host to receive. The /WAKE signal is used for the host to wake up FT5502 from the Hibernate mode. Upon exiting the Hibernate mode, FT5502 shall enter the Active mode.

4.4. Serial Interface

PS/2 interface:

FT5502 supports the PS/2 interface, which can be used by a host processor or other devices. Refer to IBM PS2 specification. All of the command specified by IBM are implemented. The data transfer format is shown in Figure 4-.

Device-to-Host Communication

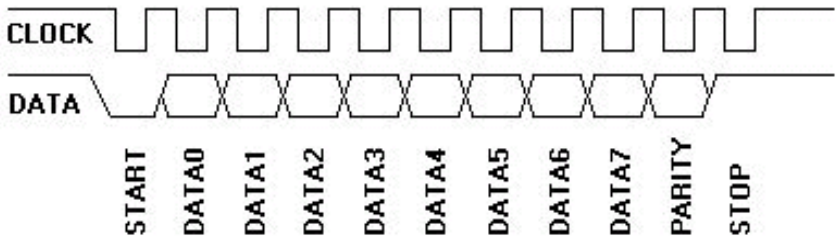


Figure 4-5 Device -to- Host Communication

Host -to- Device Communication

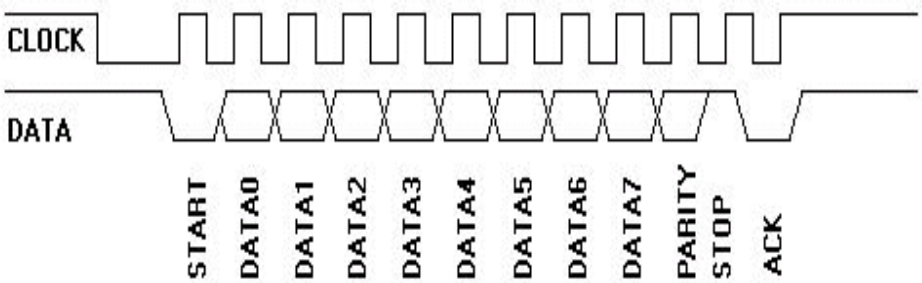


Figure 4-6 Host-to-Device Communication

Movement data packet:

The standard PS/2 mouse sends movement(and button) information to the host using the following 3-byte packet

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	Y overflow	X overflow	Y sign bit	X sign bit	Always 1	Middle Btn	Right Btn	Left Btn
Byte 2	X Movement							
Byte 3	Y Movement							

Figure 4-7 Standard 3-byte packet

Intellimouse Extensions:

Extend to support 4-byte movement data packet.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	Y overflow	X overflow	Y sign bit	X sign bit	Always 1	Middle Btn	Right Btn	Left Btn
Byte 2	X Movement							
Byte 3	Y Movement							
Byte 4	Z Movement							

Figure 4-8 Intellimouse Extensions 4-byte packet

Table 4-1 PS/2 Specifications

parameter	Unit	Min	Typ	Max
PS2_CLK Frequency	KHz	10	12.5	30
Sample Rate in stream mode	Hz		60	80

I2C interfaces:

FT5502 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 4-.

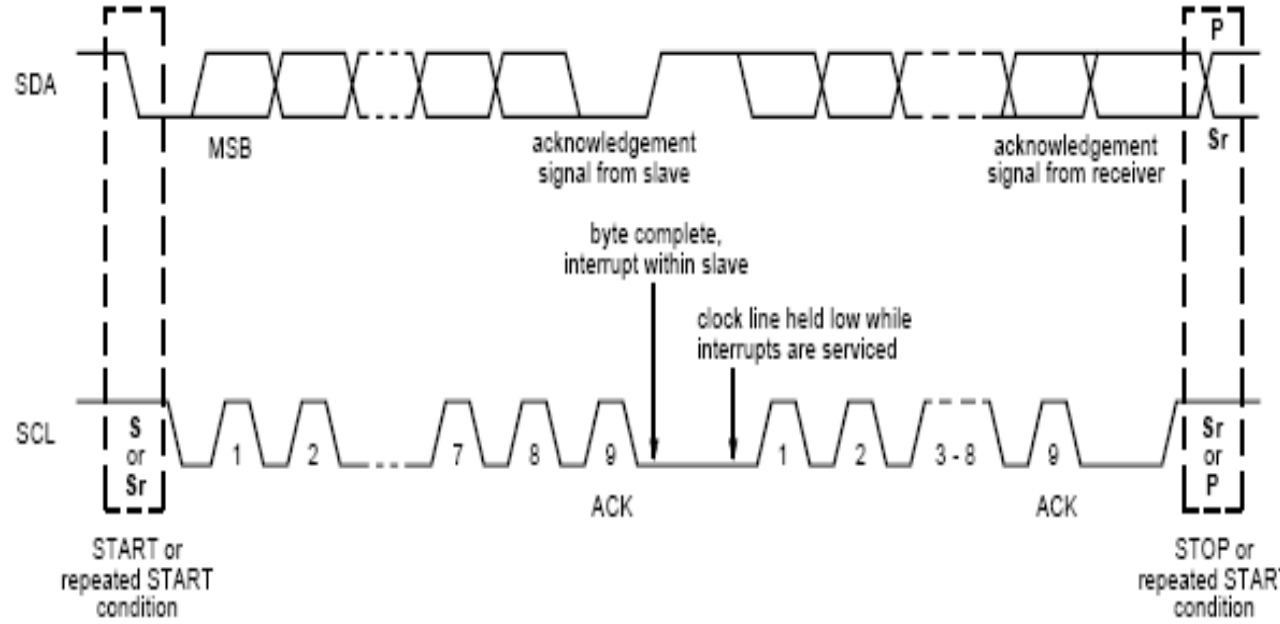


Figure 4-9 I2C serial data transfer format

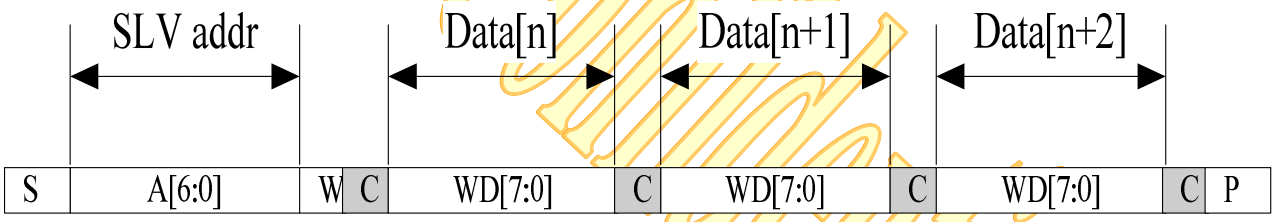


Figure 4-10 I2C master write, slave read

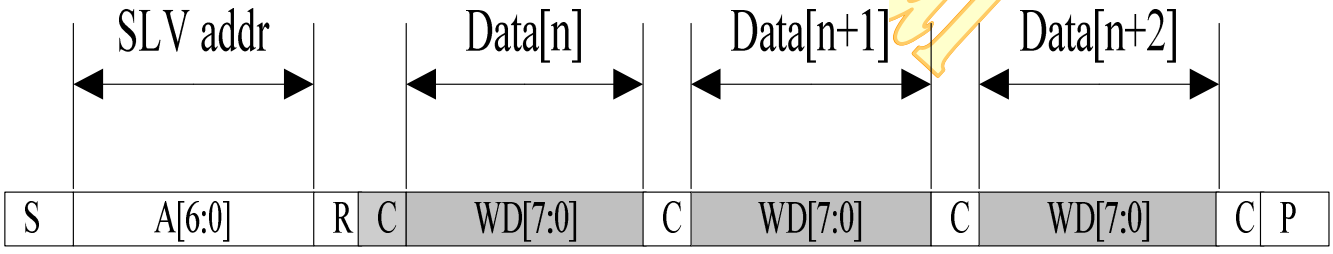


Figure 4-11 I2C master read, slave write

Table 4- lists the meanings of the mnemonics used in the above figures.

Table 4-2 Mnemonics description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b1: Read
C	ACK
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics

parameter	Unit	MIN	MUX
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

5. Electrical Specifications

5.1. Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDDA1 - VSSA1	V	-0.3 ~ +3.6	1, 2
Power Supply Voltage 2	VDDA2 – VSSA2	V	-0.3 ~ +3.6	1, 3

Power Supply Voltage 3	VPP	V	-0.3 ~ +8	1
Input Voltage	Vt	V	-0.3 ~VDDA + 0.3	1
Operating Temperature	Topr	℃	-40 ~ +85	1, 4
Storage Temperature	Tstg	℃	-55 ~ +110	1

Notes:

1. If used beyond the absolute maximum ratings, FT5502 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDDA1(high)≥VSSA1 (low)
3. Make sure VDDA2(high)≥VSSA2 (low)
4. The DC/AC characteristics of die and wafer products are guaranteed at 85℃

5.2. DC Characteristics

Table 5-2 DC Characteristics (VDDA=VDDA1=VDDA2=2.6~3.3V, Ta=-40~85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.8 x VDDA	--	VDDA	
Input low -level voltage	VIL	V		-0.3	--	0.2 x VDDA	
Output high -level voltage	VOH	V	IOH=-0.1mA	0.8 x VDDA	--	--	
Output low -level voltage	VOL	V	IOH=0.1mA	--	--	0.2 x VDDA	
I/O leakage current	ILI	μA	Vin=0~VDDA	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDDA1=VDDA2 = 2.8V Ta=25℃	--	3	4.5	
Current consumption （Monitor mode）	Imon	mA	VDDA1=VDDA2 = 2.8V Ta=25℃	--	2.4	--	
Current consumption （Sleep mode）	Islp	mA	VDDA1=VDDA2 = 2.8V Ta=25℃	--	0.03	--	
Step-up output voltage	V8X	V	VDDA1=VDDA2 = 2.8V	18	20	--	
Input voltage	VDDA2	V		2.8	--	3.6	

5.3. AC Characteristics

Table 5-3 AC Characteristics of oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDDA2 = 2.8V 25℃	25	27	29	
OSC clock 2	fosc2	KHz	VDDA2 = 2.8V Ta=25℃	29	32	35	

Table 5-4 AC Characteristics of TX & RX

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
TX acceptable clock	ftx	KHz		100	150	270	
TX output rise time	Ttxr	nS		--	20	--	
TX output fall time	Ttxf	nS		--	20	--	
RX input voltage	Trxi	V		1.2	--	1.5	

Notes:

DC/AC electrical characteristics of bare die and wafer products are guaranteed at +85℃.

5.4. I/O Ports Circuits

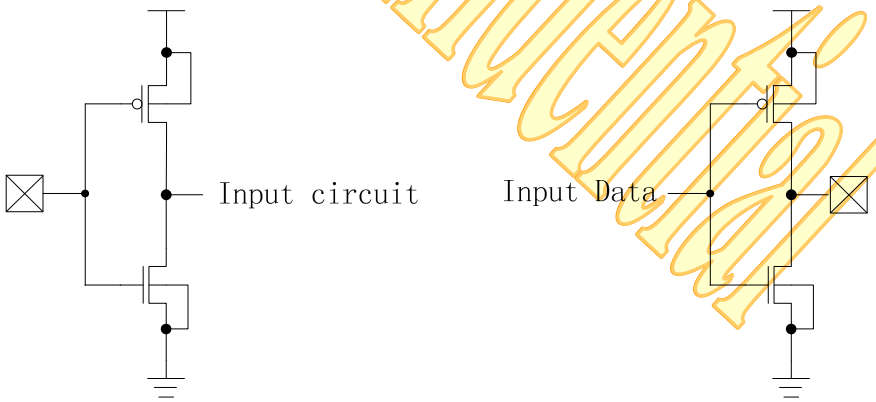


Figure 5-1 Input & Output port circuits

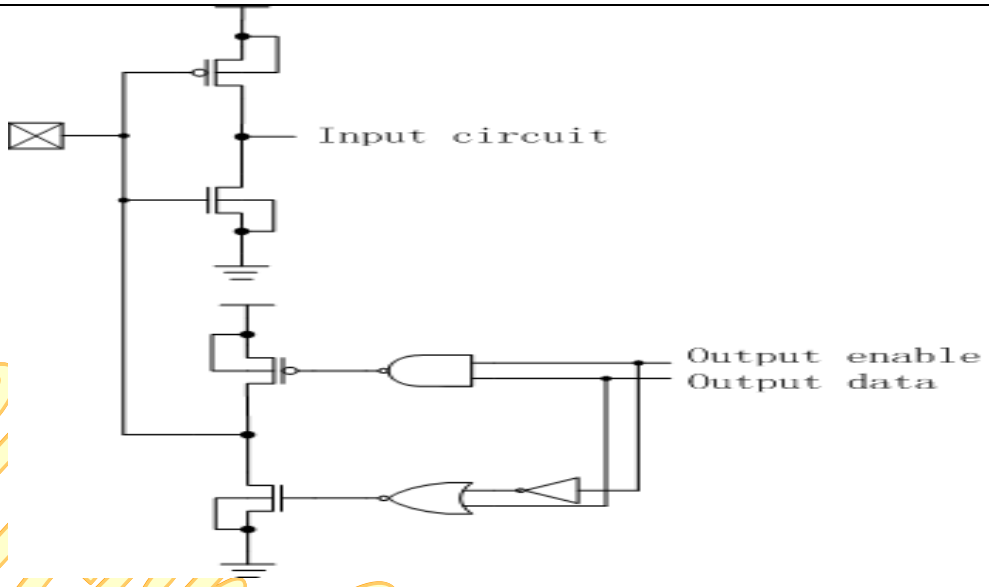


Figure 5-2 In/out port circuit

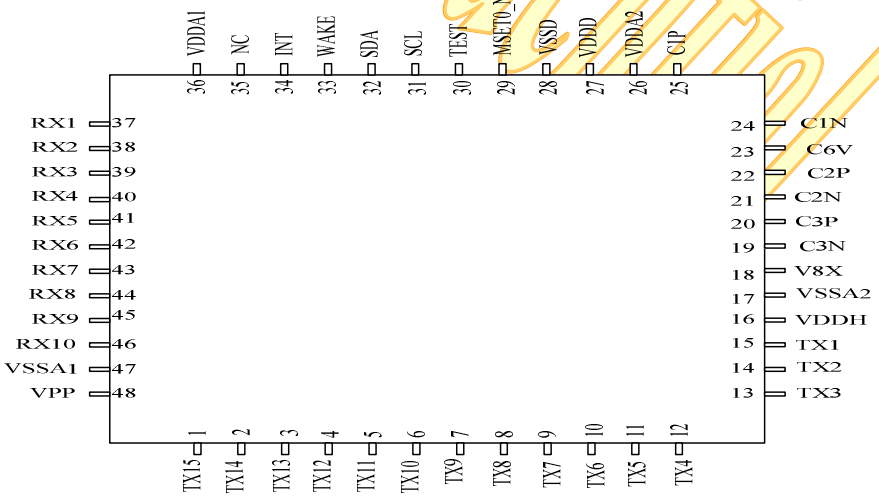
6. Pin Configurations

6.1. Pin List of FT5502 (QFN48L-6x6)

Name	Pin Number	Type	Description
	DE1		
TX15	1	O	Transmit output pin
TX14	2	O	Transmit output pin
TX13	3	O	Transmit output pin
TX12	4	O	Transmit output pin
TX11	5	O	Transmit output pin
TX10	6	O	Transmit output pin
TX9	7	O	Transmit output pin
TX8	8	O	Transmit output pin
TX7	9	O	Transmit output pin
TX6	10	O	Transmit output pin
TX5	11	O	Transmit output pin
TX4	12	O	Transmit output pin
TX3	13	O	Transmit output pin
TX2	14	O	Transmit output pin

TX1	15	O	Transmit output pin
VDDH	16	PWR	High voltage power supply (12 – 18V) from the charge pump LDO，generated internal. A 1 μ F ceramic to ground is required.
VSSA2	17	GND	Analog ground
V8X	18	I/O	Charge pump output at 8 times of the input voltage. A 1 μ F ceramic capacitor to ground is required.
C3N	19	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C3P
C3P	20	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C3N
C2N	21	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C2P
C2P	22	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C2N
C6V	23	I/O	Charge pump output at twice of the input voltage. A 1 μ F ceramic capacitor to ground is required.
C1N	24	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C1P
C1P	25	I/O	Charge pump power boost for an external ceramic capacitor of 1 μ F connected to C1N
VDDA2	26	PWR	Analog power supply
VDDD	27	PWR	Digital power supply, generated internal. A 1 μ F ceramic capacitor to ground is required.
VSSD	28	GND	Digital ground
MSET0_N	29	I	Boot select: 0: From I2C 1: From OTP
TEST	30	I	Test mode enabled at high and normal mode when low
SCL	31	I/O	I2C clock input
SDA	32	I/O	I2C data input and output
PS/2_DAT WAKE	33	I/O	PS/2 Data input and output External interrupt from the host

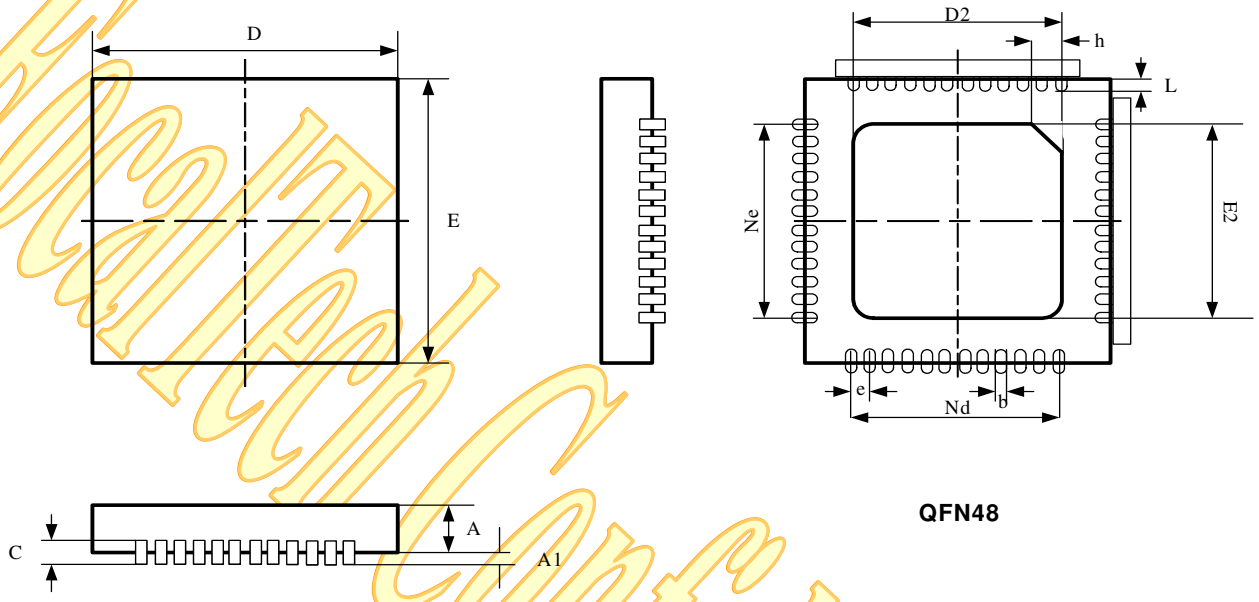
PS/2_CLK INT	34	I/O	PS/2 Clock input and output External interrupt to the host
NC	35	I/O	Not connected
VDDA1	36	PWR	Analog power supply
RX1	37	I	Receiver input pins
RX2	38	I	Receiver input pins
RX3	39	I	Receiver input pins
RX4	40	I	Receiver input pins
RX5	41	I	Receiver input pins
RX6	42	I	Receiver input pins
RX7	43	I	Receiver input pins
RX8	44	I	Receiver input pins
RX9	45	I	Receiver input pins
RX10	46	I	Receiver input pins
VSSA1	47	GND	Analog ground
VPP	48	PWR	OTP Program power supply, 7.5V when programming. VSS/VDD/Floating when not programming



FT5502DE1 Package Diagram

7. Package information

7.1. Package information of QFN-6x6-48L Package



QFN48

SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.70	0.75	0.80	Ne	4.40BSC		
A1	----	0.01	0.05	Nd	4.40BSC		
b	0.18	0.22	0.28	E	5.90	6.00	6.10
c	0.15	0.20	0.25	E2	4.10REF		
D	5.90	6.00	6.10	L	0.35	0.40	0.45
D2	4.10REF			h	0.30	0.35	0.40
e	0.40 BSC			L/F (MIL)	177*177		

7.2. Order Information

Package Type	QFN
	48 Pin (6 * 6)
	0.8 - P0.4
Product Name	FT5502DE1

Note:

1). The last two letters in the product name indicate the package type and lead pitch and thickness.

2). The second last letter indicates the package type.

D : QFN-6*6

3). The last letter indicates the lead pitch and thickness.

E : 0.8 - P0.4

T : Track Code

F : "F" for Lead Free process.

Y : Year Code

WW : Week Code

SV : Lot Code

Product Name	Package Type	# TX Pins	# RX Pins
FT5502DE1	QFN-48L	15	10

REVISION TABLE

Version	Revisions	Date
1.0	First draft	2010-03-26

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