FTP04N65
FTA04N65

N-Channel MOSFET

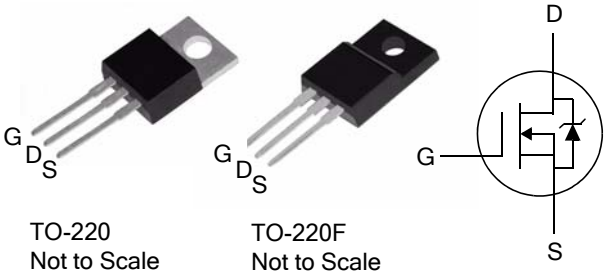
Applications:

- Adaptor
- Charger
- SMPS Standby Power
- LCD Panel Power

V_{DSS}	$R_{DS(ON)}$ (Max.)	I_D
650V	2.2 Ω	4.0A

Features:

- Lead Free
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves



TO-220
Not to Scale

TO-220F
Not to Scale

Ordering Information

PART NUMBER	PACKAGE	BRAND
FTP04N65	TO-220	FTP04N65
FTA04N65	TO-220F	FTA04N65

Absolute Maximum Ratings T_C=25 °C unless otherwise specified

Symbol	Parameter	FTP04N65	FTA04N65	Units
V_{DSS}	Drain-to-Source Voltage (NOTE *1)	650		V
I_D	Continuous Drain Current	4.0	4.0*	A
I_D@ 100 °C	Continuous Drain Current	Figure 3		
I_{DM}	Pulsed Drain Current, V_{GS}@ 10V (NOTE *2)	Figure 6		
P_D	Power Dissipation	100	24	W
	Derating Factor above 25 °C	0.80	0.19	W/ °C
V_{GS}	Gate-to-Source Voltage	± 30		V
E_{AS}	Single Pulse Avalanche Engergy L=3.0 mH, I_D=4.1 Amps	250		mJ
I_{AS}	Pulsed Avalanche Rating	Figure 8		
dv/dt	Peak Diode Recovery dv/dt (NOTE *3)	3.0		V/ns
T_L T_{PKG}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds Package Body for 10 seconds	300 260		°C
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150		

**Drain Current limited by Maximum Junction Temperature.*

***Caution:** Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.*

Thermal Resistance

Symbol	Parameter	FTP04N65	FTA04N65	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.25	5.2	°C/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150 °C.
$R_{\theta JA}$	Junction-to-Ambient	62	62		1 cubic foot chamber, free air.

OFF Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	V_{GS}=0V, I_D=250μA
$\Delta BV_{DSS}/\Delta T_J$	BreakdownVoltage Temperature Coefficient, Figure 11.	--	0.71	--	V/°C	Reference to 25°C, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V_{DS}=650V, V_{GS}=0V
		--	--	250		V_{DS}=520V, V_{GS}=0V T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{GS}=+30V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -30V

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance Figure 9 and 10.	--	1.8	2.2	Ω	V_{GS}=10V, I_D=2.4A (NOTE *4)
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250μA
gfs	Forward Transconductance	--	3.8	--	S	V_{DS}=15V, I_D=4.0A (NOTE *4)

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	660	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz Figure 14
C_{oss}	Output Capacitance	--	85	--		
C_{rss}	Reverse Transfer Capacitance	--	18	--		
Q_g	Total Gate Charge	--	23	--	nC	V_{DD}=325V I_D=4.0A V_{GS}=10V Figure 15
Q_{gs}	Gate-to-Source Charge	--	4.3	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	10.6	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	21	--	ns	V_{DD}=325V I_D=4.0A V_{GS}=10V R_G=12Ω
t_{rise}	Rise Time	--	21	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	44	--		
t_{fall}	Fall Time	--	40	--		

Source-Drain Diode Characteristics T_C=25 °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	4.0	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	16.0	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=4.0A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	250	380	ns	V_{GS}=0V
Q_{rr}	Reverse Recovery Charge	--	1.6	2.4	μC	I_F=4.0A, di/dt=100 A/μs

Notes:

*1. T_J = +25 °C to +150 °C.

*2. Repetitive rating; pulse width limited by maximum junction temperature.

*3. I_{SD}= 4.0A di/dt ≤ 100 A/μs, V_{DD} ≤ BV_{DSS}, T_J=+150 °C.

*4. Pulse width ≤ 380μs; duty cycle ≤ 2%.

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

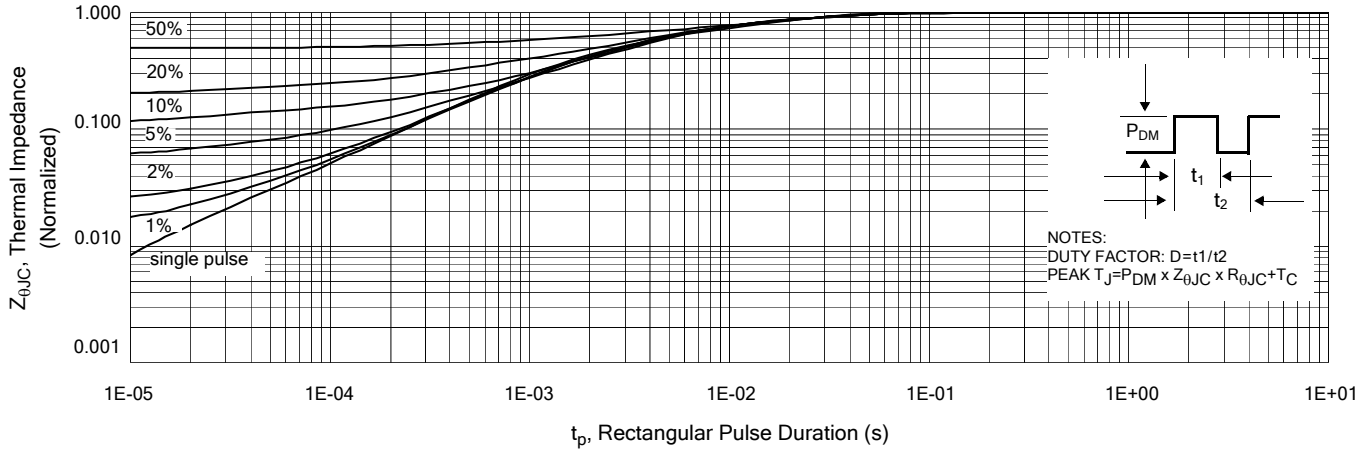


Figure 2. Maximum Power Dissipation vs Case Temperature

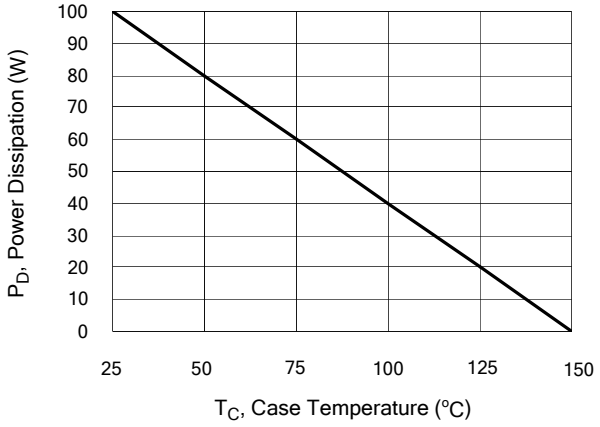


Figure3. Maximum Continuous Drain Current vs Case Temperature

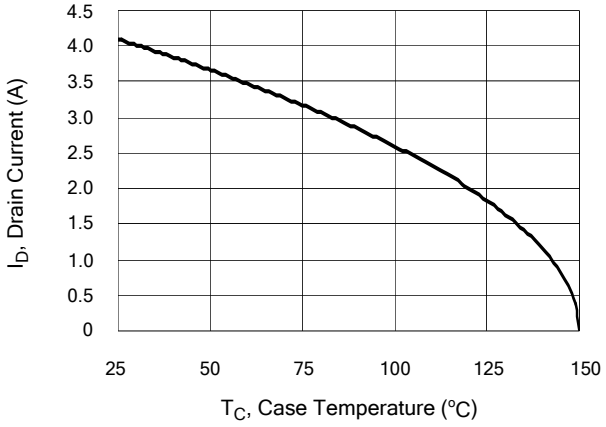


Figure 4. Typical Output Characteristics

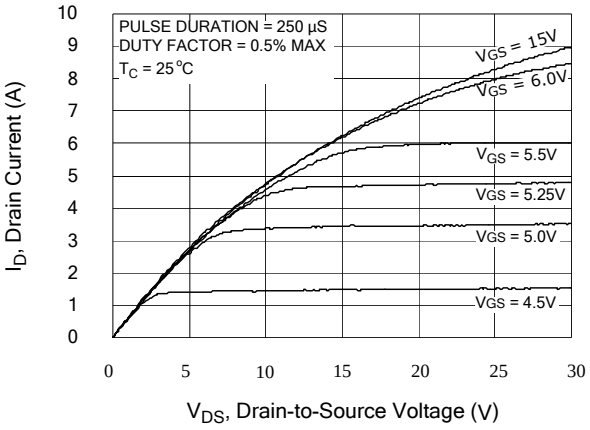


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

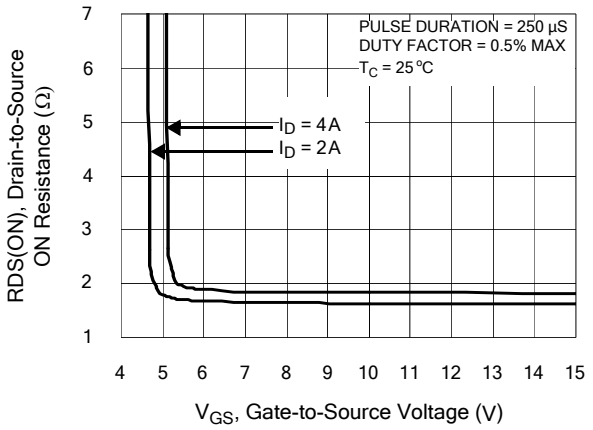


Figure 6. Maximum Peak Current Capability

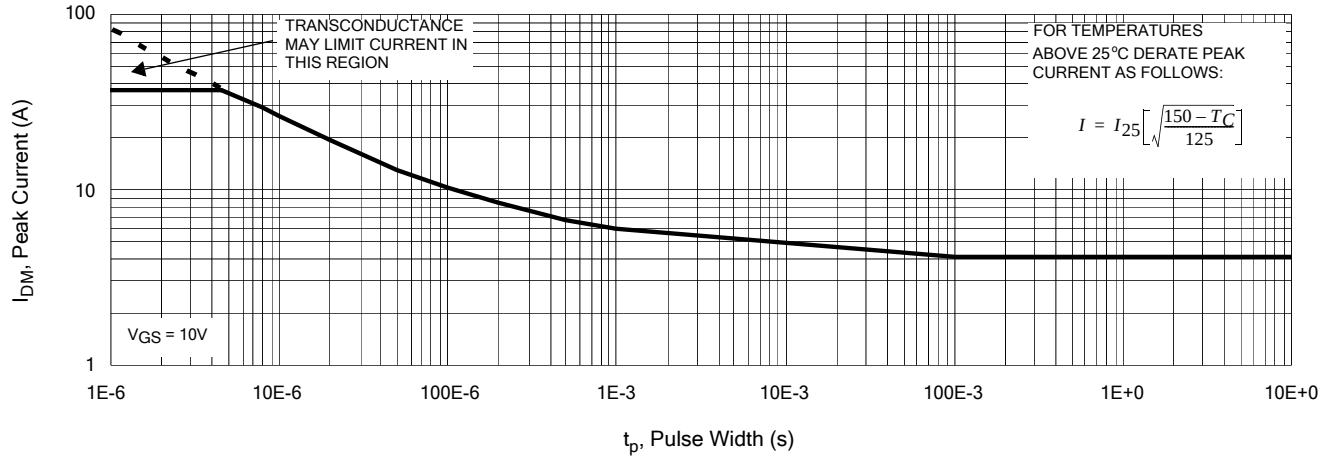


Figure 7. Typical Transfer Characteristics

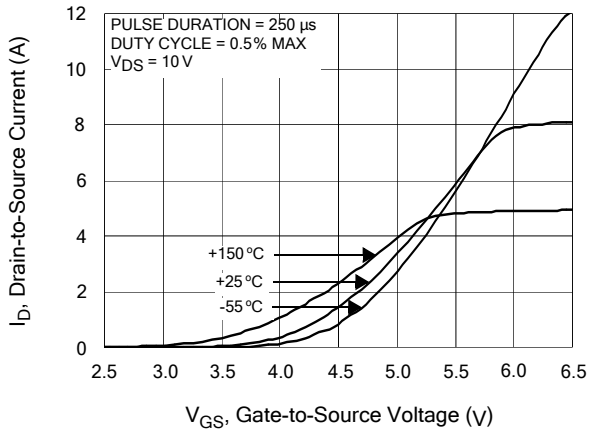


Figure8. Unclamped Inductive Switching Capability

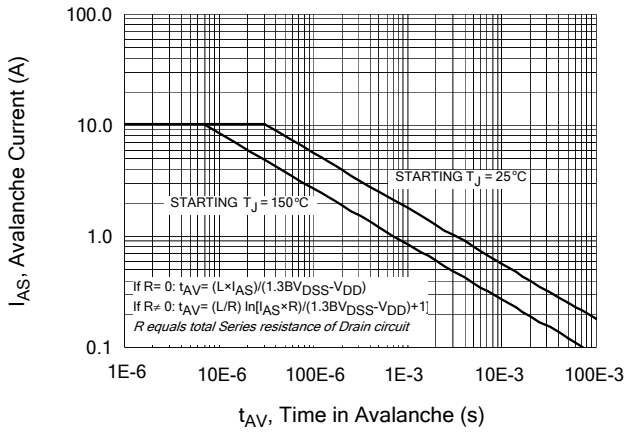


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

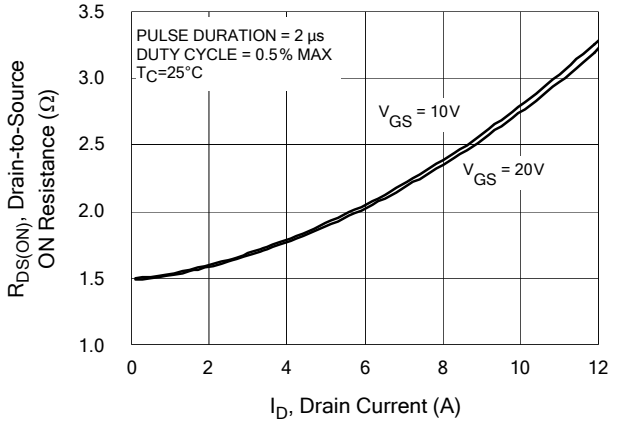


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

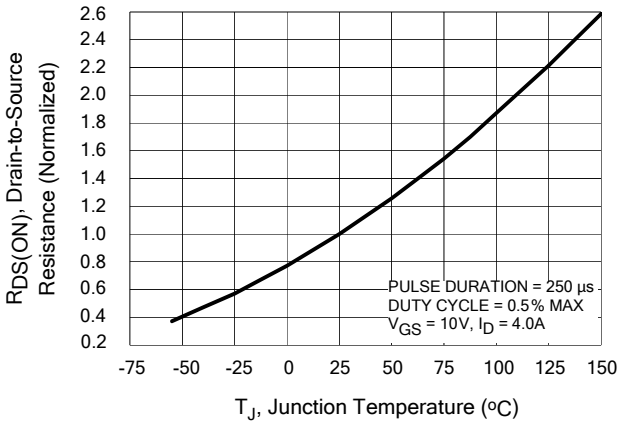


Figure 11. Typical Breakdown Voltage vs Junction Temperature

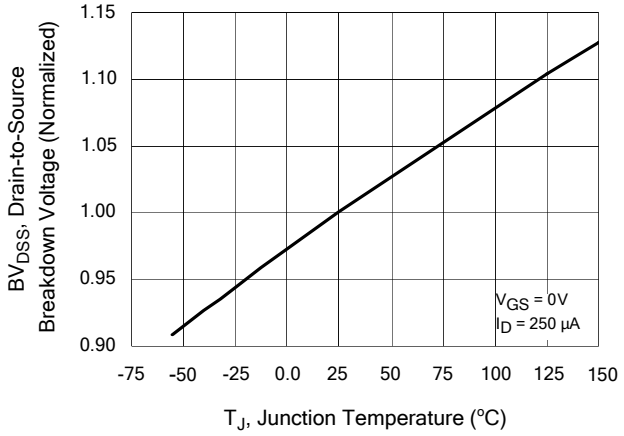


Figure 12. Typical Threshold Voltage vs Junction Temperature

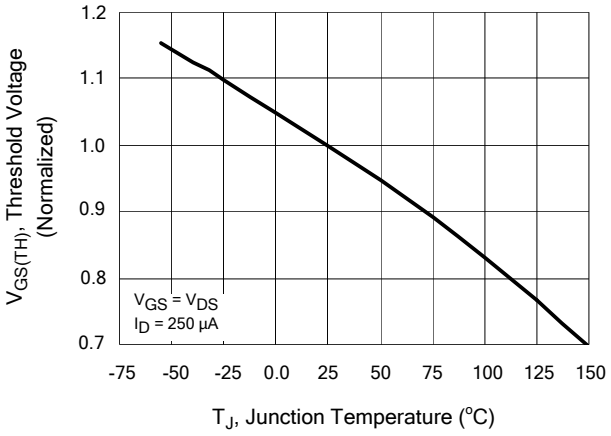


Figure 13. Maximum Forward Bias Safe Operating Area

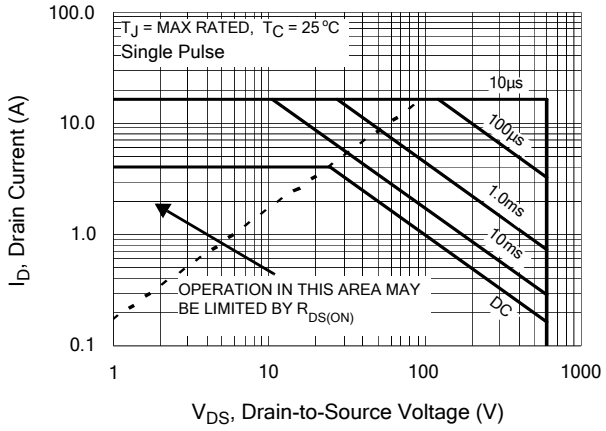


Figure 14. Typical Capacitance vs

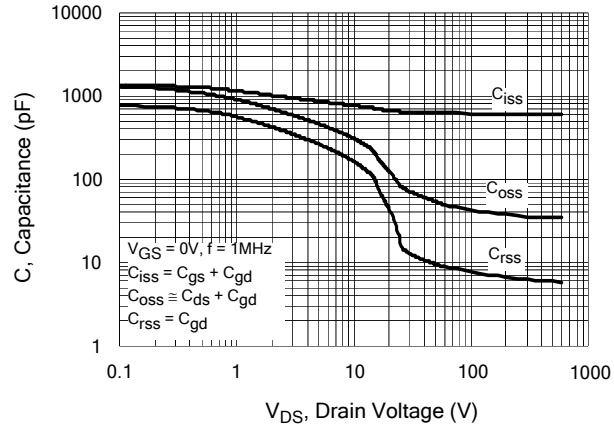


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

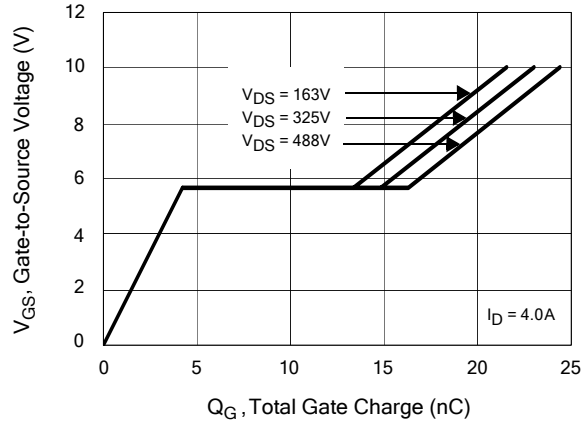
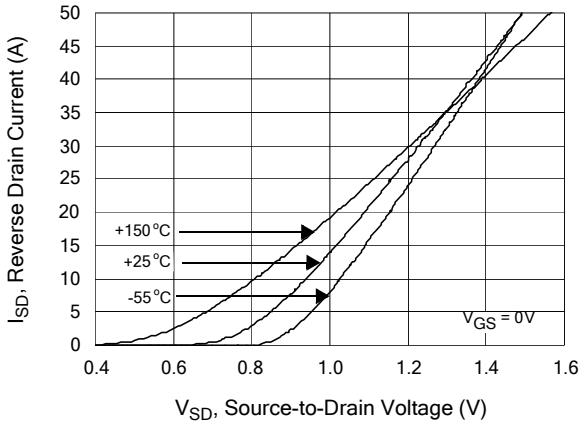


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

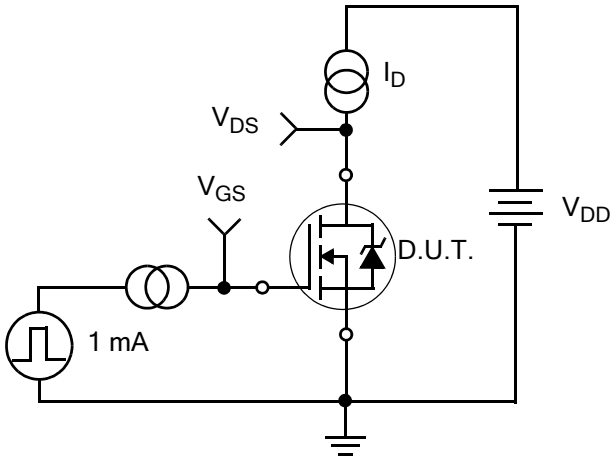


Figure 17. Gate Charge Test Circuit

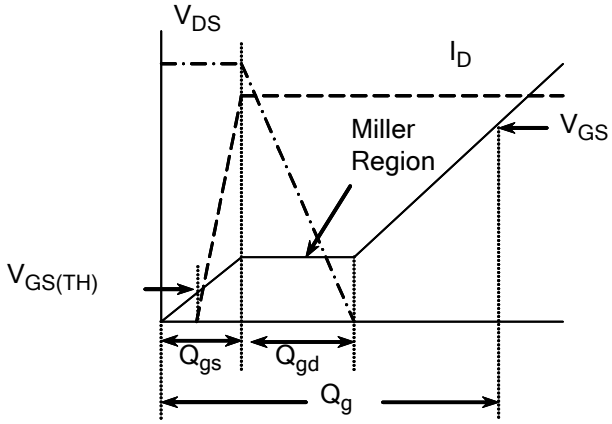


Figure 18. Gate Charge Waveform

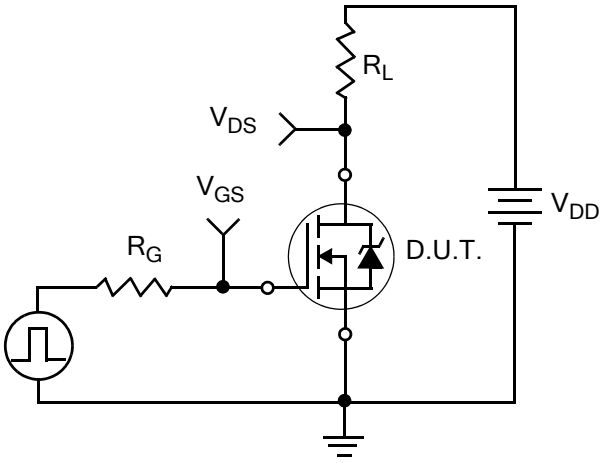


Figure 19. Resistive Switching Test Circuit

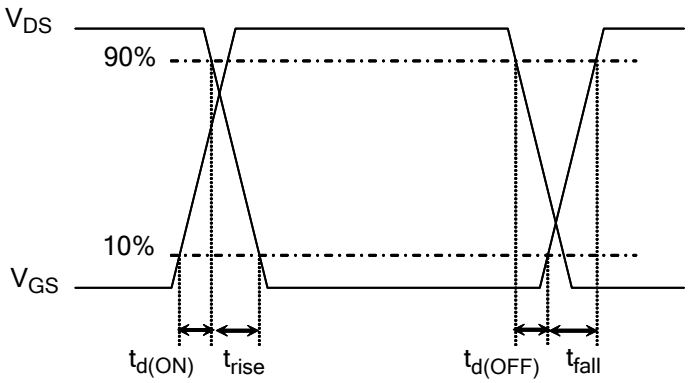


Figure 20. Resistive Switching Waveforms

Test Circuits and Waveforms

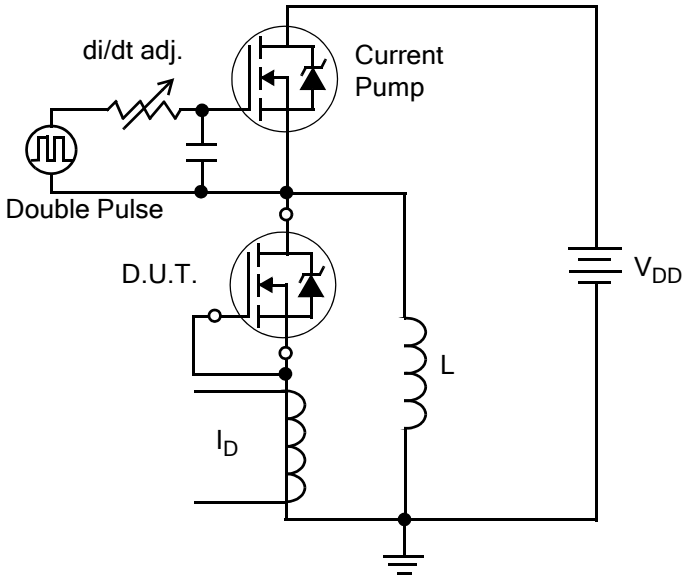


Figure 21. Diode Reverse Recovery Test Circuit

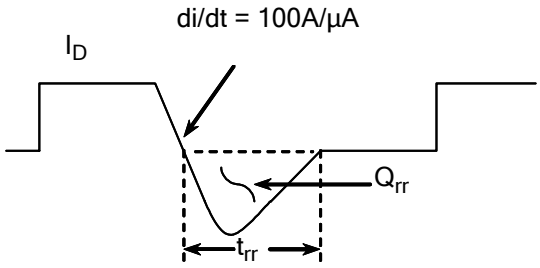


Figure 22. Diode Reverse Recovery Waveform

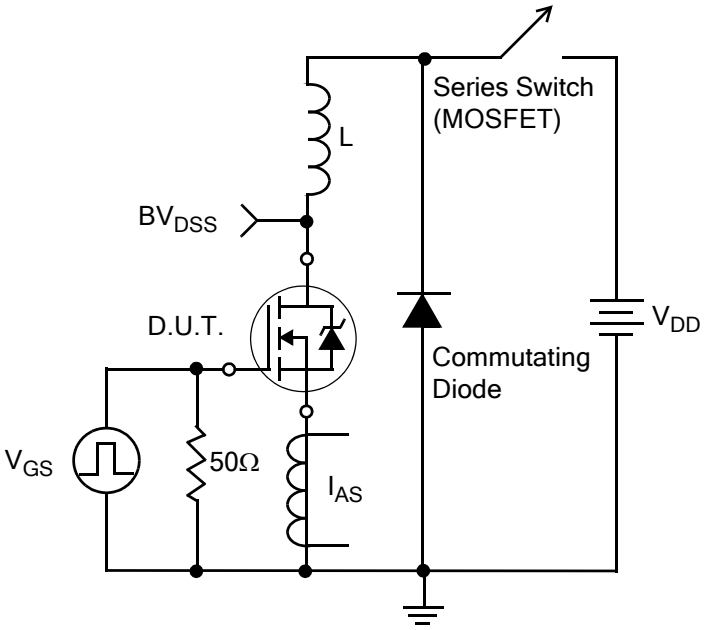
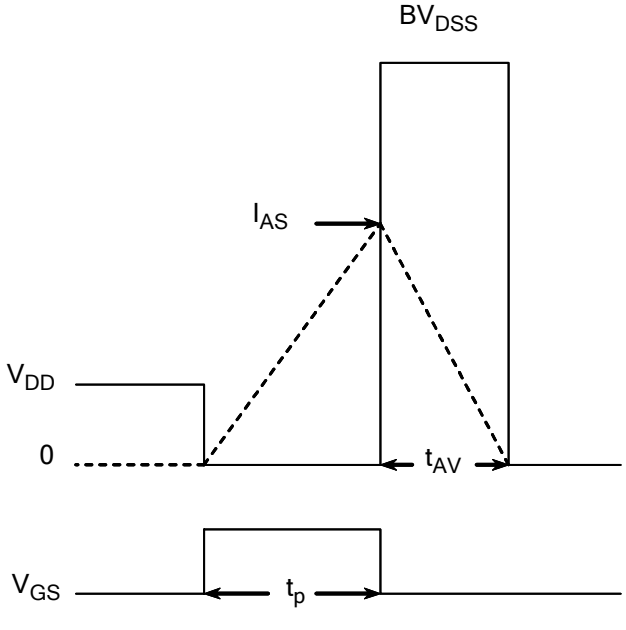


Figure 23. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}{}^2 L}{2}$$

Figure 24. Unclamped Inductive Switching Waveforms

Disclaimers:

InPower Semiconductor Co., Ltd (IPS) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to IPS's terms and conditions supplied at the time of order acknowledgement.

InPower Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent IPS deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

InPower Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using IPS's components. To minimize risk, customers must provide adequate design and operating safeguards.

InPower Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in IPS's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of IPS's products with statements different from or beyond the parameters stated by InPower Semiconductor Co., Ltd for that product or service voids all express or implied warrantees for the associated IPS's product or service and is unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for any such statements.

Life Support Policy:

InPower Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of InPower Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
    a. are intended for surgical implant into the human body,
    b. support or sustain life,
    c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.