

## N-Channel MOSFET

**Lead Free Package and Finish**

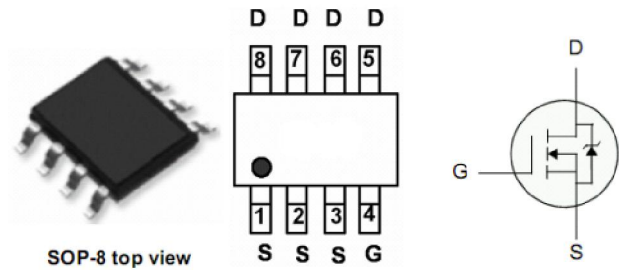
### Applications:

- Adaptor
- Charger
- SMPS
- Synchronous Rectifier

$V_{DSS}$	$R_{DS(ON)}(Typ.)$	$I_D$
100V	20mΩ	6.3A

### Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves



### Ordering Information

PART NUMBER	PACKAGE	BRAND
FTE25N10N	SOP-8	<b>IPS</b>

### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	FTE25N10N	Units
$V_{DSS}$	Drain-to-Source Voltage	100	V
$I_D$	Continuous Drain Current	6.3	A
$I_{DM}$	Pulsed Drain Current, $V_{GS}@10\text{V}$ (Note*1)	25	A
$P_D$	Power Dissipation	2	W
	Derating Factor above $25^\circ\text{C}$	0.016	$\text{W}/^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Note*2)	210	mJ
$E_{AR}$	Avalanche Energy, Repetitive	0.2	mJ
$I_{AR}$	Avalanche Current	0.2	A
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note*3)	5	$\text{V}/\text{ns}$
$T_L$	Maximum Temperature for Soldering	300	$^\circ\text{C}$
$T_J$ and $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	

### Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
$R_{\theta JA}$	Junction-to-Ambient		62.5	$^\circ\text{C}/\text{W}$	1 cubic foot chamber, free air.



# FTE25N10N

## OFF Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	100	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	1	$\mu A$	$V_{DS}=100V, V_{GS}=0V$ $T_J=25^\circ\text{C}$
		--	--	10		$V_{DS}=80V, V_{GS}=0V$ $T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	--	--	+100	nA	$V_{GS}=+20V$
	Gate-to-Source Reverse Leakage	--	--	-100		$V_{GS}=-20V$

## ON Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	20	25	m $\Omega$	$V_{GS}=10V, I_D=5A$
		--	22	25	m $\Omega$	$V_{GS}=4.5V, I_D=5A$
$V_{GS(TH)}$	Gate Threshold Voltage	1	--	3	V	$V_{DS}=V_{GS}, I_D=250\mu A$

## Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$C_{iss}$	Input Capacitance	--	4700	--	pF	$V_{GS}=0V, V_{DS}=25V$ $f=1.0\text{MHz}$
$C_{oss}$	Output Capacitance	--	217	--		
$C_{rss}$	Reverse Transfer Capacitance	--	162	--		
$Q_g$	Total Gate Charge	--	92.3	--	nC	$I_D=6A, V_{DD}=80V$ $V_{GS}=10V$
$Q_{gs}$	Gate-to-Source Charge	--	12.8	--		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	--	21	--		

## Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	25		ns	$V_{DD}=50V, I_D=5A,$ $V_G=10V R_G=10\Omega$
$t_{rise}$	Rise Time	--	22			
$t_{d(OFF)}$	Turn-Off Delay Time	--	183			
$t_{fall}$	Fall Time	--	62			



## Source-Drain Diode Characteristics

T<sub>c</sub>=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	--	--	6.2	A	T <sub>C</sub> =25°C
I <sub>SM</sub>	Maximum Pulsed Current (Body Diode)	--	--	25	A	
V <sub>SD</sub>	Diode Forward Voltage	--	--	1.5	V	I <sub>SD</sub> =6A, V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time	--	49		ns	I <sub>S</sub> =6A, di/dt=100A/us
Q <sub>rr</sub>	Reverse Recovery Charge	--	108		nC	

### Notes:

- \*1. Repetitive rating; pulse width limited by maximum junction temperature.
- \*2. L=0.27mH, I<sub>D</sub>=39.5A, Start T<sub>J</sub>=25°C
- \*3. I<sub>SD</sub> =6A, di/dt ≤100A/us, VDD≤BVDS, Start T<sub>J</sub>=25°C

## Characteristics Curve:

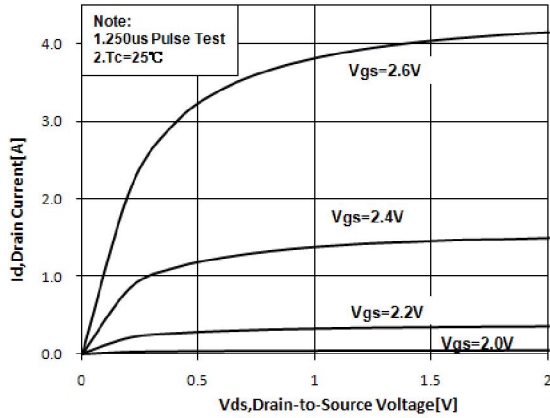


Figure 1 Output Characteristics

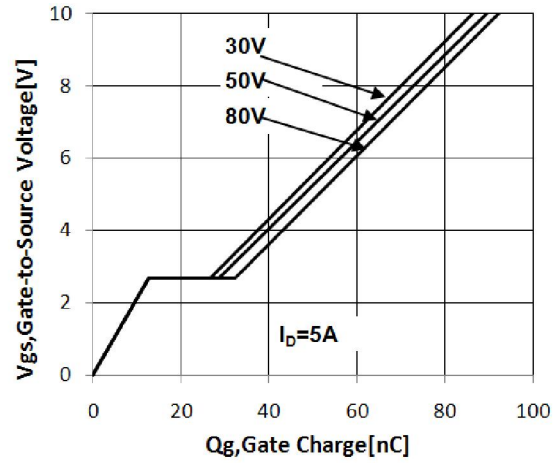


Figure 2 Gate Charge

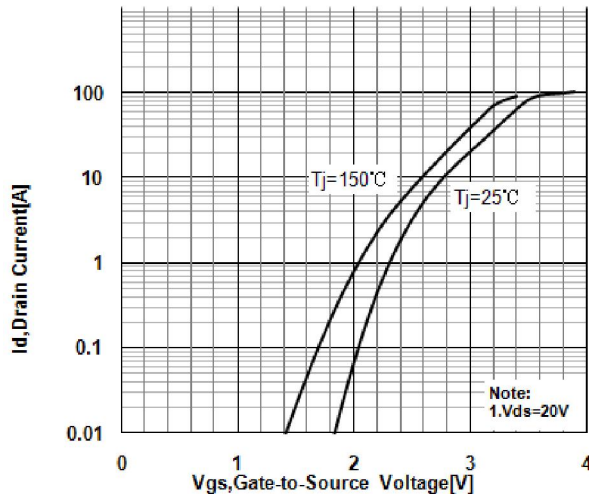


Figure 3 Transfer Characteristics

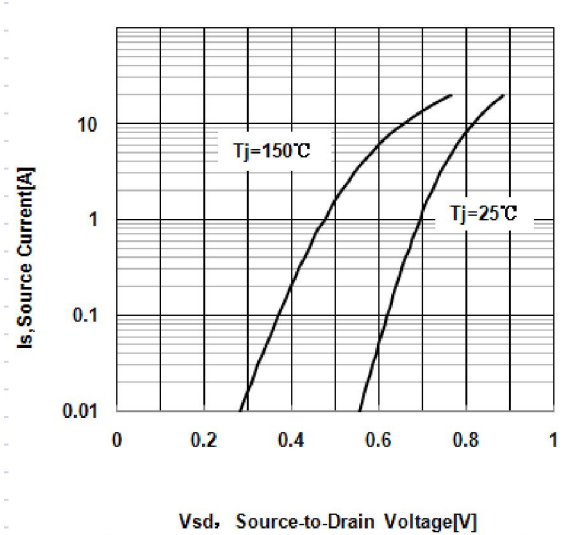


Figure 4 Source- Drain Diode Forward

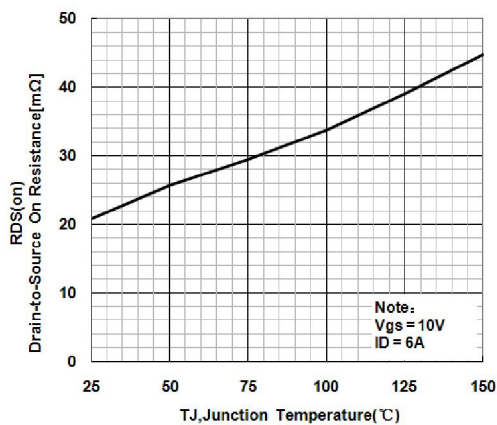


Figure 5 Rds(on)-Junction Temperature

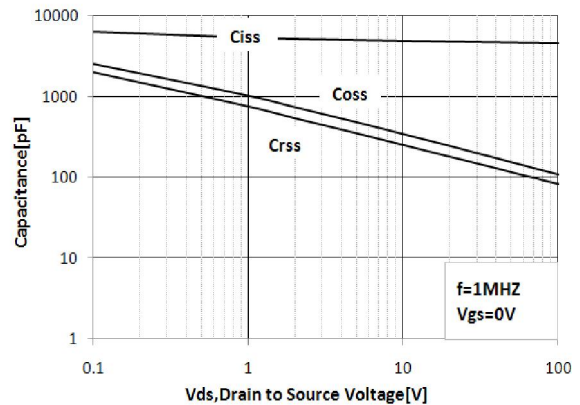


Figure 6 Capacitance vs Vds

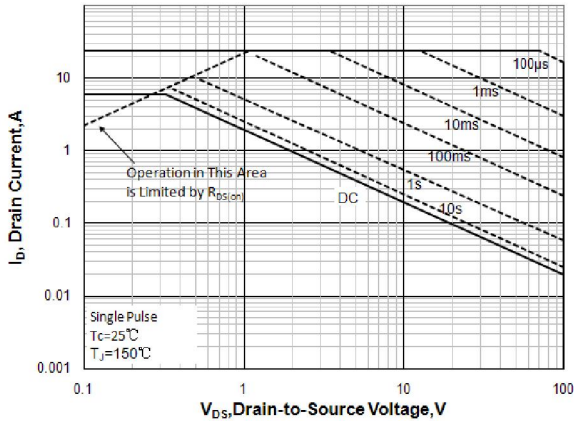


Figure 7 Maximum Safe Operating Area

Figure 7 Safe Operation Area

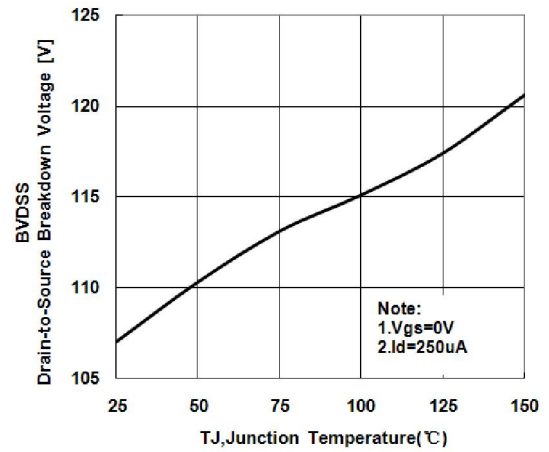


Figure 8  $BV_{DSS}$  vs Junction Temperature

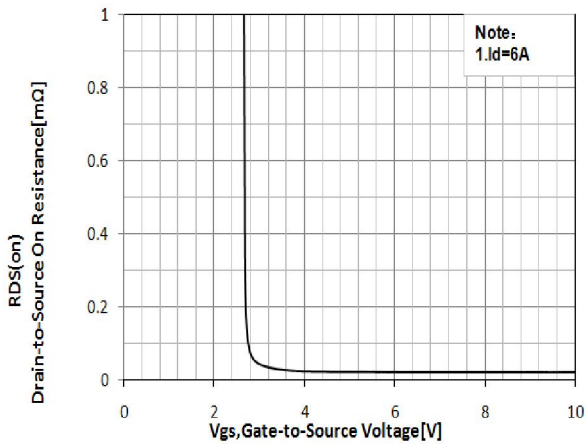


Figure 9  $R_{ds(on)}$  vs  $V_{gs}$

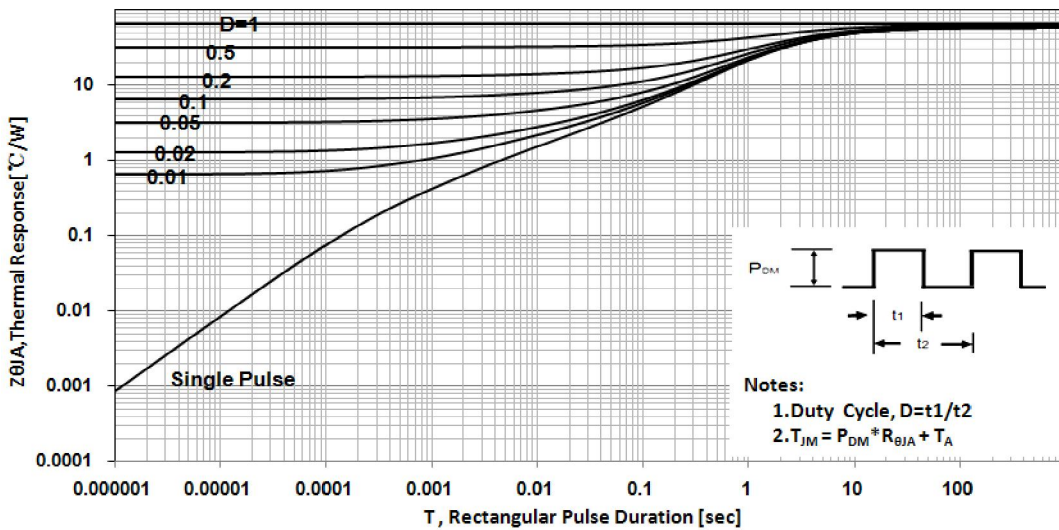


Figure 10 Normalized Maximum Transient Thermal Impedance

## Test Circuits and Waveforms

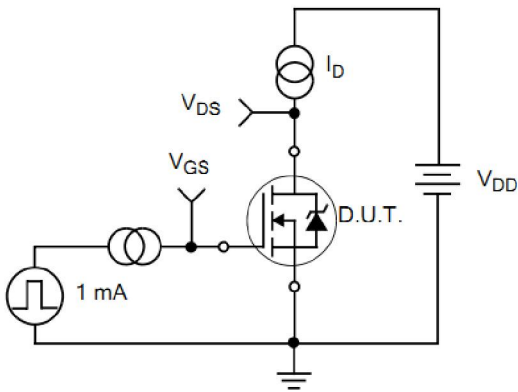


Figure 11. Gate Charge Test Circuit

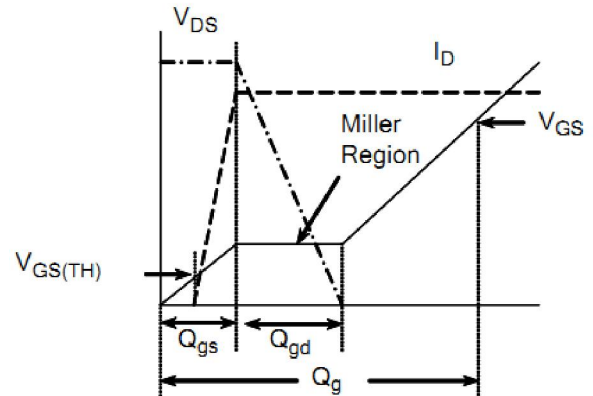


Figure 12. Gate Charge Waveforms

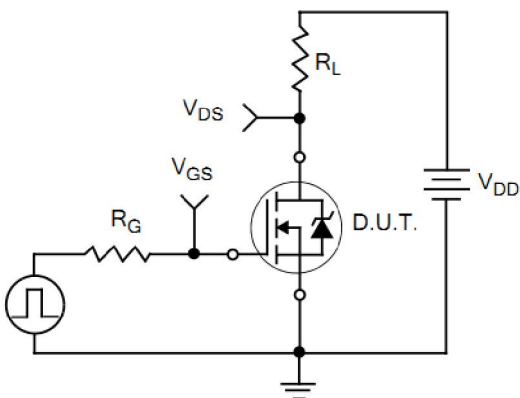


Figure 13. Resistive Switching Test Circuit

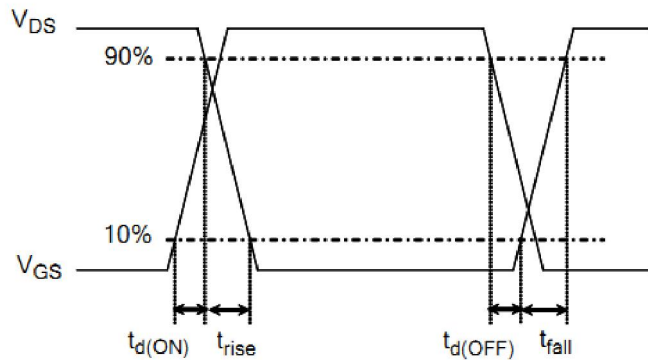


Figure 14. Resistive Switching Waveforms

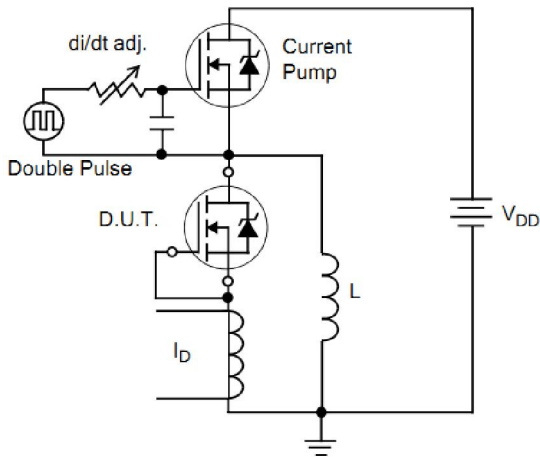


Figure 15. Diode Reverse Recovery Test Circuit

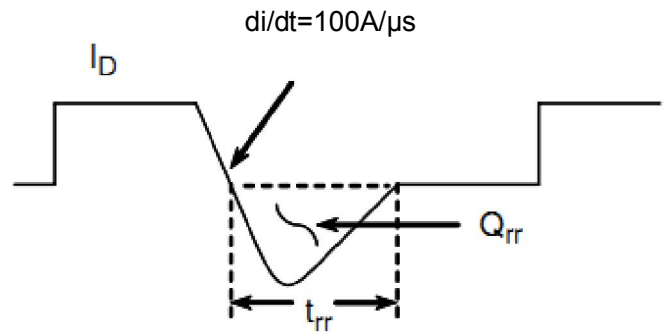


Figure 16. Diode Reverse Recovery Waveform

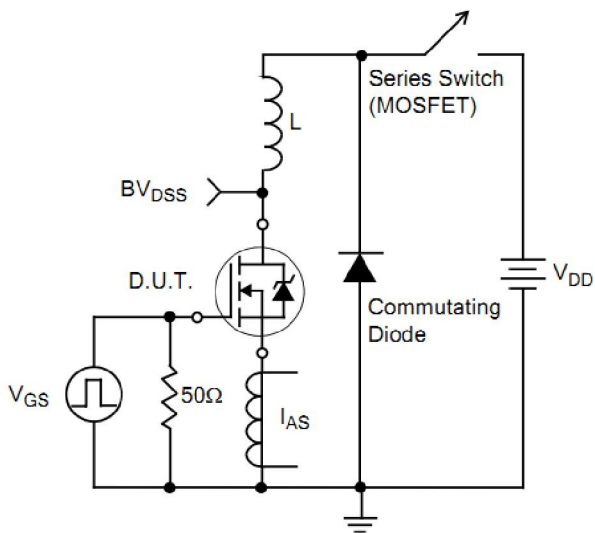


Figure 17. Unclamped Inductive Switching Test Circuit

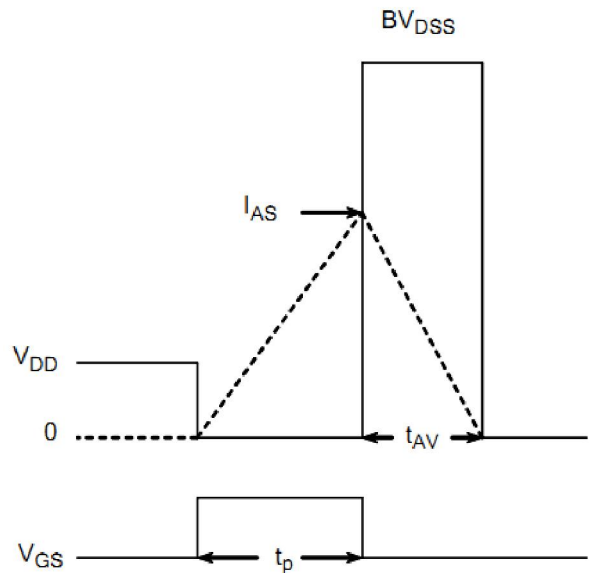


Figure 18. Unclamped Inductive Switching Waveform

$$E_{AS} = \frac{I_{AS}^2 L}{2}$$



## Disclaimers:

InPower Semiconductor Co., Ltd (IPS) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to IPS's terms and conditions supplied at the time of order acknowledgement.

InPower Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing reliability and quality control are used to the extent IPS deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

InPower Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using IPS's components. To minimize risk, customers must provide adequate design and operating safeguards.

InPower Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in IPS's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of IPS's products with statements different from or beyond the parameters stated by InPower Semiconductor Co., Ltd for that product or service voids all express or implied warranties for the associated IPS's product or service and is unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for any such statements.

---

## Life Support Policy:

InPower Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of InPower Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
  - a. are intended for surgical implant into the human body,
  - b. support or sustain life,
  - c. whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.