1.25Gbps Spring-Latch SFP Transceiver

(For 550m transmission)

Members of Flexon™ Family

Features

- Dual data-rate of 1.25Gbps/1.0625Gbps operation
- 850nm VCSEL laser and PIN photodetector
- 550m transmission with 50/125 μm MMF
- 275m transmission with 62.5/125 μm MMF
- Standard serial ID information Compatible with SFP MSA
- SFP MSA package with duplex LC connector
- With Spring-Latch for high density application
- Very low EMI and excellent ESD protection
- +3.3V single power supply
- Operating case temperature: 0 to +70°C

Applications

- Switch to Switch interface
- Switched backplane application
- Router/Server interface
- Other optical transmission systems

Standard

- Compatible with SFP MSA
- Compatible with IEEE 802.3z
- Compatible with ANSI specifications for Fibre Channel
- Compatible with FCC 47 CFR Part 15,Class B
- Compatible with FDA 21 CFR 1040.10 and 1040.11, Class I
- Compatible with Telcordia GR-468-CORE
- RoHS compliance and lead free assembly process compatibility

Description

Fiberxon FTM-8012C-SLG SFP transceiver is high performance, cost effective module supporting dual data-rate of 1.25Gbps/1.0625Gbps and 550m transmission on 50/125 μm MMF.

The transceiver consists of two sections: The transmitter section incorporates a VCSEL laser. And the receiver section consists of a PIN photodiode integrated with a trans-impedance preamplifier (TIA). All modules satisfy class I laser safety requirements.

The optical output can be disabled by a TTL logic high-level input of Tx Disable. Tx Fault is provided to indicate that degradation of the laser. Loss of signal (LOS) output is provided to indicate the loss of an input optical signal of receiver.

The standard serial ID information Compatible SFP MSA describes the transceiver's capabilities, standard interfaces, manufacturer and other information. The host equipment can access this information via the 2-wire serial CMOS EEPROM protocol. For further information, please refer to SFP Multi-Source Agreement (MSA).

FTM-8012C-SLG is compliant with RoHS .

Regulatory Compliance

The transceivers have been tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Flexon™ regulatory specification and safety guidelines, or contact with Fiberxon, Inc. America sales office listed at the end of documentation.

Table 1 - Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>500 V)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	IEC 61000-4-2 GR-1089-CORE	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compatible with standards
Immunity	IEC 61000-4-3	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compatible with Class I laser product.
Component Recognition	UL and CSA	UL file E223705
RoHS	2002/95/EC 4.1&4.2	Compliant with standards

Absolute Maximum Ratings

Stress in excess of the maximum absolute ratings can cause permanent damage to the module.

Table 2 – Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Operating Relative Humidity	-	5	95	%

Recommended Operating Conditions

Table 3 - Recommended Operating Conditions

Parameter		Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature		T_C	0		+70	°C
Power Supply Voltage		V_{CC}	3.13		3.47	V
Power Supply Current		I_{CC}		190	300	mA
Data Rate	Gigabit Ethernet			1.25		Gbps
	Fibre Channel			1.0625		

Optical and Electrical Characteristics

Table 4 –Optical and Electrical Characteristics

Parameter		Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter							
Centre Wavelength		λ_C	830	850	860	nm	
Average Output Power		P_{0ut}	-9.5		-4	dBm	1
P_{OUT} @TX Disable Asserted		P_{0ut}			-45	dBm	1
Spectral Width (RMS)		σ			0.85	nm	
Extinction Ratio		ER	9			dB	
Rise/Fall Time (20%~80%)		t_r /t_f			0.26	ns	2
Total Jitter	1.25G	T_J			0.431	UI	3
	1.0625G				0.43		
Deterministic Jitter	1.25G	D_J			0.2	UI	3
	1.0625G				0.21		
Output Optical Eye		IEEE 802.3z and ANSI Fibre Channel Compatible					4
Differential Data Input Swing		V_{IN}	500		1660	mV	5
Differential Input Impedance		Z_{IN}	90	100	110	Ω	
TX Disable	Disable		2.0		Vcc	V	
	Enable		0		0.8	V	
TX Fault	Fault		2.0		Vcc+0.3	V	
	Normal		0		0.8	V	
Receiver							
Centre Wavelength		λ_C	770		860	nm	
Receiver Sensitivity					-17	dBm	6
Receiver Overload			0			dBm	6
Return Loss			12			dB	
LOS De-Assert		LOS_D			-18	dBm	
LOS Assert		LOS_A	-30			dBm	
LOS Hysteresis			1		4	dB	
Total Jitter	1.25G	T_J			0.749	UI	3
	1.0625G				0.61		
Deterministic Jitter	1.25G	D_J			0.462	UI	3
	1.0625G				0.36		
Differential Data Output Swing		V_{OUT}	370		2000	mV	5
LOS	High		2.0		Vcc+0.3	V	
	Low		0		0.8	V	

Notes:

1. The optical power is launched into MMF.
2. Unfiltered, measured with a PRBS 2^7-1 test pattern @1.25Gbps
3. Meet the specified maximum output jitter requirements if the specified maximum input jitter is present.
4. Measured with a PRBS 2^7-1 test pattern @1.25Gbps/1.0625Gbps.
5. PECL logic, internally AC coupled.
6. Measured with a PRBS 2^7-1 test pattern @1.25Gbps, worst-case extinction ratio, BER $\leqslant 1\times 10^{-12}$.

EEPROM Information

The SFP MSA defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard interfaces, manufacturer, and other information, which is accessible over a 2 wire serial interface at the 8-bit address 1010000X (A0h). The memory contents refer to Table 5

Table 5 - EEPROM Serial ID Memory Contents (A0h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
0	1	Identifier	03	SFP
1	1	Ext. Identifier	04	MOD4
2	1	Connector	07	LC
3—10	8	Transceiver	00 00 00 01 20 40 0C 01	Transmitter Code
11	1	Encoding	01	8B10B
12	1	BR, nominal	0D	1.25Gbps
13	1	Reserved	00	
14	1	Length (9um)-km	00	
15	1	Length (9um)	00	
16	1	Length (50um)	37	550m
17	1	Length (62.5um)	1B	270m
18	1	Length (copper)	00	
19	1	Reserved	00	
20—35	16	Vendor name	46 49 42 45 52 58 4F 4E 20 49 4E 43 2E 20 20 20	"FIBERXON INC. "(ASCⅡ)
36	1	Reserved	00	
37—39	3	Vendor OUI	00 00 00	
40—55	16	Vendor PN	46 54 4D 2D 38 30 31 32 43 2D 53 4C 47 20 20 20	"FTM-8012C-SLG " (ASCⅡ)
56—59	4	Vendor rev	xx xx 20 20	ASCⅡ("31 30 20 20" means 1.0 revision)
60-61	2	Wavelength	03 52	850nm
62	1	Reserved	00	
63	1	CC BASE	xx	Check sum of bytes 0 - 62
64—65	2	Options	00 1A	LOS, TX_FAULT and TX_DISABLE
66	1	BR, max	00	
67	1	BR, min	00	
68—83	16	Vendor SN	xx xx xx xx xx xx xx xx xx xx xx xx 20 20 20 20	ASCⅡ, 12 bytes are used for Fiberxon SFPs
84—91	8	Vendor date code	xx xx xx xx xx xx 20 20	Year(2 byte), Month(2 byte), Day (2 byte)
92—94	3	Reserved	00 00 00	
95	1	CC EXT	xx	Check sum of bytes 64 - 94
96—255	160	Vendor specific		

Note: The "xx" byte should be filled in according to practical case. For more information, please refer to the related document of SFP Multi-Source Agreement (MSA).

Recommended Host Board Power Supply Circuit

Figure 1 shows the recommended host board power supply circuit.

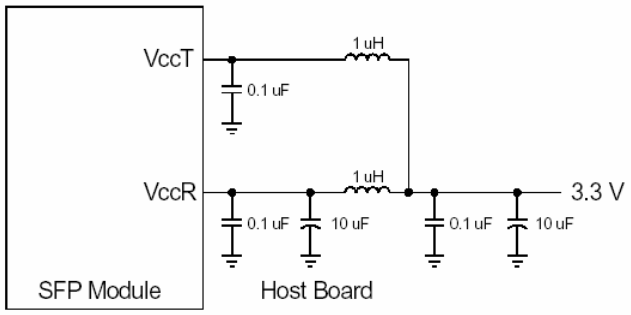
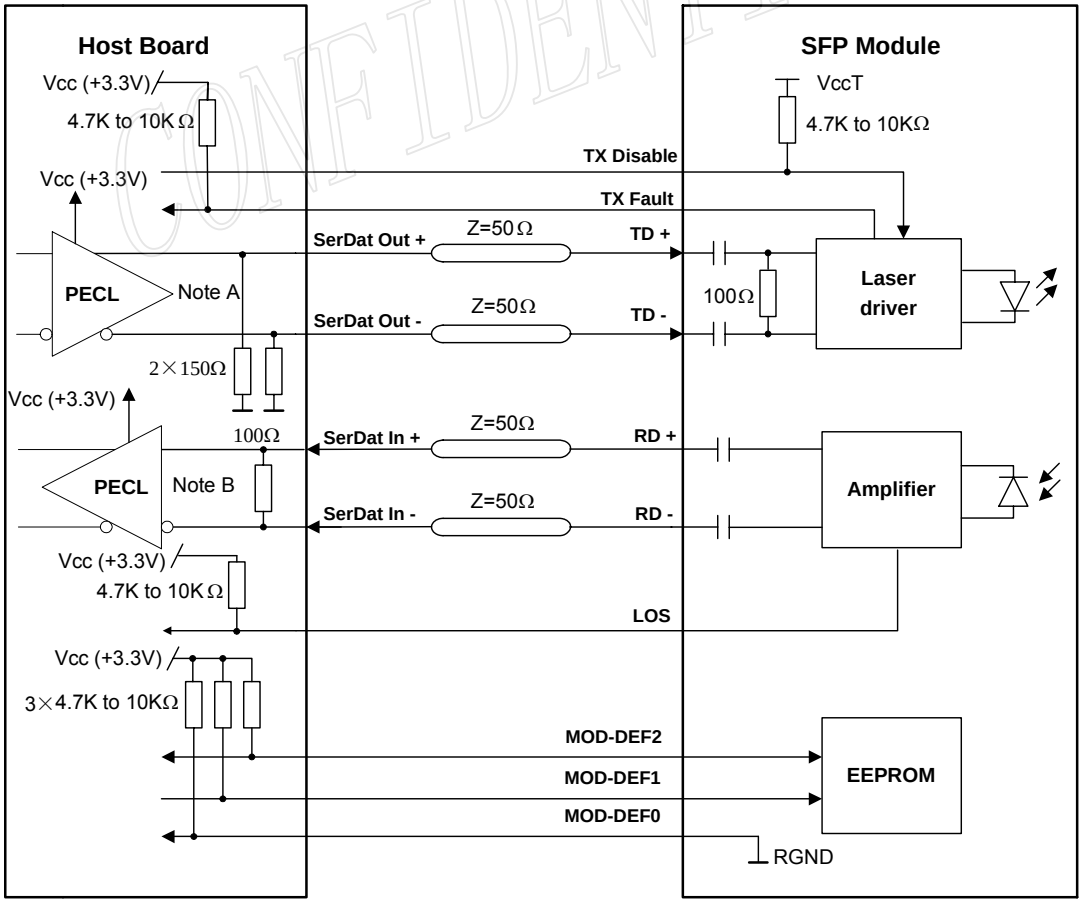


Figure 1, Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

Figure 2 shows the recommended interface circuit.



Note A: Circuit assumes open emitter output
Note B: Circuit assumes high impedance internal bias @Vcc-1.3V

Figure 2, Recommended Interface Circuit

Pin Definitions

Figure 3 below shows the pin numbering of SFP electrical interface. The pin functions are described in Table 6 with some accompanying notes.

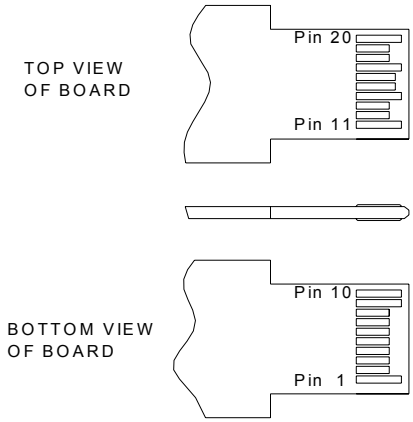


Figure 3, Pin View

Table 6 – Pin Function Definitions

Pin No.	Name	Function	Plug Seq.	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	Note 1
3	TX Disable	Transmitter Disable	3	Note 2
4	MOD-DEF2	Module Definition 2	3	Note 3
5	MOD-DEF1	Module Definition 1	3	Note 3
6	MOD-DEF0	Module Definition 0	3	Note 3
7	Rate Select	Not Connected	3	
8	LOS	Loss of Signal	3	Note 4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inv. Received Data Out	3	Note 5
13	RD+	Received Data Out	3	Note 5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power	2	
16	VccT	Transmitter Power	2	
17	VeeT	Transmitter Ground	1	
18	TD+	Transmit Data In	3	Note 6
19	TD-	Inv. Transmit Data In	3	Note 6
20	VeeT	Transmitter Ground	1	

Notes:

1. TX Fault is an open collector output, which should be pulled up with a 4.7k~10kΩ resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates a laser fault of some kind. In the low state, the output will be pulled to less than 0.8V.
2. TX Disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7k~10kΩ resistor. Its states are:
   Low (0~0.8V): Transmitter on
   (>0.8V, <2.0V): Undefined
   High (2.0~3.465V): Transmitter Disabled

Open: Transmitter Disabled

3. MOD-DEF 0,1,2 are the module definition pins. They should be pulled up with a 4.7k~10kΩ resistor on the host board. The pull-up voltage shall be VccT or VccR.
   MOD-DEF 0 is grounded by the module to indicate that the module is present
   MOD-DEF 1 is the clock line of two wire serial interface for serial ID
   MOD-DEF 2 is the data line of two wire serial interface for serial ID
4. LOS is an open collector output, which should be pulled up with a 4.7k~10kΩ resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates loss of signal. In the low state, the output will be pulled to less than 0.8V.
5. These are the differential receiver output. They are internally AC-coupled 100Ω differential lines which should be terminated with 100Ω (differential) at the user SERDES.
6. These are the differential transmitter inputs. They are AC-coupled, differential lines with 100Ω differential termination inside the module.

Mechanical Design Diagram

The mechanical design diagram is shown in Figure 4.

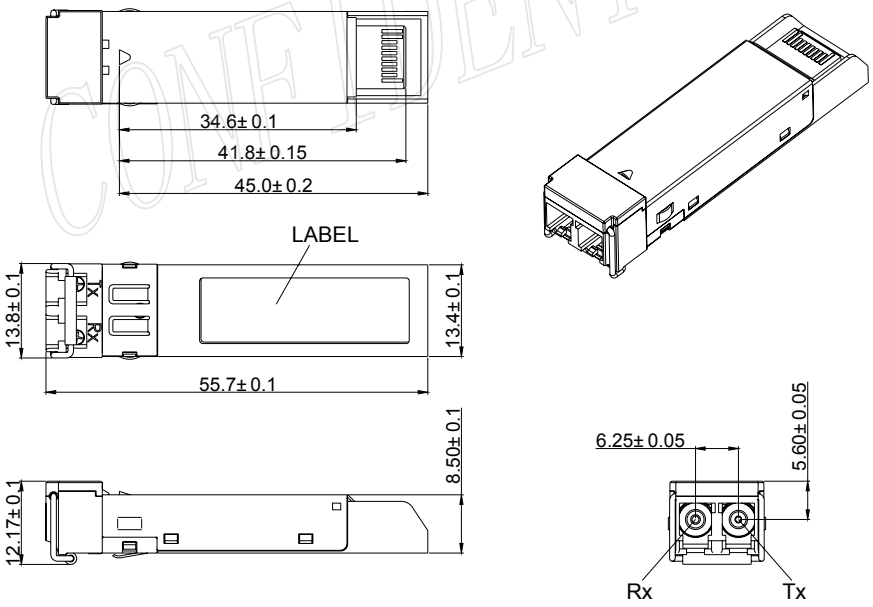
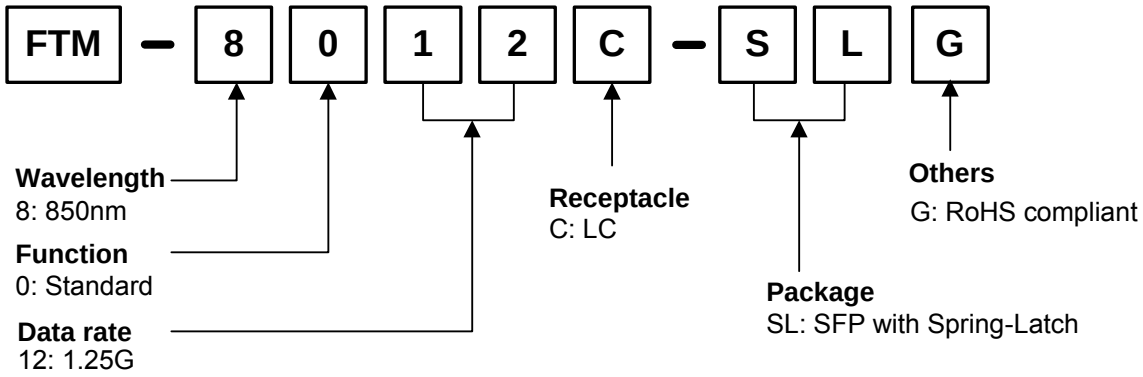


Figure 4, Mechanical Design Diagram of SFP with Spring-Latch

Ordering Information



Part No.	Product Description
FTM-8012C-SLG	850nm, 1.25Gbps, 550m, SFP with Spring-Latch, 0°C~+70°C

Related Documents

For further information, please refer to the following documents:

- *Fiberxon Spring-Latch SFP Installation Guide*
- *Fiberxon SFP Application Notes*
- *SFP Multi-Source Agreement (MSA)*

Obtaining Document

You can visit our website:

http://www.fiberxon.com

Or contact with Fiberxon, Inc. America Sales Office listed at the end of documentation to get the latest documents.

Revision History

Revision	Initiate	Review	Approve	Subject	Release Date
Rev. 1a	Zeus.Shen	Simon.Jiang	Walker.Wei	Initial datasheet	July 8, 2005
Rev. 1b	Univer.Yang	Simon.Jiang	Walker.Wei	Recense preliminary version	Feb. 28, 2006

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Contact

U.S.A. Headquarter:
5201 Great America Parkway, Suite 340
Santa Clara, CA 95054
U. S. A.
Tel: 408-562-6288
Fax: 408-562-6289
Or visit our website: http://www.fiberxon.com