



# FTP02N65B FTA02N65B FTQ02N65B

## N-Channel MOSFET

Lead Free Package and Finish

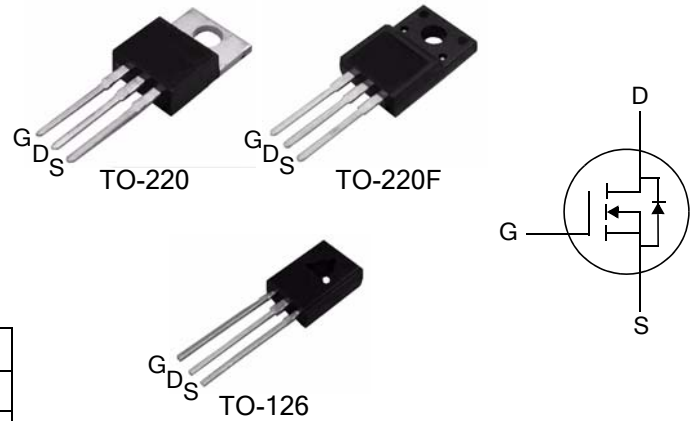
### Applications:

- Adaptor
- Charger
- SMPS Standby Power
- LCD Panel Power

$V_{DSS}$	$R_{DS(ON)}$ (Max.)	$I_D$
650V	8.0 $\Omega$	1.5A

### Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves



### Ordering Information

PART NUMBER	PACKAGE	BRAND
FTP02N65B	TO-220	FTP02N65B
FTA02N65B	TO-220F	FTA02N65B
FTQ02N65B	TO-126	Q02N65B

Packages  
Not to Scale

### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	FTP02N65B FTQ02N65B	FTA02N65B	Units
$V_{DSS}$	Drain-to-Source Voltage (NOTE *1)	650		V
$I_D$	Continuous Drain Current	1.5	1.5*	A
$I_{D@100^\circ\text{C}}$	Continuous Drain Current	Figure 3		
$I_{DM}$	Pulsed Drain Current, $V_{GS}@10\text{V}$ (NOTE *2)	Figure 6		
$P_D$	Power Dissipation	52	21	W
	Derating Factor above $25^\circ\text{C}$	0.42	0.17	W/ $^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulse Avalanche Energy $L=10\text{mH}$ , $I_D=2.24\text{Amps}$	25		mJ
$I_{AS}$	Pulsed Avalanche Rating	Figure 8		
dv/dt	Peak Diode Recovery dv/dt (NOTE *3)	3.0		V/ns
$T_L$ $T_{PKG}$	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds	300		$^\circ\text{C}$
	Package Body for 10 seconds	260		
$T_J$ and $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150		

\*Drain current limited by Maximum Junction Temperature.

**Caution:** Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

## Thermal Resistance

Symbol	Parameter	FTP02N65B FTQ02N65B	FTA02N65B	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	2.4	6.0	°C/W	Water cooled heatsink, $P_D$ adjusted for a peak junction temperature of +150 °C.
$R_{\theta JA}$	Junction-to-Ambient	62	100		1 cubic foot chamber, free air.

## OFF Characteristics $T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	650	--	--	V	$V_{GS}=0V$ , $I_D=250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient, Figure 11.	--	0.572	--	V/°C	Reference to 25 °C, $I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	25	$\mu A$	$V_{DS}=650V$ , $V_{GS}=0V$
		--	--	250		$V_{DS}=520V$ , $V_{GS}=0V$ $T_J=125\text{ }^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	--	--	100	nA	$V_{GS}=+30V$
	Gate-to-Source Reverse Leakage	--	--	-100		$V_{GS}=-30V$

## ON Characteristics $T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance Figure 9 and 10.	--	6.5	8.0	$\Omega$	$V_{GS}=10V$ , $I_D=0.9A$ (NOTE *4)
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2.0	--	4.0	V	$V_{DS}=V_{GS}$ , $I_D=250\mu A$
gfs	Forward Transconductance	--	2.2	--	S	$V_{DS}=15V$ , $I_D=1.5A$ (NOTE *4)

## Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$C_{iss}$	Input Capacitance	--	246	--	pF	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$ Figure 14
$C_{oss}$	Output Capacitance	--	28.5	--		
$C_{rss}$	Reverse Transfer Capacitance	--	7.5	--		
$Q_g$	Total Gate Charge	--	12.2	--	nC	$V_{DD}=325V$ $I_D=1.5A$ Figure 15
$Q_{gs}$	Gate-to-Source Charge	--	2.0	--		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	--	6.6	--		

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	6	--	ns	$V_{DD}=325V$ $I_D=1.5A$ $V_{GS}=10V$ $R_G=10\Omega$
$t_{rise}$	Rise Time	--	19	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	17	--		
$t_{fall}$	Fall Time	--	16	--		

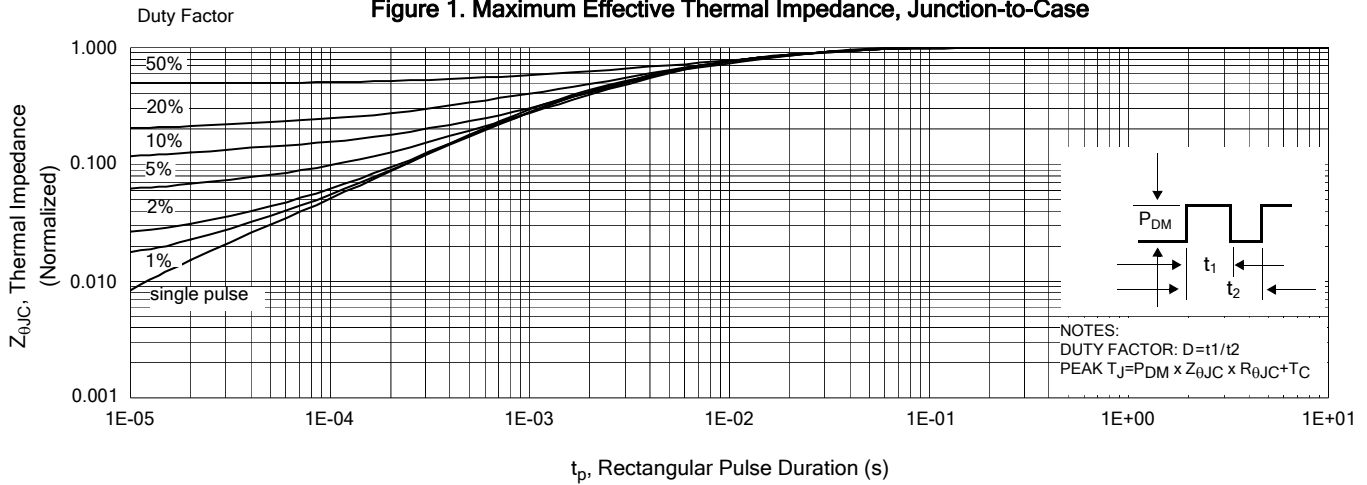
**Source-Drain Diode Characteristics**  $T_C=25^\circ C$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	--	--	1.5	A	Integral pn-diode in MOSFET
$I_{SM}$	Maximum Pulsed Current (Body Diode)	--	--	6.0	A	
$V_{SD}$	Diode Forward Voltage	--	--	1.5	V	$I_S=1.5A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	17.2	25.8	ns	$V_{GS}=0V$ $I_F=1.5A, di/dt=100 A/\mu s$
$Q_{rr}$	Reverse Recovery Charge	--	150	225	nC	

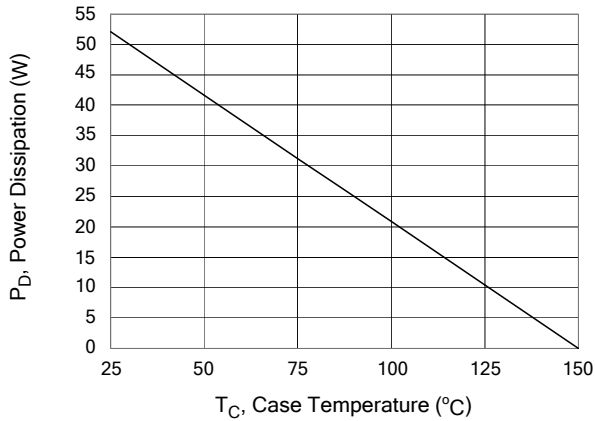
Notes:

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- \*1.  $T_J = +25^\circ C$  to  $+150^\circ C$ .
  - \*2. Repetitive rating; pulse width limited by maximum junction temperature.
  - \*3.  $I_{SD}= 1.5A$   $di/dt \leq 100 A/\mu s$ ,  $V_{DD} \leq BV_{DSS}$ ,  $T_J=+150^\circ C$ .
  - \*4. Pulse width  $\leq 380\mu s$ ; duty cycle  $\leq 2\%$ .

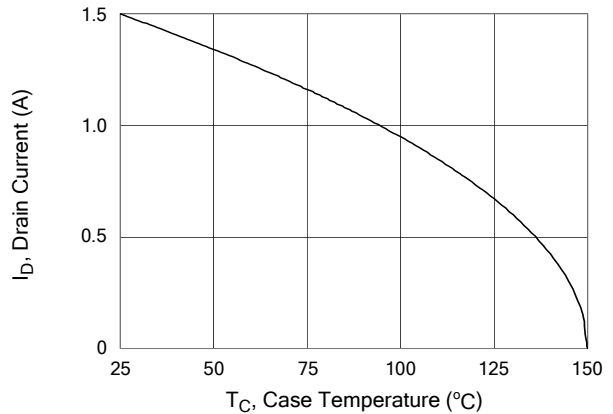
**Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case**



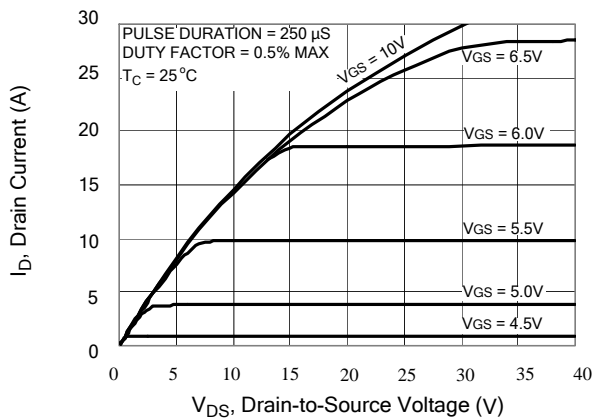
**Figure 2. Maximum Power Dissipation vs Case Temperature**



**Figure 3. Maximum Continuous Drain Current vs Case Temperature**



**Figure 4. Typical Output Characteristics**



**Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current**

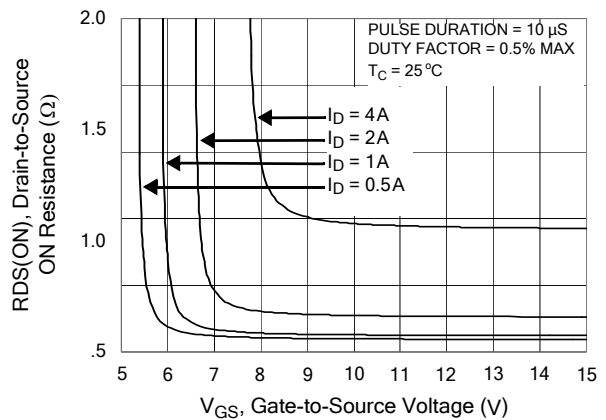


Figure 6. Maximum Peak Current Capability

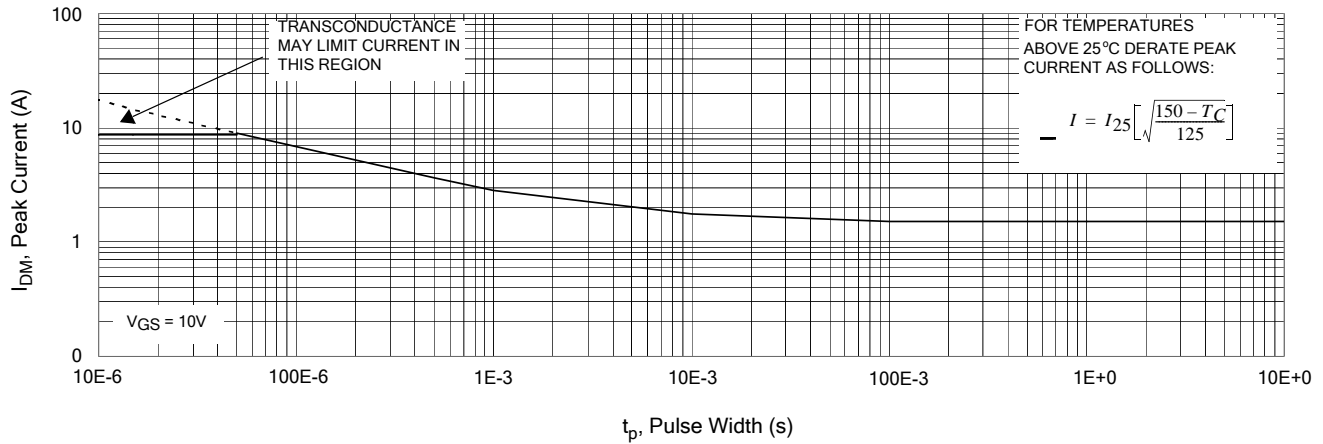


Figure 7. Typical Transfer Characteristics

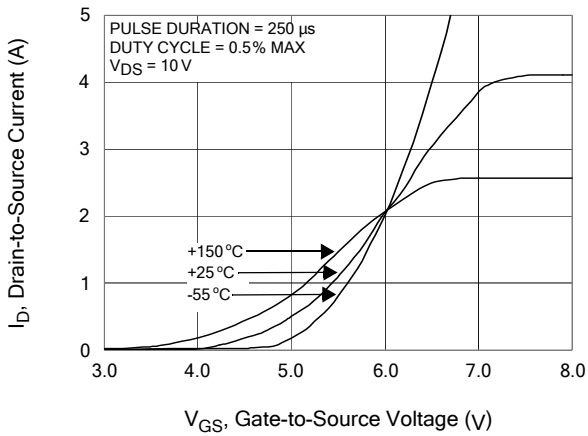


Figure 8. Unclamped Inductive Switching Capability

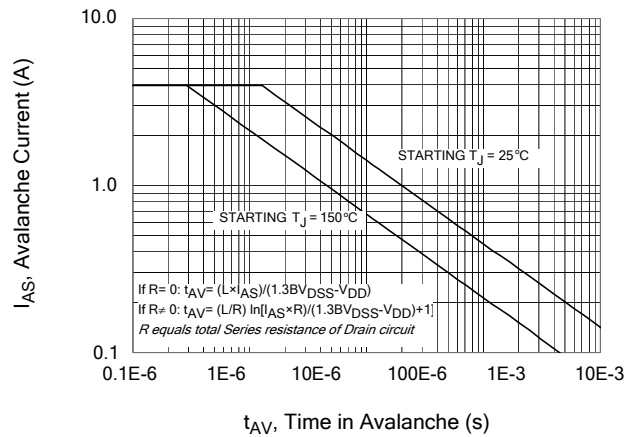


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

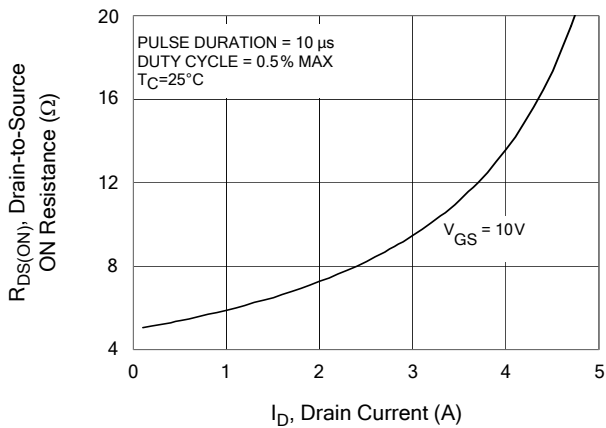
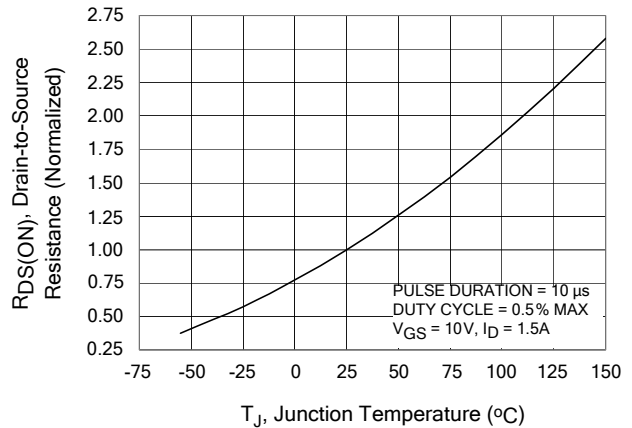
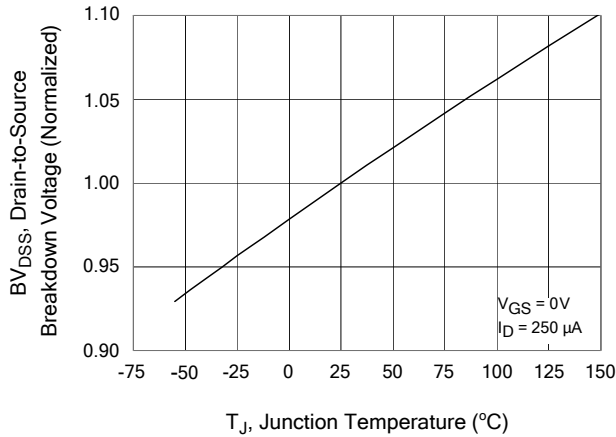


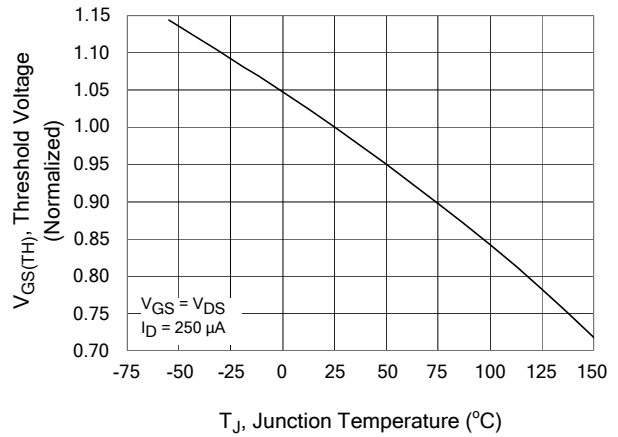
Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



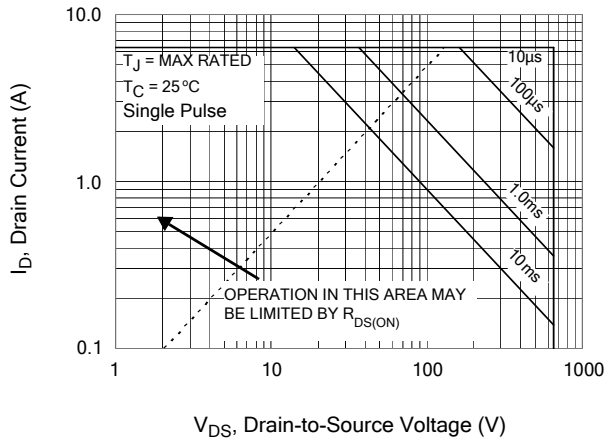
**Figure 11. Typical Breakdown Voltage vs Junction Temperature**



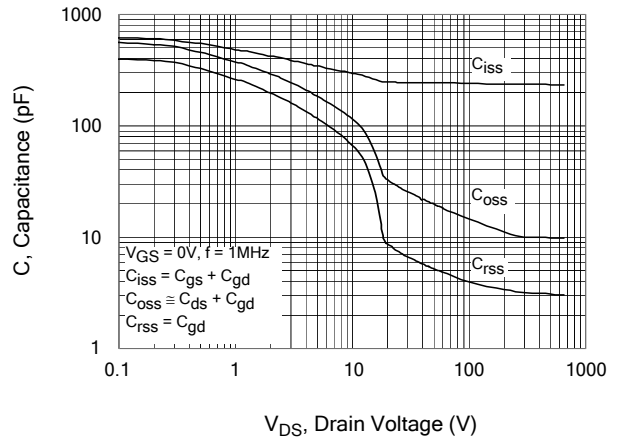
**Figure 12. Typical Threshold Voltage vs Junction Temperature**



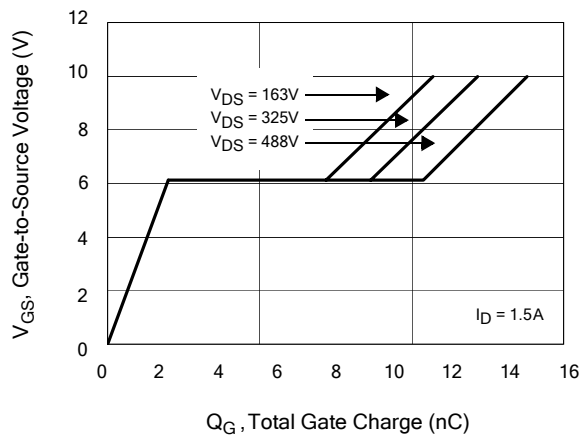
**Figure 13. Maximum Forward Bias Safe Operating Area**



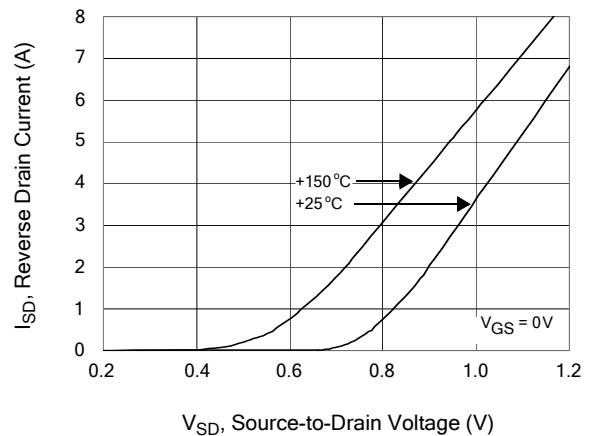
**Figure 14. Typical Capacitance vs Drain-to-Source Voltage**



**Figure 15. Typical Gate Charge vs Gate-to-Source Voltage**



**Figure 16. Typical Body Diode Transfer Characteristics**



# Test Circuits and Waveforms

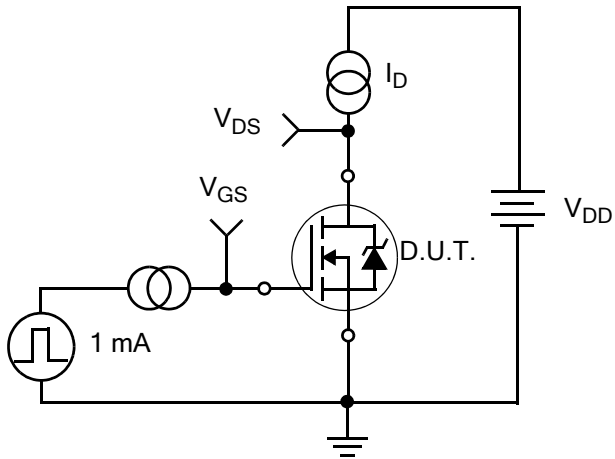


Figure 17. Gate Charge Test Circuit

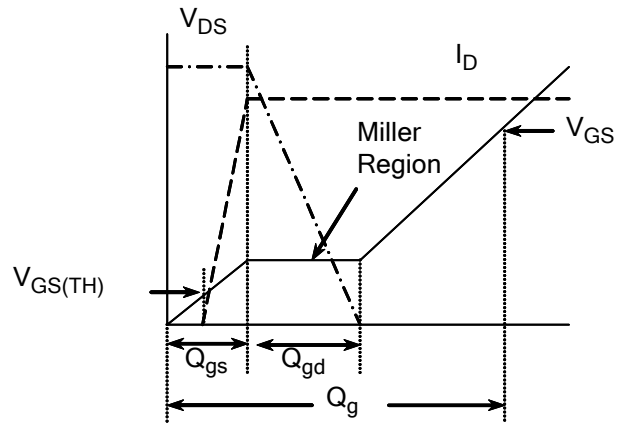


Figure 18. Gate Charge Waveform

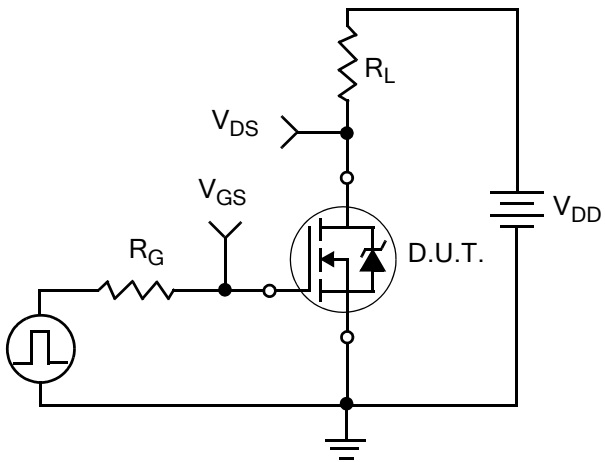


Figure 19. Resistive Switching Test Circuit

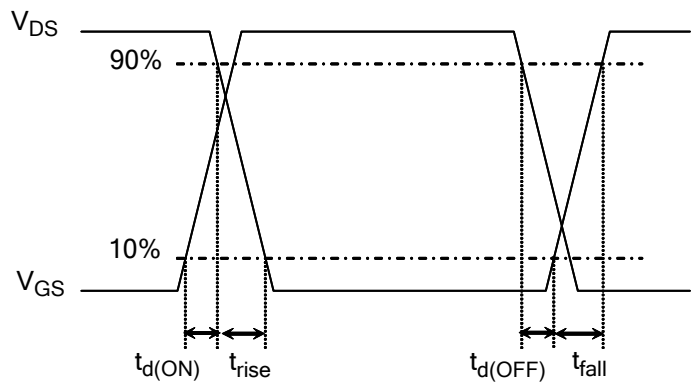


Figure 20. Resistive Switching Waveforms

## Test Circuits and Waveforms

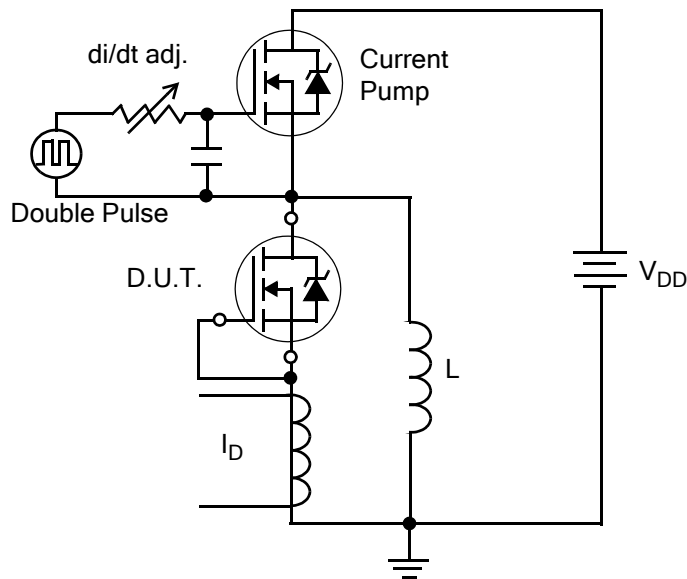


Figure 21. Diode Reverse Recovery Test Circuit

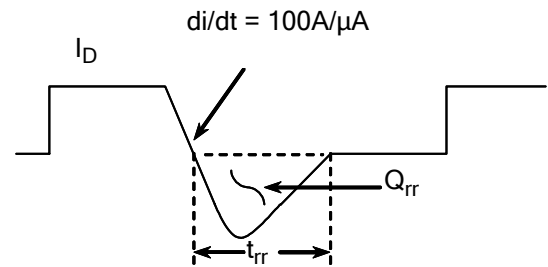


Figure 22. Diode Reverse Recovery Waveform

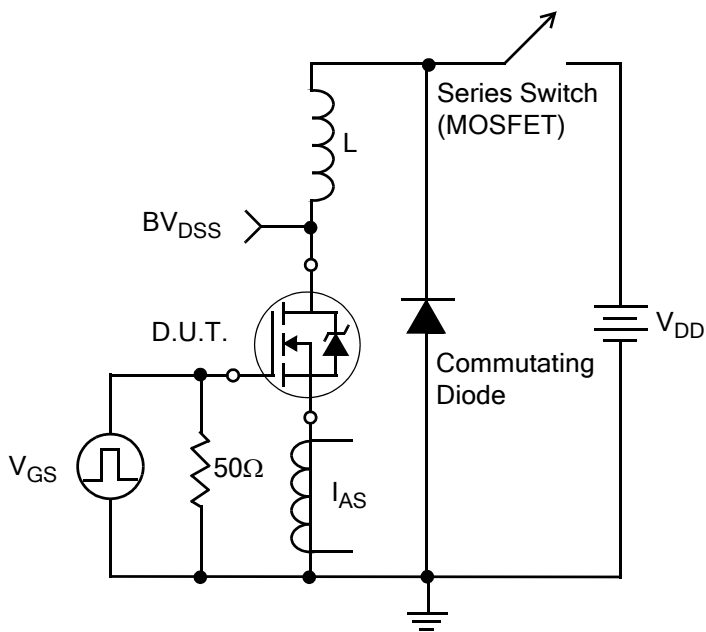


Figure 23. Unclamped Inductive Switching Test Circuit

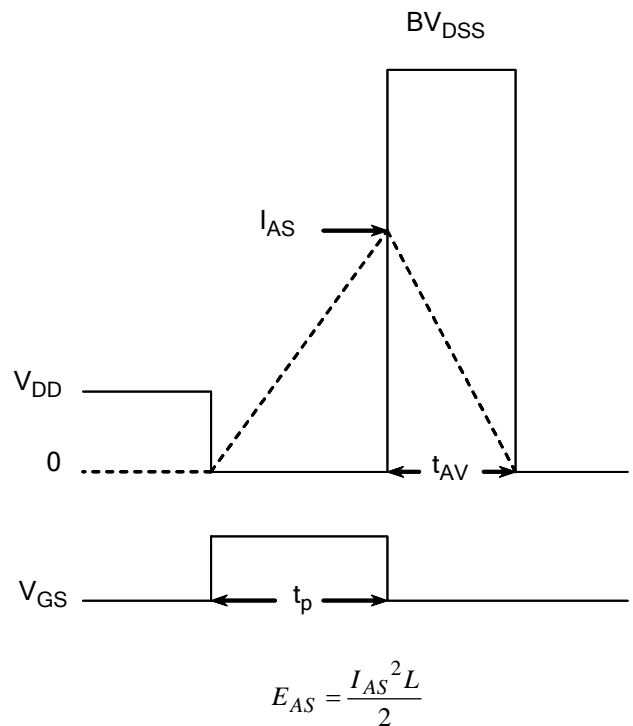


Figure 24. Unclamped Inductive Switching Waveforms



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