FTP08N08NE

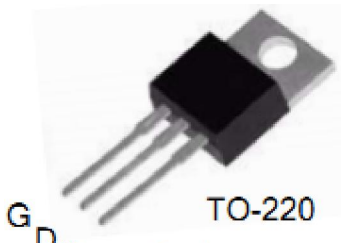
N-Channel MOSFET

Lead Free Package and Finish

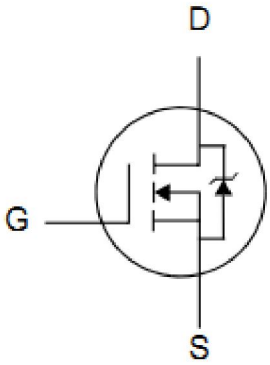
Applications:
- Adaptor
- Charger
- SMPS

V_{DSS}	$R_{DS(ON)}$(Typ.)	I_D
85V	6.6mΩ	100A

Features:
- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves



Packages
Not to Scale



Ordering Information

PART NUMBER	PACKAGE	BRAND
FTP08N08NE	TO-220	***IPS***

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	FTP08N08NE	Units
V_{DSS}	Drain-to-Source Voltage	85	V
I_D	Continuous Drain Current	100	A
	Continuous Drain Current T_C =100℃	65	A
I_{DM}	Pulsed Drain Current (NOTE *1)	400	A
P_D	Power Dissipation	198	W
	Derating Factor above 25℃	1.58	W/℃
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy(NOTE *2)	460	mJ
T_L	Maximum Temperature for Soldering	300	℃
T_J and T_{STG}	Operating Junction and Storage Temperature Range	150，-55 to150	

Thermal Resistance

Symbol	Parameter	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	0.63	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

OFF Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	85	--	--	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=85V, V_{GS}=0V T_J=25℃
		--	--	100		V_{DS}=68V, V_{GS}=0V T_J=125℃
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	V_{GS}=+20V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -20V

ON Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	StaticDrain-to-Source On-Resistance	--	6.6	8.5	mΩ	V_{GS}=10V, I_D=50A
$V_{GS(TH)}$	Gate Threshold Voltage	2	--	4	V	V_{DS}=V_{GS},I_D=250μA
Pulse width ≤300μs; duty cycle≤ 2%						

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	3564	--	pF	V_{GS}= 0V,V_{DS} = 25V f =1.0MHz
C_{oss}	Output Capacitance	--	408	--		
C_{rss}	Reverse Transfer Capacitance	--	237	--		
Q_g	Total Gate Charge	--	59.8	--	nC	I_D=50A,V_{DD}=64V V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	--	17.6	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	20.8	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	32.3	--	ns	V_{DD}=40V, I_D=50A, V_G=10V R_G=5Ω
t_{rise}	Rise Time	--	22.7	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	55.5	--		
t_{fall}	Fall Time	--	13.9	--		

Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	100	A	T_C=25℃
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	400	A	
V_{SD}	Diode Forward Voltage	--	--	1.2	V	I_{SD}=50A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	44	--	ns	I_F= I_S di/dt=100A/us
Q_{rr}	Reverse Recovery Charge	--	78.8	--	nC	
Pulse width ≤300μs; duty cycle ≤ 2%						

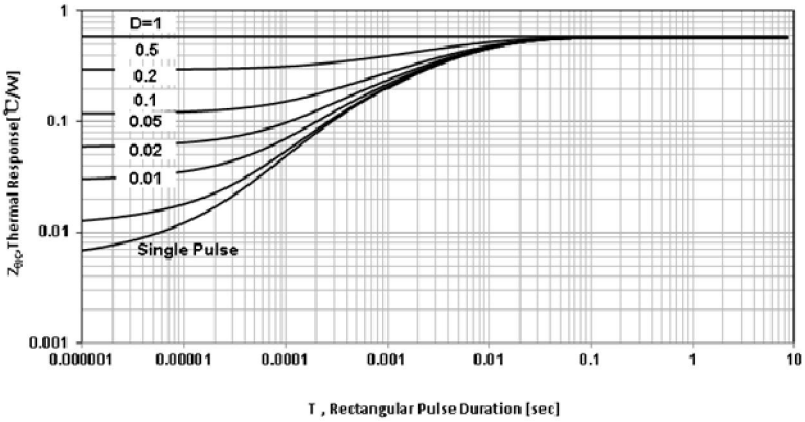
Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. L=0.5mH, I_D=43A, Start T_J=25℃

Characteristics Curve：

Figure 1.Maximum Effective Thermal Impedance，Junction-to-Case



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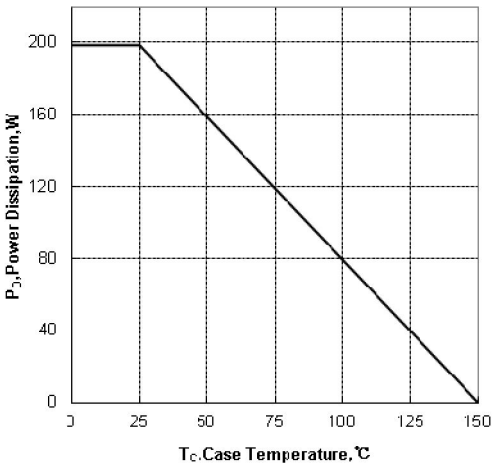
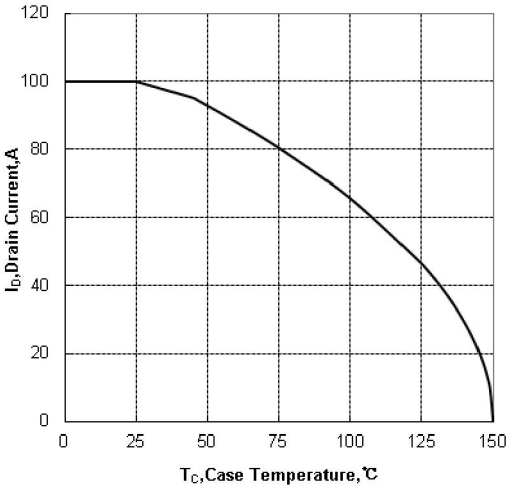
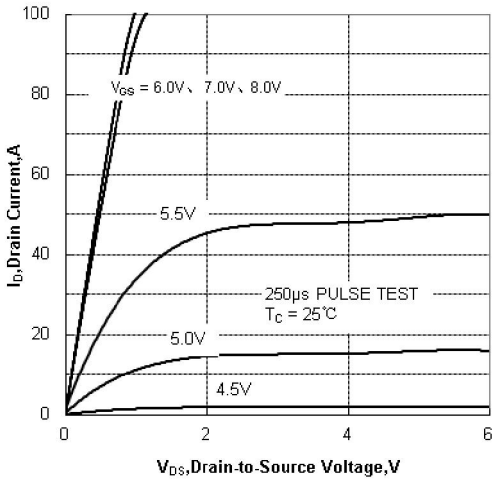






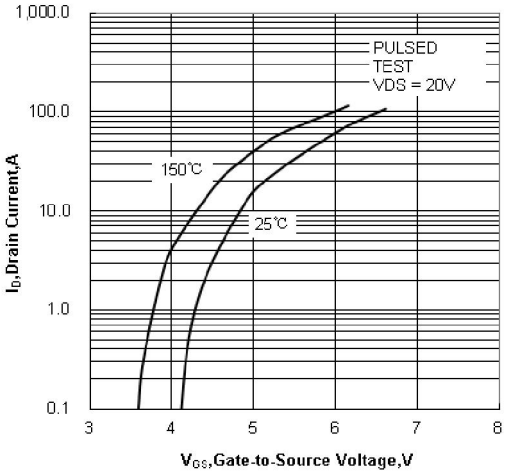


Figure 6. Typical Body Diode Transfer Characteristics

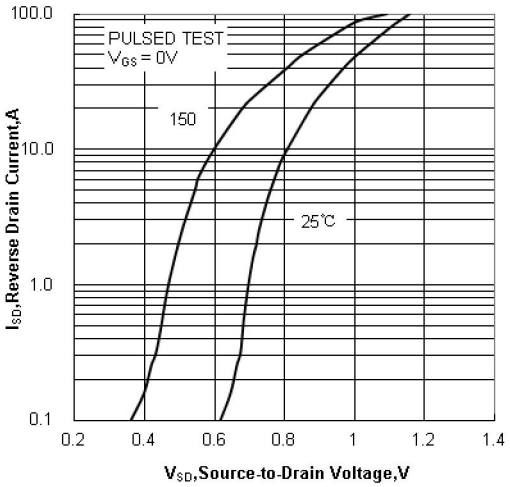
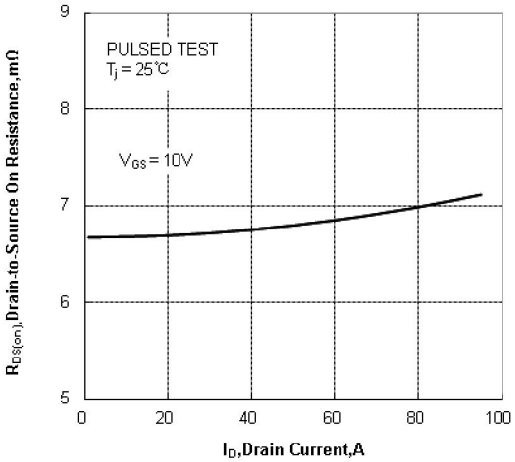
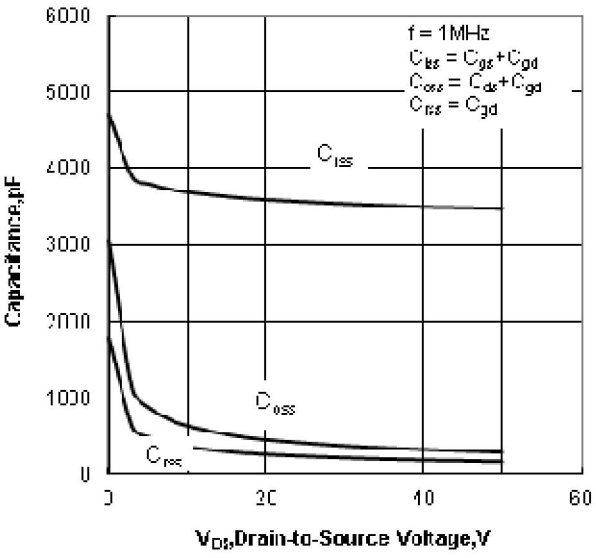


Figure 7. Typical on Resistance VS Drain Current





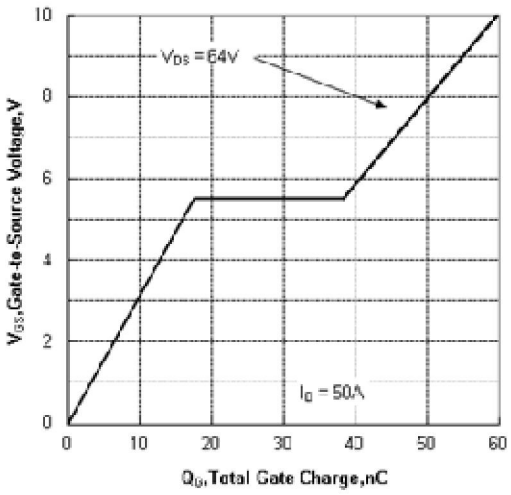


Figure 10. Breakdown Voltage VS Temperature

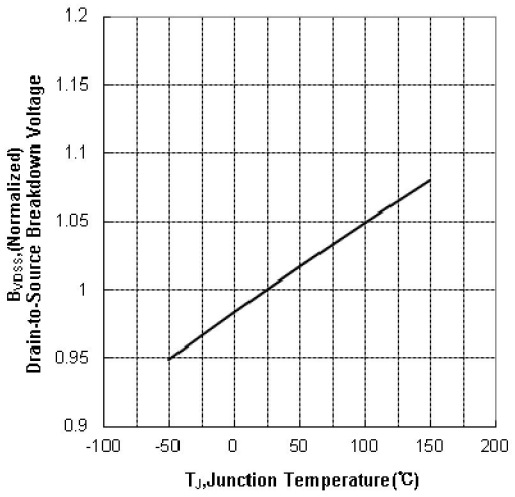
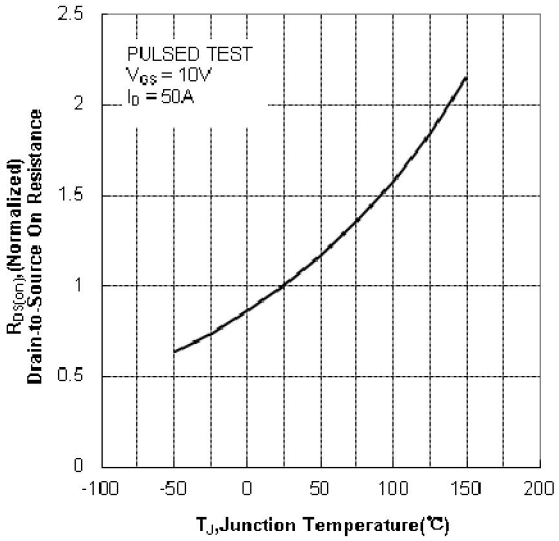
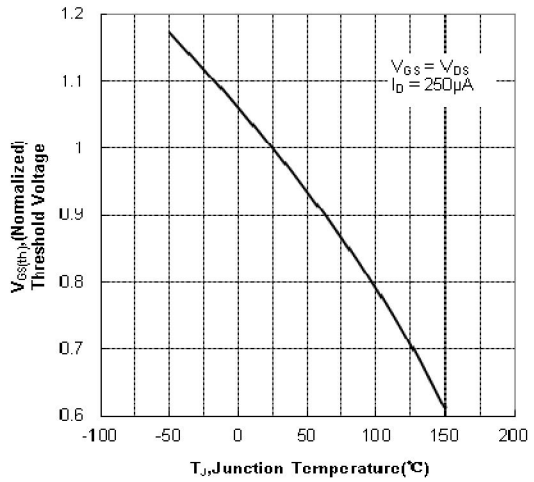
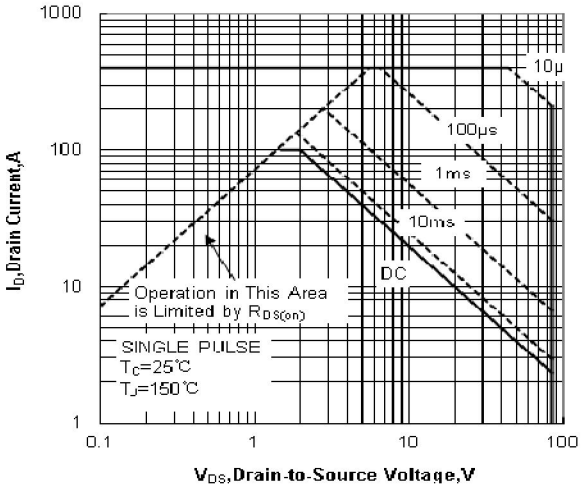


Figure 11. on-Resistance VS Temperature







Test Circuits and Waveforms

Figure 14. Gate Charge Test Circuit

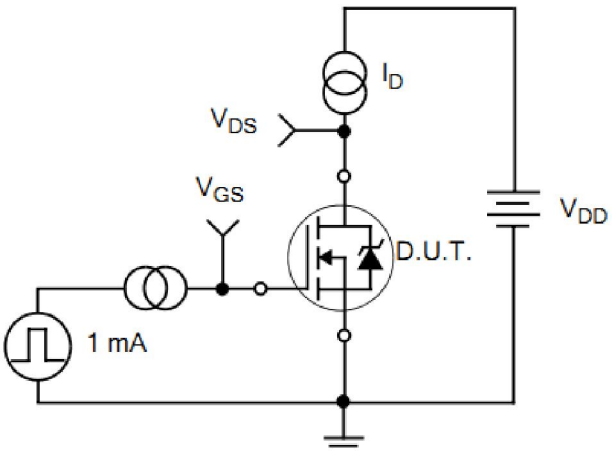


Figure 15. Gate Charge Waveforms

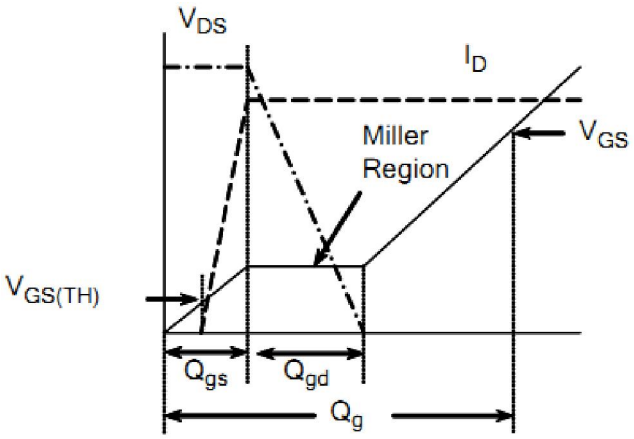


Figure 16. Resistive Switching Test Circuit

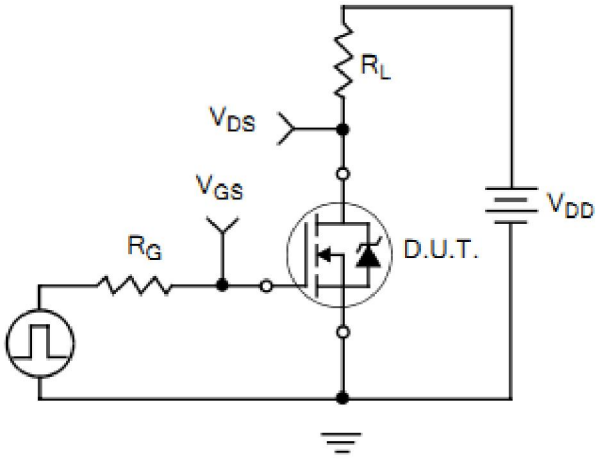


Figure 17. Resistive Switching Waveforms

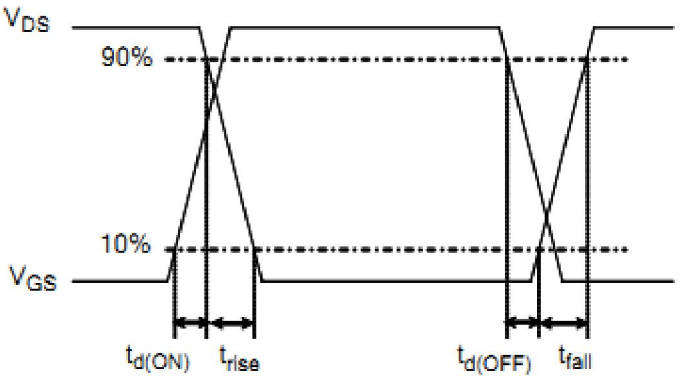


Figure 18. Diode Reverse Recovery Test Circuit

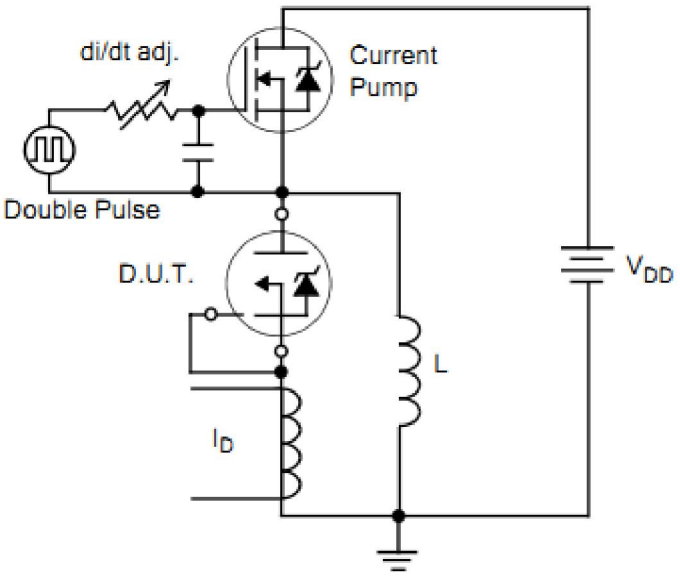


Figure 19. Diode Reverse Recovery Waveform

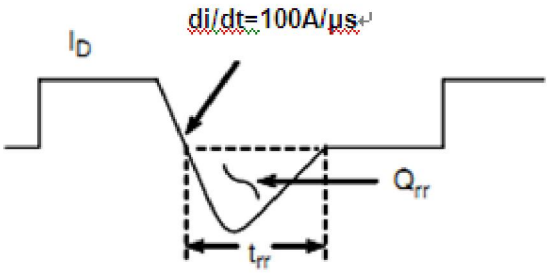


Figure20.Unclamped Inductive Switching Test Circuit

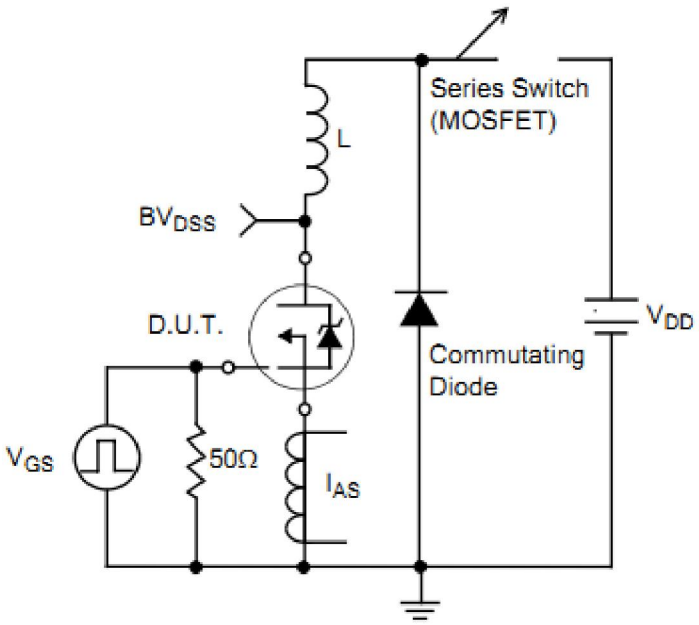
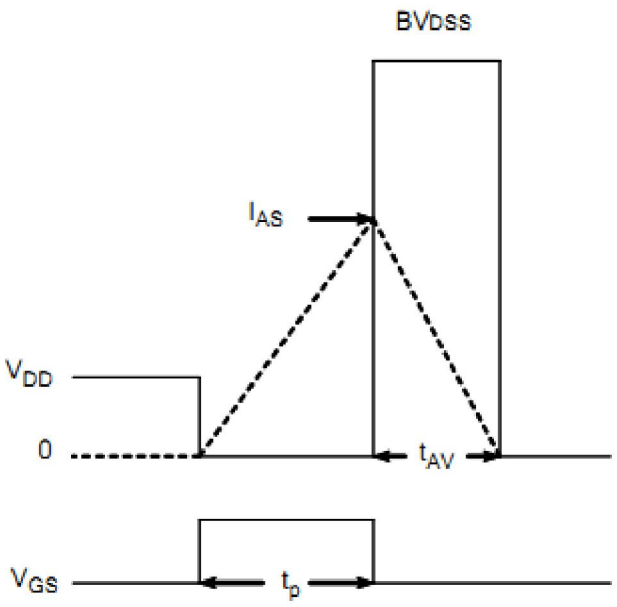


Figure21.Unclamped Inductive Switching Waveform



$$E_{AS} \quad \frac{I_{AS}^{2} L}{2}$$

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